

Delay and power calculation standards —

Part 2: Pre-layout delay calculation specification for CMOS ASIC libraries

The European Standard EN 61523-2:2002 has the status of a
British Standard

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National foreword

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The UK participation in its preparation was entrusted to Technical Committee GEL/93, Design automation, which has the responsibility to:

- aid enquirers to understand the text;
- present to the responsible European committee any enquiries on the interpretation, or proposals for change, and keep the UK interests informed;
- monitor related international and European developments and promulgate them in the UK.

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**Delay and power calculation standards
Part 2: Pre-layout delay calculation specification
for CMOS ASIC libraries
(IEC 61523-2:2002)**

Calcul de puissance et de délai
Partie 2 : Spécification du calcul
du délai de pré-implantation
pour les librairies ASIC CMOS
(CEI 61523-2:2002)

Berechnung von Verzögerung und
Leistungsaufnahme beim Entwurf
von Chips
Teil 2: Vorgezogene Berechnung
der Verzögerung
für CMOS-ASIC-Bibliotheken
(IEC 61523-2:2002)

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This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Foreword

The text of document 93/151/FDIS, future edition 1 of IEC 61523-2, prepared by IEC TC 93, Design automation, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61523-2 on 2002-07-01.

The ASIC Library Representation Working Group of EIAL EDA Technical Committee also participated in the preparation of this standard.

This standard is a revision of the EIAJ ¹⁾ document: ASIC Library Representation (ALR):1994.

The following dates were fixed:

- latest date by which the EN has to be implemented
at national level by publication of an identical
national standard or by endorsement (dop) 2003-04-01
- latest date by which the national standards conflicting
with the EN have to be withdrawn (dow) 2005-07-01

Annexes designated "normative" are part of the body of the standard.
Annexes designated "informative" are given for information only.
In this standard, annex ZA is normative and annexes A to F are informative.
Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 61523-2:2002 was approved by CENELEC as a European Standard without any modification.

¹⁾ Electronic Industries Association of Japan.

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DELAY AND CALCULATION STANDARDS –

Part 2: Pre-layout delay calculation specification for CMOS ASIC libraries

1. Scope and object

This standard specifies the pre-layout delay calculation method for CMOS¹⁾ASIC²⁾ Libraries which contains cell based primitives and memories to be used during the pre-layout design phase of Logic simulation, Timing verification, and Logic synthesis.

The delay calculation method addressed in this standard consists of

- 1) Estimation of wire capacitance and
- 2) Delay calculation method based on tablelook-up.

With use of DCL and SDF, this delay calculation method helps the user have a unified timing model for various EDA tools in the pre-layout design phase.

This standard is consistent with existing standards and accepts existing standard formats, like SPEF, DCL, and SDF.

Scope of this standard covers the CMOS ASIC front end timing design for using logic synthesizer, simulators, timing verifiers.

The delay calculation method specified is based on the input slew rate calculation step and the port to port calculation step.

During these calculation steps, the table lookup method is used.

The table method of this standard specifies two interpolation methods for delay calculation. One is bi-linear interpolation which is widely used through the industry. Another is a linear interpolation using neighboring 3 points.

The nature of the delay value has monotonously increasing function of convex surface. This linear interpolation has a few percent of differences between linear interpolation and SPICE result.

2. Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies

IEEE Standard 1481:1999, *Integrated Circuit (IC) Delay and Power Calculation System*.

¹⁾ Complementary metal oxide semiconductor (CMOS).
²⁾ Application – Specific Integrated Circuits (ASIC).

3. Relations with other companion standards activities

The input to the delay calculator are net list and library.

The net list is described on either Verilog or VHDL.

The library consists of a functional part and a delay parameter part.

The functional part of the library is covered by Verilog or VHDL.

NOTE The delay parameter part of the library has not been standardized, because it depends strongly on the delay calculation method. EIAJ/ALR version 1.1 described the delay calculation method, and the delay calculation method of EIAJ/ALR version 1.1 is represented by DCL and DCL-PI standard (IEEE 1481).

This part of IEC 61523 specifies in detail a table look up calculation formula for CMOS ASIC library¹⁾.

The output of the delay calculator is a Standard Delay Format (SDF).

4. Terms and Definitions

capacitance of the net: Net means equipotential signal pins which will be connected by routing. The capacitance of the net is the capacitance of all the signal pins that are connected by routing.

CMOS: Complementary Metal Oxide Semiconductor.

DCL: Delay Calculation Language.

front end design: Logical design phase of ASIC design. Back end design means layout design.

gate: module containing only one output which is a simple boolean function of its inputs. Some basic simple boolean functions are and/or/not.

input slew rate: Slope of the input signal of the gate. In CMOS, the gate output delay is the function of its input slope of the signal.

load capacitance: Capacitance driven by gate. Usually it is separated into two items: i.e. wiring load capacitance and the sum of input load capacitance.

logic synthesizer: CAD package function performing the translation from RTL-level descriptions to Gate-level descriptions.

port to port delay: One meaning is pin to pin delay inside of gate. The other is pin to pin delay between gates.

pre-layout: Design phase before layout, i.e. logical design phase.

propagation delay: Traveling time of a given edge of a signal. Usually it is separated into two items: i.e. propagation delay inside a gate and propagation

¹⁾ This is not defined in EIAS/ARL version 1.1.

delay from the output of a gate to the input of another gate which is driven by it.

SDF: Standard Delay Format.

simulator: CAD package function of the circuit simulator based on behavior, network, and stimulus. There are Digital and Analog Simulators.

SPEF: Standard Parasitic Exchangeable Format.

SPICE: Simulation Program similar to the program with the same name developed at UC Berkeley. The simulation results are in terms of continuous waveforms representing current or voltage. It emphasizes Integrated Circuit timing and waveforms.

timing verifier: CAD package function that checks register to register timing violations

of setup and hold time. Network description and clock timing are necessary.

transient timing group: Group of signal values. The delay will be defined when the signal changes from one value to the other.

5. Pre-layout delay calculation method for CMOS ASIC libraries

Timing design is the critical issue in sub-micron CMOS ASIC. This clause specifies the detail pre-layout delay calculation.

5.1 Delay model

When considering a sub-micron pre-layout (capacitance-based) timing model, two items should be considered, (1) port to port delay timing and (2) input slew rate effect.

In this model, it is necessary to first calculate the capacitance of wires, and then, calculate delays. As a first step of delay calculation, input slew rate is calculated, and then, port to port delay can be calculated by using the input slew rate.

Therefore, a two step approach is necessary as shown in Figure 1.

Two Step Delay Calculation

step 1: Calculate < Input Slew Rate >

**step 2: Calculate < Port to Port Propagation Delay; T_{pd} >
by using < Input Slew Rate >**

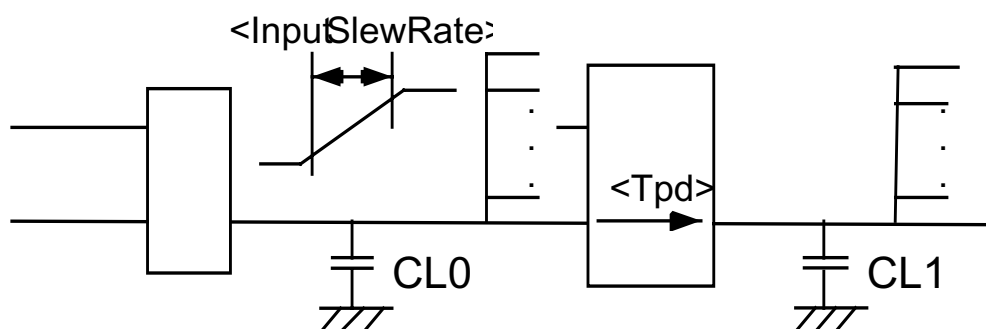


Figure 1: CMOS Delay Model & Calculation Steps

5.2. Table Look-Up delay calculation method

The table look-up model of delay calculation specification uses 3 types of table models. First is the 'Net capacitance table' (named C_n table). This table is used for 'load capacitance' estimation. Second is 'Input slew rate table' (named T_s table), and 3rd is 'Port to port propagation delay time table' (named T_{pd} table). As a first step of delay calculation, input slew rate is calculated by using net capacitance, and T_s table. And then, port to port propagation delay can be calculated by using net capacitance, input slew rate, and T_{pd} table.

The propagation delay is calculated using a T_{pd} table by applying one of the methods for interpolation approximation. One is bilinear interpolation approximation by 4 points. This method will be de facto standard from major EDA vendors. The other is linear interpolation approximation by 3 points. This approximation is more accurate than bilinear interpolation, and both linear and bilinear methods can use the same T_{pd} table.

5.2.1 Load capacitance estimation

First step is to estimate the load capacitance of each net. Load capacitance is estimated by the following rule.

Load Capacitance = (Input port capacitance) + estimated net capacitance
where (Input port capacitance) is the summation of input port capacitance

in the net

The estimated capacitance is a function of fanout and estimated size which is calculated by summing up the cell size of all cells in the top hierarchy to which the net belongs. So, to estimate capacitance, a two dimensional table is used. Indices of the table are fanout and sum of cell size. Different tables should be prepared according to chip size(standard cell) or type of base array(gate array). As shown in figure 2, each net capacitance is calculated by step interpolation using Cn table.

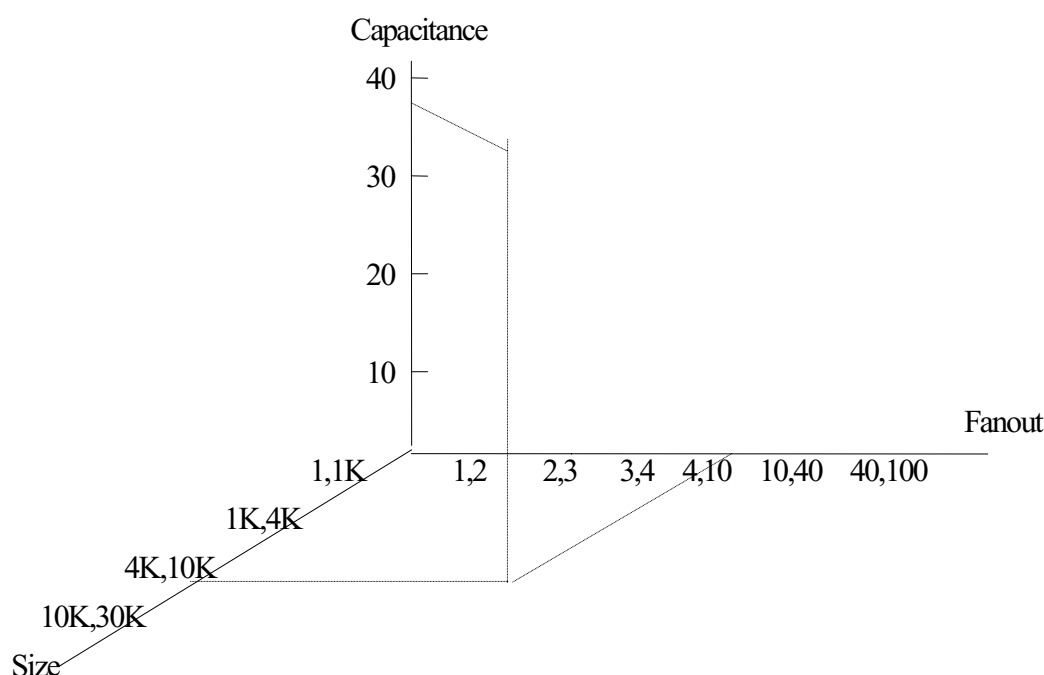


Figure 2. Example of net capacitance estimation

5.2.1.1 Cn table specification

Cn table is a 2 dimensional matrix specified for each design methodology, i.e. gate array, standard cell.(See Annex F.1)

The 1st index is size(S[i]): sum of cell size, or sum of number of gates, or base array size for gate array.

The 2nd index(Fo[j]) is the number of fanout in net.

The value(C[i][j]) is pre-defined capacitance value.

where

1 i M (M is effective maximum number of size values used),

1 j N (N is effective maximum number of fanout values used).

C[i][j] has a real value.

Values of S[i] and Fo[j] have 2 integer values each, which are in the following relationship;

0 first value second value,
 second value of S[i] = first value of S[i+1],

second value of $Fo[j]$ = first value of $Fo[j+1]$,
first value effective value second value,
 $Cn[i][j]$ is real value, unit is pF or fF.

5.2.1.2 Net capacitance(CnE) estimation rule

The Net capacitance estimation (CnE) is specified below.

If the size is ranged in $S[i]$ and the fanout is ranged in $Fo[j]$

then

$$CnE = Cn[i][j] \dots\dots\dots(1)$$

If the size is less than the first value of $S[1]$, then set i to 1.

If the size is greater than or equal to the second value of $S[M]$, then set i to M .

If the fanout is less than the first value of $Fo[1]$, then set j to 1.

If the fanout is greater than or equal to the second value of $Fo[N]$,

then set j to N .

Then apply it to function (1).

5.2.2 Input slew rate calculation

Input slew rate is calculated by linear interpolation shown in figure 3.

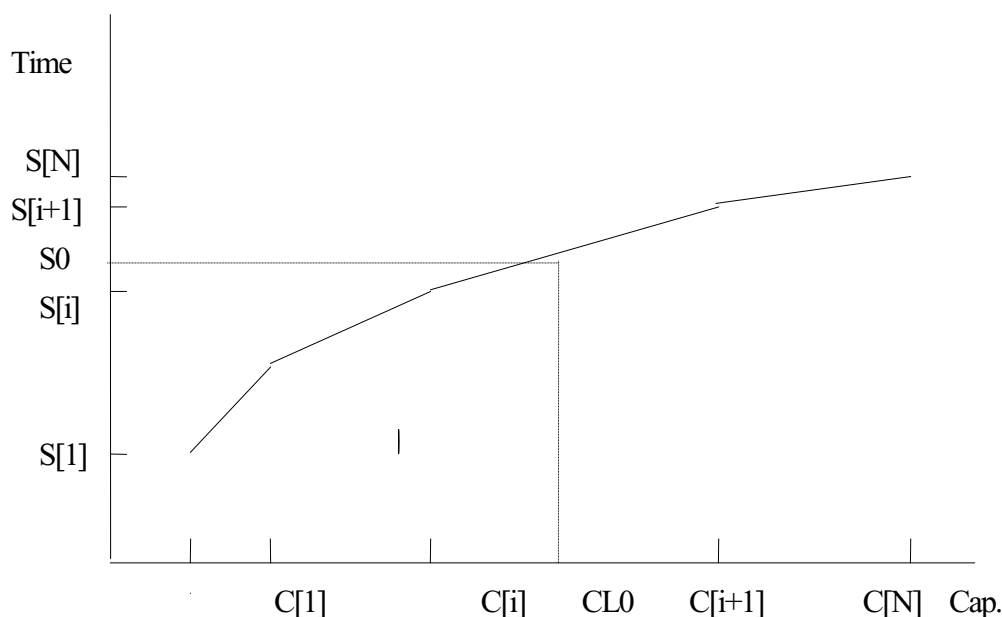


Figure 3. Example of input slew rate calculation

5.2.2.1 Ts table specification

A Ts table is a one dimensional matrix for each transient timing group.(See F.2)

The index($C[i]$) is the capacitance of the net which includes the input of the target gate,

The value($S[i]$) is the characterized input slew rate

where

2 i N (N is effective maximum number of capacitance values used,

$C[i]$ has 1 real value of capacitance, unit is pF or fF,

0 $C[i]$ $C[i+1]$,

$S[i]$ has 1 real value of time, unit is ns.

5.2.2.2 Input slew rate(Ts0) calculation rule

To calculate input slew rate by Ts table, the linear interpolation method will be applied between C[i] and C[i+1].

If target input capacitance(C0) is ranged between C[i] and C[i+1]

then

$$Ts0 = a \cdot C0 + b \dots\dots\dots(2)$$

$$\text{where } a = \frac{S[i+1] - S[i]}{C[i+1] - C[i]}$$

$$b = (C[i+1] - S[i]) \cdot \frac{S[i+1] - S[i]}{C[i+1] - C[i]}$$

If target input capacitance is less than C[1], then set i to 1.

If target input capacitance is greater than C[N],

then set i to N-1.

Then apply it to function of (2).

5.2.3 Port to Port propagation delay time calculation

Port to port delay is calculated using as Tpd table ,shown in Figure 4, using either a linear or a bilinear interpolation method.

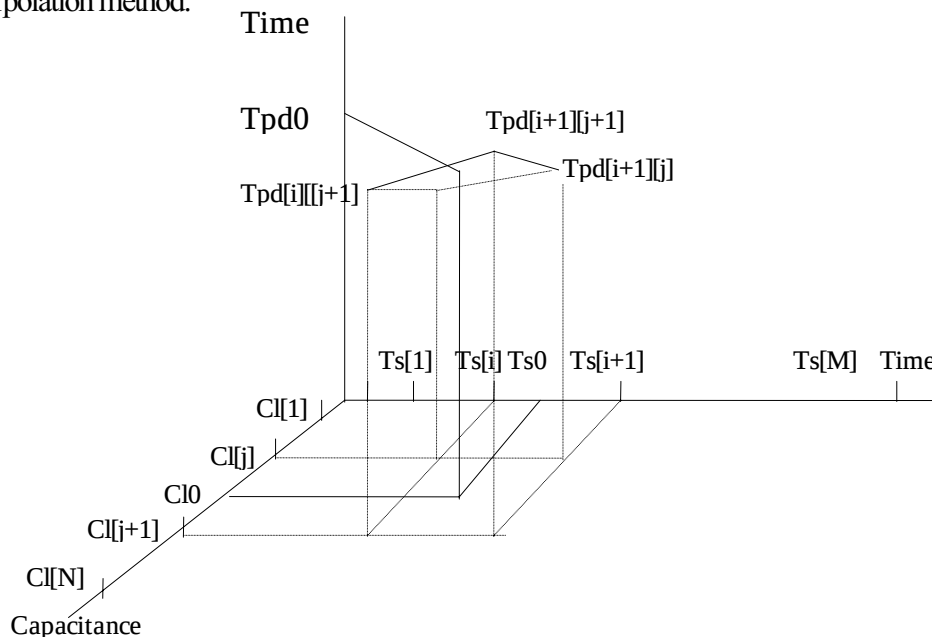


Figure 4. Example of propagation delay time calculation

5.2.3.1 Tpd table specification

Tpd table is a two dimensional matrix for each transient timing group.(See F.3)

The 1st index ($Ts[i]$) is input slew rate ,

The 2nd index($Cl[j]$) is load capacitance of output of gate,

The value ($Tpd[i][j]$) is characterized propagation delay time,

where

$2 \leq i \leq M$ (M is effective maximum number of input slew rates used),

$Ts[i]$ has 1 real value of time, unit is ns,

$0 \leq Ts[i] \leq Ts[i+1]$,

$2 \leq j \leq N$ (N is effective maximum number of load capacitance values of gate output used),

$Cl[j]$ has 1 real value of capacitance, unit is pF or fF,

$0 \leq Cl[j] \leq Cl[j+1]$,

$Tpd[i][j]$ has 1 real value of time, unit is ns,

$Tpd[i][j] \leq Tpd[i+1][j], Tpd[i][j+1] \leq Tpd[i+1][j+1]$.

5.2.3.2 Selection rule of 4 points

To calculate port to port propagation delay time by Tpd table, both linear and bilinear interpolation method are applied among 4 points .

($Tpd[i][j], Tpd[i+1][j], Tpd[i][j+1], Tpd[i+1][j+1]$) as shown in Figure 4.

If calculated Ts_0 is ranged between $Ts[i]$ and $Ts[i+1]$ and

if target load capacitance(CL_1) is ranged between $Cl[j]$ and $Cl[j+1]$,

then select

$Tpd[i][j], Tpd[i+1][j], Tpd[i][j+1], Tpd[i+1][j+1]$.

If Ts_0 is less than $Ts[1]$, set i to 1.

If Ts_0 is greater than $Ts[M]$, set i to M-1.

If CL_1 is less than $Cl[1]$, set j to 1.

If CL_1 is greater than $Cl[N]$, set j to N-1.

Then select

$Tpd[i][j], Tpd[i+1][j], Tpd[i][j+1], Tpd[i+1][j+1]$.

5.2.3.3 Propagation delay time(Tpd_0) approximation

Two methods are specified here.

One is to solve bilinear interpolation ($Z = a \cdot X + b \cdot Y + c \cdot X \cdot Y + d$).

See Annex A in details.

Another method is the linear interpolation based on 3 points which are selected from 4 points shown in figure 5. (See Annex F.4 for detail interpolation example)

5.2.3.3.1 Selection rule of 3 points

Tpd is slowly increasing convex function with negative second derivatives.

In this case, 3 point linear approximation is more accurate than bilinear interpolation