

Behavioural languages —

Part 2: VHDL multilogic system for model interoperability

The European Standard EN 61691-2:2001 has the status of a
British Standard

ICS 35.240.50

National foreword

This British Standard is the official English language version of EN 61691-2:2001. It is identical with IEC 61691-2:2001.

The UK participation in its preparation was entrusted to Technical Committee GEL/93, Design automation, which has the responsibility to:

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- monitor related international and European developments and promulgate them in the UK.

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Summary of pages

This document comprises a front cover, an inside front cover, the EN title page, the EN foreword page, the IEC title page, pages 2 to 23 and a back cover.

The BSI copyright date displayed in this document indicates when the document was last issued.

Amendments issued since publication

Amd. No.	Date	Comments

© BSI 2 April 2002

ISBN 0 580 39266 X

Behavioural languages
Part 2: VHDL multilogic system for model interoperability
(IEC 61691-2:2001)

Langages relatifs au comportement
Partie 2: Système multilogique en VHDL
permettant l'interopérabilité des modèles
(CEI 61691-2:2001)

Verhaltensebenensprache
Teil 2: System für mehrwertige Logik
für das VHDL-Interoperabilitätsmodell
(IEC 61691-2:2001)

This European Standard was approved by CENELEC on 2001-09-01. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Foreword

The text of document 93/130/FDIS, future edition 1 of IEC 61691-2, prepared by IEC TC 93, Design automation, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61691-2 on 2001-09-01.

The following dates were fixed:

- latest date by which the EN has to be implemented
at national level by publication of an identical
national standard or by endorsement (dop) 2002-06-01
- latest date by which the national standards conflicting
with the EN have to be withdrawn (dow) 2004-09-01

This standard is based on IEEE Std 1164:1993, Multivalued logic system for VHDL model interoperability.

Endorsement notice

The text of the International Standard IEC 61691-2:2001 was approved by CENELEC as a European Standard without any modification.

INTERNATIONAL STANDARD

IEC
61691-2

First edition
2001-06

Behavioural languages –

**Part 2:
VHDL multilogic system
for model interoperability**



Reference number
IEC 61691-2:2001(E)

BEHAVIOURAL LANGUAGES - Part 2: VHDL multilogic system for model interoperability

1. Overview

1.1 Scope

This standard is embodied in the Std_logic_1164 package package body along with this clause 1 documentation. The information annex AA is a guide to users and is not part of this standard, but suggests ways in which one might use

1.2 Conformance with this standard

The following conformance rules shall apply as they

- a) No modifications shall be made to the package declaration
- b) The Std_logic_1164 package body represents the formal Std_logic_1164 package declaration. Implementers of this package body as it is; or they may choose to implement to the user. Users shall not implement a semantic that

2. Std_logic_1164 package declaration

```
--  
-- Title   : Std_logic_1164 multivalue logic system  
-- Library : This package shall be compiled into a library  
--         : symbolically named IEEE.  
--         :  
-- Developers: IEEE model standards group (par 1164)  
-- Purpose  : This packages defines a standard for designers  
--         : to use in describing the  
--         : used in VHDL modeling.  
--         :
```

```
-- Limitation: The logic system defined in this package may
--           : be insufficient for modeling switched
--           : since such a requirement is out of the
--           : effort. Furthermore, mathematics, primitives,
--           : timing standards, etc. are considered
--           : issues in relation to this package and
--           : beyond the scope of this effort.
--           :
-- Note      : No declarations or definitions shall be
--           : or excluded from, this package. The
--           : defines the types, subtypes, and
--           : Std_logic_1164. The Std_logic_1164
--           : considered the formal definition of the
--           : this package. Tool developers may
--           : the package body in the most efficient
--           : to them.
--           :
--
-- modification history :
--
-- version | mod. date:|
-- v4.200 | 01/02/92 |
--
PACKAGE Std_logic_1164 IS

    -- logic state system (unresolved)

    TYPE std_ulogic IS ( 'U', -- Uninitialized
                        'X', -- Forcing Unknown
                        '0', -- Forcing 0
                        '1', -- Forcing 1
                        'Z', -- High Impedance
                        'W', -- Weak Unknown
                        'L', -- Weak 0
                        'H', -- Weak 1
                        '-' -- Don't care
                      );

    -- unconstrained array of std_ulogic for use with the

    TYPE std_ulogic_vector IS ARRAY ( NATURAL RANGE <> )

    -- resolution function

    FUNCTION resolved ( s : std_ulogic_vector ) RETURN std_ulogic;

    -- *** industry standard logic type ***
    -----
    SUBTYPE std_logic IS resolved std_ulogic;

    -- unconstrained array of std_logic for use in

    TYPE std_logic_vector IS ARRAY ( NATURAL RANGE <> ) OF
```

-- common subtypes

```
SUBTYPE X01   IS resolved std_ulogic RANGE '
SUBTYPE X01Z  IS resolved std_ulogic RANGE "Z"
SUBTYPE UX01  IS resolved std_ulogic RANGE "1"
SUBTYPE UX01Z IS resolved std_ulogic RANGE "1", 'Z')
```

-- overloaded logical operators

```
FUNCTION "and" (l : std_ulogic; r :
FUNCTION "nand" (l : std_ulogic; r :
FUNCTION "or"   (l : std_ulogic; r :
FUNCTION "nor"  (l : std_ulogic; r :
FUNCTION "xor"  (l : std_ulogic; r :
FUNCTION "xnor" (l : std_ulogic; r :
FUNCTION "not"  (l : std_ulogic
```

-- vectorized overloaded logical operators

```
FUNCTION "and" (l, r : std_logic_vector )
FUNCTION "and" (l, r : std_ulogic_vector )
FUNCTION "nand" (l, r : std_logic_vector )
FUNCTION "nand" (l, r : std_ulogic_vector )
FUNCTION "or"   (l, r : std_logic_vector )
FUNCTION "or"   (l, r : std_ulogic_vector )
FUNCTION "nor"  (l, r : std_logic_vector )
FUNCTION "nor"  (l, r : std_ulogic_vector )
FUNCTION "xor"  (l, r : std_logic_vector )
FUNCTION "xor"  (l, r : std_ulogic_vector )
```

--

-- Note : The declaration and implementation of the "
 -- specifically commented until a time at which the VHDL
 -- officially adopted as containing such a function. At
 -- the following comments may be removed along with this
 -- further "official" balloting of this
 -- the intent of this effort to provide such a function
 -- available in the VHDL standard.

--

```
-- FUNCTION "xnor" (l, r : std_logic_vector )
-- FUNCTION "xnor" (l, r : std_ulogic_vector )
FUNCTION "not" (l : std_logic_vector )
FUNCTION "not" (l : std_ulogic_vector )
```

-- conversion functions

```
FUNCTION To_bit    (s : std_ulogic;   xmap :
FUNCTION To_bitvector (s : std_logic_vector ; xmap : BIT_VECTOR;
FUNCTION To_bitvector (s : std_ulogic_vector; xmap : BIT_VECTOR;
FUNCTION To_StdULogic    (b : BIT
FUNCTION To_StdLogicVector (b : BIT_VECTOR
FUNCTION To_StdLogicVector (s : std_ulogic_vector ) RETURN std_logic_vector;
FUNCTION To_StdULogicVector (b : BIT_VECTOR
FUNCTION To_StdULogicVector (s : std_logic_vector ) RETURN std_ulogic_vector;
```

```
-- strength strippers and type converters

FUNCTION To_X01 ( s : std_logic_vector ) RETURN
FUNCTION To_X01 ( s : std_ulogic_vector ) RETURN
FUNCTION To_X01 ( s : std_ulogic      ) RETURN X01;
FUNCTION To_X01 ( b : BIT_VECTOR      ) RETURN
FUNCTION To_X01 ( b : BIT_VECTOR      ) RETURN
FUNCTION To_X01 ( b : BIT              ) RETURN X01;
FUNCTION To_X01Z ( s : std_logic_vector ) RETURN
FUNCTION To_X01Z ( s : std_ulogic_vector ) RETURN
FUNCTION To_X01Z ( s : std_ulogic      ) RETURN X01Z;
FUNCTION To_X01Z ( b : BIT_VECTOR      ) RETURN
FUNCTION To_X01Z ( b : BIT_VECTOR      ) RETURN
FUNCTION To_X01Z ( b : BIT              ) RETURN X01Z;
FUNCTION To_UX01 ( s : std_logic_vector ) RETURN
FUNCTION To_UX01 ( s : std_ulogic_vector ) RETURN
FUNCTION To_UX01 ( s : std_ulogic      ) RETURN UX01;
FUNCTION To_UX01 ( b : BIT_VECTOR      ) RETURN
FUNCTION To_UX01 ( b : BIT_VECTOR      ) RETURN
FUNCTION To_UX01 ( b : BIT              ) RETURN UX01;

-- edge detection

FUNCTION rising_edge (SIGNAL s : std_ulogic) RETURN BOOLEAN;
FUNCTION falling_edge (SIGNAL s : std_ulogic) RETURN BOOLEAN;

-- object contains an unknown

FUNCTION Is_X ( s : std_ulogic_vector ) RETURN BOOLEAN;
FUNCTION Is_X ( s : std_logic_vector   ) RETURN BOOLEAN;
FUNCTION Is_X ( s : std_ulogic         ) RETURN BOOLEAN;
END Std_logic_1164;
```

3. Std_logic_1164 package body

```
--
--
-- Title   : Std_logic_1164 multivalue logic system
-- Library : This package shall be compiled into a library
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-- Developers: IEEE model standards group (par 1164)
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-- Limitation: The logic system defined in this package may
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--          : effort. Furthermore, mathematics, primitives,
--          : timing standards, etc., are considered
--          : issues in relation to this package and
```