

Consumer audio/video equipment — Digital interface —

Part 1: General

The European Standard EN 61883-1:1998 has the status of a
British Standard

ICS 33.160.01; 35.200

National foreword

This British Standard is the English language version of EN 61883-1:1998. It is identical with IEC 61883-1:1998.

The UK participation in its preparation was entrusted by Technical Committee EPL/100, Audio, video and multimedia systems and equipment, to Subcommittee EPL/100/3, Equipment and systems in the field of audio, video and audiovisual engineering, which has the responsibility to:

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Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, the EN title page, pages 2 to 38 and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

Amendments issued since publication

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Digital interface
Part 1: General

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Unterhaltungselektronik
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CENELEC

European Committee for Electrotechnical Standardization
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Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B-1050 Brussels

Foreword

The text of document 100C/182/FDIS, future edition 1 of IEC 61883-1, prepared by SC 100C, Audio, video and multimedia subsystems and equipment, of IEC TC 100, Audio, video and multimedia systems and equipment, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61883-1 on 1998-04-01.

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Endorsement notice

The text of the International Standard IEC 61883-1:1998 was approved by CENELEC as a European Standard without any modification.

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1 Scope and object

This part of IEC 61883 specifies a digital interface for consumer electronic audio/video equipment using the IEEE 1394 standard. It describes the general packet format, data flow management and connection management for audiovisual data, and also the general transmission rules for control commands.

The object of this standard is to define the transmission protocol for audiovisual data and control commands which provides for the connectability of digital audio and video equipment, using the IEEE 1394 standard.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 61883. At the time of publication, the editions indicated were valid. All normative documents are subject to revision, and parties to agreements based on this part of IEC 61883 are encouraged to investigate the possibility of applying the most recent editions of the normative documents listed below. Members of IEC and ISO maintain registers of currently valid International Standards.

ISO/IEC 13213:1994, *Information technology — Microprocessor systems — Control and Status Registers (CSR) Architecture for microcomputer buses*.

IEEE 1394:1995, *Standard for a High Performance Serial Bus*.

3 Definitions, symbols and abbreviations

For the purpose of this part of IEC 61883, the following abbreviations and definitions of IEEE 1394 apply:

AV/C	audio video control
CHF	CIP header field
CIP	common isochronous packet
CMP	connection management procedures
CSR	command and status register
CTS	command/transaction set
CRC	cyclic redundancy check code
DVCR	digital video cassette recorder
EOH	end of CIP header
FCP	function control protocol
iPCR	input plug control register
iMPR	input master plug register
MPEG	motion picture experts group
oPCR	output plug control register
oMPR	output master plug register
PCR	plug control register
ROM	read only memory
cycle master capable	
isochronous resource manager capable	
quadlet	
S100	
S200	
S400	

4 High performance serial bus layers

4.1 Cable physical layer

All cable physical layer implementations conforming to this standard shall meet the performance criteria specified in IEEE 1394, chapter 4. In addition to the cable and connector defined in IEEE 1394, the AV cable and connector defined in Annex A may be used.

For AV devices, it is recommended not to generate a bus reset until access to the bus has been granted as specified in IEEE 1394. Furthermore, it is recommended that AV devices maintain the reset condition on the bus for the minimum time permitted by IEEE 1394.

4.2 Link layer

All link layer implementations conforming to this standard shall meet the performance criteria specified in IEEE 1394, chapter 6.

4.3 Transaction layer

All transaction layer implementations conforming to this standard shall meet the performance criteria specified in IEEE 1394, chapter 7.

5 Serial bus management

5.1 Basic serial bus management

All implementations regarding basic serial bus management conforming to this standard shall meet the performance criteria specified in IEEE 1394, chapter 8.

5.2 Bus management capability

A node shall conform to the following requirements:

- a node shall be cycle master capable. This is because every node has the possibility to be assigned as a root;
- a node shall be isochronous resource manager capable;
- a node which transmits or receives the isochronous packets shall have plug control registers (see 7.2).

5.3 Command and status registers

5.3.1 CSR core registers

This standard uses the standardized CSR architecture. Details of the registers are given in the IEEE 1394 standard. There are no additional requirements for implementations of this standard except for the STATE_CLEAR.cmstr bit.

The STATE_CLEAR.cmstr bit shall be implemented, since a node shall be cycle master capable as described previously. A special emphasis in this standard is that cmstr bit is set automatically by system software or hardware. It shall be executed when a node becomes the new root after the bus reset initialization process is completed. In this manner, it is possible to ensure the fast resumption and continuity of data transmission where the time scale is critical at the level of microseconds.

5.3.2 Serial bus node registers

Implementation requirements for bus-dependent registers in this standard conform to IEEE 1394. A node shall have the following registers:

- CYCLE_TIME register
- BUS_TIME register
- BUS_MANAGER_ID register
- BANDWIDTH_AVAILABLE register
- CHANNELS_AVAILABLE register

5.3.3 Configuration ROM requirements

A node shall implement the general ROM format as defined in ISO/IEC 13213 and IEEE 1394. Additional information required for implementations of this standard shall be included in one of the unit directories. Figure 1 shows an example of the configuration ROM implementation for this standard.

5.3.3.1 *Bus_Info_Block entry*

Implementation requirements for bus_info_block in this standard conform to IEEE 1394. The Node_Unique_Id shall be present in the bus_info_block.

5.3.3.2 *Root directory*

The following entries shall be present:

- Module_Vendor_Id;
- Node_Capabilities;
- Node_unique_id offset;
- Unit_Directory offset for this standard.

Other entries can be implemented in addition to the above required entries.

5.3.3.3 *Unit directory*

The following entries shall be present:

- Unit_Spec_Id;
- Unit_Sw_Version.

The value of the Unit_Spec_Id and the Unit_Sw_Version for this standard are given as follows:

Unit_Spec_Id:	First octet	= 00 ₁₆
	Second octet	= A0 ₁₆
	Third octet	= 2D ₁₆
Unit_Sw_Version:	First octet	= 01 ₁₆

The second and third octets are reserved for this standard and indicate capabilities for command/transaction sets. The 4-bit CTS (see 9.3) allows 16 command/transaction sets. Each bit of the second and third octets corresponds to one command/transaction set. The least significant bit corresponds to CTS code = 0000₂. The most significant bit corresponds to CTS code = 1111₂. When a node supports a CTS, the node shall set the corresponding bit to 1. A node may support more than one (plural) CTS.

6 Real time data transmission protocol

6.1 Common isochronous packet (CIP) format

6.1.1 *Isochronous packet structure*

The structure of the isochronous packet for this standard is as illustrated in Figure 2. The packet header and header CRC are placed as the first two quadlets of an IEEE 1394 isochronous packet. The CIP header is placed at the beginning of the data field of an IEEE 1394 isochronous packet, immediately followed by zero or more data blocks.

6.1.2 *Packet header structure*

The packet header consists of the following items as specified in IEEE 1394.

Data_length:	specifies the length of the data field of the isochronous packet in bytes, which is determined as follows: CIP header size + signal data size
Tag:	provides a high level label for the format of data carried by the isochronous packet. 00 ₂ = No CIP header included 01 ₂ = CIP header included as specified in 6.1.3 10 ₂ = Reserved 11 ₂ = Reserved
Channel:	specifies the isochronous channel number for the packet.
Tcode:	specifies the packet format and the type of transaction that shall be performed (fixed at 1010 ₂).
Sy:	Application-specific control field.

6.1.3 CIP header structure

The CIP header is placed at the beginning of the data field of an IEEE 1394 isochronous packet. It contains information on the type of the real time data contained in the data field following it. The structure of the CIP header is shown in Figure 3.

The definitions of the fields are given as follows:

EOH_n (End of CIP header): means the last quadlet of a CIP header.

0 = Another quadlet will follow

1 = The last quadlet of a CIP header

Form_n: in combination with EOH, shows the additional structure of CHF_n.

CHF_n (CIP header field): CIP header field of nth quadlet. The additional structure of CHF_n depends on EOH_0, form_0, EOH_1, form_1, ... EOH_n, and form_n.

6.2 Transmission of fixed length source packet

This protocol transfers a stream of source packets from an application on a device to an application on other device(s). A source packet is assumed to have a fixed length, which is defined for each type of data. The data rate can be variable.

A source packet may be split into 1, 2, 4 or 8 data blocks, and zero or more data blocks are contained in an IEEE 1394 isochronous packet. A receiver of the packet shall collect the data blocks in the isochronous packet and combine them to reconstruct the source packet to send to the application.

A model complying with above statement is shown in Figure 4.

6.2.1 Two-quadlet CIP header (form_0=0, form_1=0)

This standard defines the two-quadlet CIP header for a fixed length source packet. There are two types for the structure of the two quadlet CIP header as shown in Figure 5. One is the CIP header with SYT field (Figure 5a), and the other is the CIP header without SYT field (Figure 5b). If a device transmits real time data (identified by FMT) and requires time stamp in the CIP header, it shall use the SYT format.

The definitions of the fields are given as follows.

— SID: Source node ID (node ID of transmitter);

— DBS: Data block size in quadlets;

DBS field is 8 bits because 256 quadlets is the maximum payload size for S100 mode. When 8 bits are all 0, it means 256 quadlets; and 00000001₂ to 11111111₂ means 1 quadlet to 255 quadlets accordingly.

00000000₂ = 256 quadlets

00000001₂ = 1 quadlet

00000010₂ = 2 quadlets

.....

11111111₂ = 255 quadlets

Several data blocks may be put into a bus packet, which is a packet to be transmitted on the bus, if higher bandwidth is required for S200 and S400 mode.

NOTE S100, S200, S400 are transmission modes as defined in IEEE 1394.

— FN: Fraction number

The number of data blocks into which a source packet is divided. The allowable numbers and allocated FN codes are listed in Table 1.

— QPC: Quadlet padding count (0 quadlet to 7 quadlets)

The number of dummy quadlets padded at the end of every source packet to enable division into equally sized data blocks. The value of all bits in padding quadlets is always zero.

The number of padding quadlets shall be less than the number of data blocks into which every source packet is divided, as encoded by FN.

The number of padding quadlets shall be less than the size of a single data block, as encoded by DBS. Consequently, a data block shall never consist entirely out of padding quadlets.

- SPH: Source packet header;

The value one indicates that the source packet has a source packet header. The format of the source packet header is shown in Figure 6. Code allocation of the time stamp field is shown in Table 4a.

When a time stamp is indicated, the time stamp field shall be encoded as the lower 25 bits of the IEEE 1394 CYCLE_TIME register. Other bits are reserved for future extension and shall be zeros.

- Rsv: Reserved for future extension and shall be zeros.

- DBC: DBC is the continuity counter of data blocks for detecting a loss of data blocks.

The value refers to the first data block following the CIP header in the bus packet. The lower FN bits contain the sequence number of the data block within its source packet. The remaining 8-FN bits form the sequence number of the source packet. The first data block of any source packet always has a sequence number with value zero. If FN is zero, then all 8 bits of DBC are used to represent a source packet sequence number. See also Table 2.

- FMT: Format ID

The code allocation is illustrated in Table 3.

If FMT is 111111₂ (no data), the fields for DBS, FN, QPC, SPH and DBC are ignored and no data blocks shall be transmitted. The most significant bit of the FMT field identifies SYT_available/SYT_not_available. See also Figure 5 and Table 3.

- FDF: Format dependent field

This field is defined for each FMT.

- SYT: The code allocation of the SYT field is shown in Table 4b. When a time stamp is indicated by the msb of the FMT field, the SYT field shall be encoded as the lower 16 bits of the IEEE 1394 CYCLE_TIME register.

6.2.2 Isochronous packet transmission

Active transmitters shall send an isochronous packet in every cycle. If no data block is available, an empty packet shall be sent. An empty packet shall always contain a two-quadlet CIP header. The DBC field of empty packet shall show the count for the first data block contained in the first non-empty IEEE 1394 isochronous packet following this empty packet. The other fields shall match the fields of the CIP header of non-empty packets on the same transmission stream.

7 Isochronous data flow management

7.1 Introduction

To start and stop isochronous data flows on the bus and to control their attributes, the concept of plugs and plug control registers is used. Plug control registers are special purpose CSR registers.

NOTE Plugs do not physically exist on an AV device. Only the concept of a plug is used to establish an analogy with existing AV devices where each flow of information is routed via a physical plug.

The contents of the plug control registers and how they may be modified is described in this clause. The set of procedures that use the plug control registers to control an isochronous data flow are called connection management procedures (CMP). The CMP that shall be used by AV devices is described in clause 8.

7.2 Plugs and plug control registers

An isochronous data flow flows from one transmitting AV device to zero or more receiving AV devices by sending isochronous packets on one isochronous channel of the IEEE 1394 bus. An isochronous channel shall not carry more than one isochronous data flow and each isochronous data flow shall be carried on one isochronous channel.

Each isochronous data flow is transmitted to an isochronous channel through one **output plug** on the transmitting AV device and it is received from that isochronous channel through one **input plug** on each of the receiving AV devices. Each input and output plug shall not carry more than one isochronous data flow.

The transmission of an isochronous data flow through an output plug is controlled by one **output plug control register (oPCR)** and one **output master plug register (oMPR)** located on the transmitting AV device. On each AV device there is only one OUTPUT_MASTER_PLUG register for all output plugs. The OUTPUT_MASTER_PLUG register controls all attributes that are common to all isochronous data flows transmitted by the corresponding AV device. The OUTPUT_PLUG_CONTROL register controls all attributes of the corresponding isochronous data flow that are independent from attributes of other isochronous data flows transmitted by that AV device.

The reception of an isochronous data flow through an input plug is controlled by one **input plug control register (iPCR)** and one **input master plug register (iMPR)** located on the receiving AV device. On each AV device there is only one INPUT_MASTER_PLUG register for all input plugs. The INPUT_MASTER_PLUG register controls all attributes that are common to all isochronous data flows received by the corresponding AV device. The INPUT_PLUG_CONTROL register controls all attributes of the corresponding isochronous data flow that are independent from attributes of other isochronous data flows received by that AV device.

An isochronous data flow can be controlled by any device connected to the IEEE 1394 bus by modifying the corresponding plug control registers. Plug control registers can be modified by means of asynchronous transactions on the IEEE 1394 bus or by internal modifications if the plug control registers are located on the controlling device.

The usage of plugs and plug control registers is illustrated in Figure 7.

Let $\#iPCR$ and $\#oPCR$ denote the number of isochronous data flows that can be simultaneously received and transmitted respectively by an AV device (such as a multiple viewing device or a multiple tuner device). Both $\#iPCR$ and $\#oPCR$ shall be constants in the range $[0 \dots 31]$ that are AV device dependent.

Each AV device shall implement $\#oPCR$ output plugs each controlled by one separate OUTPUT_PLUG_CONTROL register and $\#iPCR$ input plugs, each controlled by one separate INPUT_PLUG_CONTROL register. For AV devices implementing INPUT_PLUG_CONTROL registers, a single INPUT_PLUG_CONTROL register within that AV device shall be denoted as INPUT_PLUG_CONTROL[i], where i is in the range $[0 \dots \#iPCR-1]$. The INPUT_MASTER_PLUG register is optional when $\#iPCR = 0$ and mandatory otherwise. For AV devices implementing OUTPUT_PLUG_CONTROL registers, a single OUTPUT_PLUG_CONTROL register within that AV device shall be denoted as OUTPUT_PLUG_CONTROL[i], where i is in the range $[0 \dots \#oPCR-1]$. The OUTPUT_MASTER_PLUG register is optional if $\#oPCR = 0$ and mandatory otherwise.

The mapping between an INPUT_PLUG_CONTROL register and an isochronous data flow in a receiving AV device and the mapping between an OUTPUT_PLUG_CONTROL register and an isochronous data flow in a transmitting AV device is AV device dependent.

7.3 Connections

To transport isochronous data between two AV devices on the IEEE 1394 bus, it is necessary for an application to connect an output plug on the transmitting AV device to an input plug on the receiving AV device using one isochronous channel. The relationship between one input plug, one output plug and one isochronous channel is called a **point-to-point connection**. A point-to-point connection can only be broken by the same application that established it.

It is also possible that an application just starts the transmission or the reception of an isochronous data flow on its own AV device by connecting one of its output or input plugs respectively to an isochronous channel. The relationship between one output plug and one isochronous channel is called a **broadcast-out connection**. The relationship between one input plug and one isochronous channel is called a **broadcast-in connection**. Broadcast-out and broadcast-in connections are collectively called **broadcast connections**. A broadcast connection can be established only by the AV device on which the plug is located but it can be broken by any device. The concept of connections is illustrated in Figure 8.

Only one broadcast-out connection can exist in an output plug and only one broadcast-in connection can exist in an input plug. One broadcast connection and multiple point-to-point connections can exist simultaneously in one plug. This can be achieved by overlaying a connection over existing connections in the same input or output plug. Note that all connections that exist in one plug use the same isochronous channel and transport the same isochronous data flow. Multiple independent applications can create point-to-point connections between the same input and output plug.