

Consumer audio/video equipment — Digital interface —

Part 1: General

The European Standard EN 61883-1:2003 has the status of a
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National foreword

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CENELEC

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Foreword

The text of document 100/557/FDIS, future edition 2 of IEC 61883-1, prepared by technical area 4, Digital system interfaces, of IEC TC 100, Audio, video and multimedia systems and equipment, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61883-1 on 2003-03-01.

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Annexes designated "normative" are part of the body of the standard.
Annexes designated "informative" are given for information only.
In this standard, annex ZA is normative and annex A is informative.
Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 61883-1:2003 was approved by CENELEC as a European Standard without any modification.

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CONSUMER AUDIO/VIDEO EQUIPMENT – DIGITAL INTERFACE –

Part 1: General

1 Scope

This part of IEC 61883 specifies a digital interface for consumer electronic audio/video equipment using IEEE 1394, High Performance Serial Bus. It describes the general packet format, data flow management and connection management for audio-visual data, and also the general transmission rules for control commands.

The object of this standard is to define a transmission protocol for audio-visual data and control commands which provides for the interconnection of digital audio and video equipment, using IEEE 1394.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEEE 1212:2001, *Standard for a Control and Status Registers (CSR) Architecture for microcomputer buses*

IEEE 1394:1995, *Standard for a High Performance Serial Bus*

IEEE 1394a:2000, *Standard for a High Performance Serial Bus – Amendment 1*

NOTE Throughout this document, the term “IEEE 1394” indicates a reference to the standard that is the result of the editorial combination of IEEE 1394:1995 and IEEE 1394a:2000. Devices conforming solely to IEEE 1394:1995 may conform to IEC 61883. Devices conforming to IEC 61883 should conform to IEEE 1394a:2000.

3 Abbreviations

For the purpose of this part of IEC 61883, the following abbreviations apply:

AV/C	Audio Video Control
CHF	CIP Header Field
CIP	Common Isochronous Packet
CMP	Connection Management Procedures
CSR	Command and Status Register
CTS	Command/Transaction Set
CRC	Cyclic Redundancy Check Code
DVCR	Digital Video Cassette Recorder
EOH	End of CIP Header
FCP	Function Control Protocol
iPCR	Input Plug Control Register
iMPR	Input Master Plug Register
MPEG	Motion Picture Experts Group
oPCR	Output Plug Control Register
oMPR	Output Master Plug Register
ROM	Read Only Memory

4 High performance serial bus layers

4.1 Cable physical layer

All cable physical layer implementations conforming to this standard shall meet the performance criteria specified by IEEE 1394. Either the cable and connector defined in IEEE 1394:1995, or the cables and connector defined in IEEE 1394a:2000, shall be used.

When necessary for an AV device to generate a bus reset, it shall follow the requirements of IEEE 1394a:2000, 8.2.1. An AV device that initiates a bus reset should generate an arbitrated (short) bus reset, as specified by IEEE 1394a:2000, in preference to the long bus reset defined by IEEE 1394:1995.

4.2 Link layer

All link layer implementations conforming to this standard shall meet the specifications of IEEE 1394.

4.3 Transaction layer

All transaction layer implementations conforming to this standard shall meet the specifications of IEEE 1394.

5 Minimum node capabilities

A node shall conform to the following requirements:

- a node shall be cycle master capable. This is because every node has the possibility to be assigned as a root;
- a node shall be isochronous resource manager capable, as specified by IEEE 1394:1995, and shall implement the additional isochronous resource manager facilities and responsibilities specified by IEEE 1394a:2000 in subclauses 8.3.1.5, 8.3.2.3.8, 8.3.2.3.11, 8.4.2.3 and 8.4.2.6A;
- a node which transmits or receives isochronous packets shall have plug control registers (see 7.2).

5.1 Serial bus management

Bus manager capability is optional for AV devices, but, if implemented by devices conforming to this standard, shall conform to IEEE 1394.

5.2 Command and status registers

5.2.1 CSR core registers

This standard conforms to the CSR architecture. Details of its registers are specified by IEEE 1394.

The STATE_CLEAR.*cmstr* bit shall be implemented as specified by IEEE 1394a:2000, 8.3.2.2.1.

NOTE The *cmstr* bit is set automatically (see IEEE 1394a:2000, 8.3.2.2.1) by system software or hardware when a node becomes the new root after the bus reset process is completed. In this manner, it is possible to ensure the fast resumption and continuity of data transmission where the time scale is critical at the level of microseconds. The rapid activation of a new cycle master decreases the likelihood of a gap in the transmission of cycle start packets; uninterrupted transmission of cycle start packets at nominal 125 µs intervals is critical to the delivery of isochronous data within its latency requirements.

5.2.2 Serial bus node registers

Implementation requirements for bus-dependent registers in this standard conform to IEEE 1394. A node shall have the following registers:

CYCLE_TIME register
 BUS_TIME register
 BUS_MANAGER_ID register
 BANDWIDTH_AVAILABLE register
 CHANNELS_AVAILABLE register

A node should have the following register specified by IEEE 1394a:2000:

BROADCAST_CHANNEL register

5.2.3 Configuration ROM requirements

A node shall implement the general ROM format as defined in IEEE 1212:2001 and IEEE 1394. Additional information required for implementations of this standard shall be included in one of the unit directories. Figure 1 shows an example of the configuration ROM implementation for this standard.

5.2.3.1 Bus_Info_Block entry

Implementation requirements for the Bus_Info_Block in this standard shall conform to IEEE 1394.

5.2.3.2 Root directory

The following entries shall be present:

- Module_Vendor_ID;
- Node_Capabilities;
- Unit_Directory (offset to a unit directory defined by this standard).

Other entries may be implemented in addition to the above required entries.

5.2.3.3 Unit directory

The following entries shall be present:

- Unit_Spec_ID;
- Unit_SW_Version.

The value of the Unit_Spec_ID and the Unit_SW_Version for this standard are given as follows:

Unit_Spec_ID:	First octet	= 00 ₁₆
	Second octet	= A0 ₁₆
	Third octet	= 2D ₁₆
Unit_SW_Version:	First octet	= 01 ₁₆

The second and third octets of Unit_SW_Version for this standard are specified in Table 9 and indicate capabilities for command/transaction sets. The Unit_SW_Version field is used to identify which protocol is supported by the device. If a device supports more than one protocol, the device shall have a separate unit directory for each protocol supported.

6 Real time data transmission protocol

6.1 Common isochronous packet (CIP) format

6.1.1 Isochronous packet structure

The structure of the isochronous packet utilized by this standard is illustrated in Figure 2. The packet header and header CRC are the first two quadlets of an IEEE 1394 isochronous packet. The CIP header is placed at the beginning of the data field of an IEEE 1394 isochronous packet, immediately followed by zero or more data blocks.

6.1.2 Packet header structure

The packet header consists of the following items as specified in IEEE 1394.

Data_length:	specifies the length of the data field of the isochronous packet in bytes, which is determined as follows: CIP header size + signal data size
Tag:	provides a high level label for the format of data carried by the isochronous packet. 00 ₂ = No CIP header included 01 ₂ = CIP header included as specified in 6.1.3 10 ₂ = Reserved 11 ₂ = Reserved
Channel:	specifies the isochronous channel number for the packet.
Tcode:	specifies the packet format and the type of transaction that shall be performed (fixed at 1010 ₂).
Sy:	application-specific control field.

6.1.3 CIP header structure

The CIP header is placed at the beginning of the data field of an IEEE 1394 isochronous packet. It contains information on the type of the real time data contained in the data field following it. The structure of the CIP header is shown in Figure 3.

The definitions of the fields are given as follows:

EOH_n (End of CIP header):	means the last quadlet of a CIP header. 0 = Another quadlet will follow 1 = The last quadlet of a CIP header
Form_n:	in combination with EOH, shows the additional structure of CHF_n.
CHF_n (CIP header field):	CIP header field of n th quadlet. The additional structure of CHF_n depends on EOH_0, form_0, EOH_1, form_1, ... EOH_n, and form_n.

6.2 Transmission of fixed length source packet

This protocol transfers a stream of source packets from an application on a device to an application on other device(s). A source packet is assumed to have a fixed length, which is defined for each type of data. The data rate can be variable.

A source packet may be split into 1, 2, 4 or 8 data blocks, and zero or more data blocks are contained in an IEEE 1394 isochronous packet. A receiver of the packet shall collect the data blocks in the isochronous packet and combine them to reconstruct the source packet to send to the application.

A model conforming to these requirements is shown in Figure 4.

6.2.1 Two-quadlet CIP header (form_0=0, form_1=0)

This standard defines the two-quadlet CIP header for a fixed length source packet. There are two types for the structure of the two-quadlet CIP header as shown in Figure 5. One is the CIP header with SYT field (Figure 5a), and the other is the CIP header without SYT field (Figure 5b). If a device transmits real time data (identified by FMT) and requires time stamp in the CIP header, it shall use the SYT format.

The definitions of the fields are given as follows.

- SID: Source node ID (node ID of transmitter).
- DBS: Data block size in quadlets.

DBS field is 8 bits because 256 quadlets is the maximum payload size for S100 mode. When 8 bits are all 0, it means 256 quadlets; and 00000001₂ to 11111111₂ means 1 quadlet to 255 quadlets accordingly.

00000000₂ = 256 quadlets
 00000001₂ = 1 quadlet
 00000010₂ = 2 quadlets

 11111111₂ = 255 quadlets

Several data blocks may be put into a bus packet, which is a packet to be transmitted on the bus, if a higher bandwidth is required for S200 and S400 speed.

NOTE S100, S200 and S400 are transmission speeds as defined in IEEE 1394.

- FN: Fraction number.
 The number of data blocks into which a source packet is divided. The allowable numbers and allocated FN codes are listed in Table 1.
- QPC: Quadlet padding count (0 quadlet to 7 quadlets).
 The number of dummy quadlets padded at the end of every source packet to enable division into equally sized data blocks. The value of all bits in padding quadlets is always zero.
 The number of padding quadlets shall be less than the number of data blocks into which every source packet is divided, as encoded by FN.
 The number of padding quadlets shall be less than the size of a single data block, as encoded by DBS. Consequently, a data block shall never consist entirely of padding quadlets.
- SPH: Source packet header.

The value one indicates that the source packet has a source packet header. The format of the source packet header is shown in Figure 6. Code allocation of the time stamp field is shown in Table 4. When a time stamp is indicated, the time stamp field shall be encoded as the lower 25 bits of the IEEE 1394 CYCLE_TIME register. Other bits are reserved for future extension and shall be zeros.

- Rsv: Reserved for future extension and shall be zeros.
- DBC: Continuity counter of data blocks for detecting a loss of data blocks
The value refers to the first data block following the CIP header in the bus packet. The lower FN bits contain the sequence number of the data block within its source packet. The remaining 8-FN bits form the sequence number of the source packet. The first data block of any source packet always has a sequence number with value zero. If FN is zero, then all 8 bits of DBC are used to represent a source packet sequence number. See also Table 2.
- FMT: Format ID.
The code allocation is illustrated in Table 3.
If FMT is 111111₂ (no data), the fields for DBS, FN, QPC, SPH and DBC are ignored and no data blocks shall be transmitted. For other values of FMT, data is present and the most significant bit of the FMT field indicates whether or not a time stamp in SYT format is present. When the most significant bit of FMT is zero, the FMT-dependent field contains a time stamp in the format specified by SYT. Otherwise the contents of the FMT-dependent field are unspecified. See also Figure 5 and Table 3.
- FDF: Format dependent field.
This field is defined for each FMT.
- SYT: The code allocation of the SYT field is shown in Table 5. When a time stamp is indicated by the most significant bit of the FMT field, the SYT field shall be encoded as the lower 16 bits of the IEEE 1394 CYCLE_TIME register.

6.2.2 Isochronous packet transmission

Active transmitters shall send an isochronous packet in every cycle. If no data block is available, an empty packet shall be sent. An empty packet shall always contain a two-quadlet CIP header. The DBC field of an empty packet shall show the count for the first data block contained in the first non-empty IEEE 1394 isochronous packet for the same transmission stream following this empty packet. The other fields shall match the fields of the CIP header of non-empty packets on the same transmission stream.

7 Isochronous data flow management

7.1 General

To start and stop isochronous data flows on the bus and to control their attributes, the concept of plugs and plug control registers is used. Plug control registers are special purpose CSR registers.

NOTE Plugs do not physically exist on an AV device. Only the concept of a plug is used to establish an analogy with existing AV devices where each flow of information is routed via a physical plug.

This clause describes the contents of the plug control registers and how they may be modified. The set of procedures that use the plug control registers to control an isochronous data flow are called connection management procedures (CMP). The CMP that shall be used by AV devices are described in Clause 8.

7.2 Plugs and plug control registers

An isochronous data flow flows from one transmitting AV device to zero or more receiving AV devices by sending isochronous packets on one isochronous channel of the IEEE 1394 bus. An isochronous channel shall carry not more than one isochronous data flow and each isochronous data flow shall be carried on one isochronous channel.

Each isochronous data flow is transmitted to an isochronous channel through one output plug on the transmitting AV device and it is received from that isochronous channel through one input plug on each of the receiving AV devices. Each input and output plug shall not carry more than one isochronous data flow.

The transmission of an isochronous data flow through an output plug is controlled by one output plug control register (oPCR) and one output master plug register (oMPR) located on the transmitting AV device. On each AV device there is only one OUTPUT_MASTER_PLUG register for all output plugs. The OUTPUT_MASTER_PLUG register controls all attributes that are common to all isochronous data flows transmitted by the corresponding AV device. The OUTPUT_PLUG_CONTROL register controls all attributes of the corresponding isochronous data flow that are independent from attributes of other isochronous data flows transmitted by that AV device.

The reception of an isochronous data flow through an input plug is controlled by one input plug control register (iPCR) and one input master plug register (iMPR) located on the receiving AV device. On each AV device there is only one INPUT_MASTER_PLUG register for all input plugs. The INPUT_MASTER_PLUG register controls all attributes that are common to all isochronous data flows received by the corresponding AV device. The INPUT_PLUG_CONTROL register controls all attributes of the corresponding isochronous data flow that are independent from attributes of other isochronous data flows received by that AV device.

An isochronous data flow can be controlled by any device connected to the IEEE 1394 bus by modifying the corresponding plug control registers. Plug control registers can be modified by means of asynchronous transactions on the IEEE 1394 bus or by internal modifications if the plug control registers are located on the controlling device.

The usage of plugs and plug control registers is illustrated in Figure 7.

Let #iPCR and #oPCR denote the number of isochronous data flows that can be simultaneously received and transmitted respectively by an AV device (such as a multiple viewing device or a multiple tuner device). Both #iPCR and #oPCR shall be constants in the range [0 to 31] that are AV device-dependent.

Each AV device shall implement #oPCR output plugs, each controlled by one separate OUTPUT_PLUG_CONTROL register, and #iPCR input plugs, each controlled by one separate INPUT_PLUG_CONTROL register. For AV devices implementing INPUT_PLUG_CONTROL registers, a single INPUT_PLUG_CONTROL register within that AV device shall be denoted as INPUT_PLUG_CONTROL[*i*], where *i* is in the range [0 to #iPCR-1]. The INPUT_MASTER_PLUG register is optional when #iPCR = 0 and required otherwise. For AV devices implementing OUTPUT_PLUG_CONTROL registers, a single OUTPUT_PLUG_CONTROL register within that AV device shall be denoted as OUTPUT_PLUG_CONTROL[*i*], where *i* is in the range [0 to #oPCR-1]. The OUTPUT_MASTER_PLUG register is optional if #oPCR = 0 and required otherwise.

The mapping between an INPUT_PLUG_CONTROL register and an isochronous data flow in a receiving AV device, and the mapping between an OUTPUT_PLUG_CONTROL register and an isochronous data flow in a transmitting AV device, are AV device-dependent.

7.3 Connections

To transport isochronous data between two AV devices on the IEEE 1394 bus, it is necessary for an application to connect an output plug on the transmitting AV device to an input plug on the receiving AV device using one isochronous channel. The relationship between one input plug, one output plug and one isochronous channel is called a *point-to-point connection*. A point-to-point connection can only be broken by the same application that established it.

It is also possible that an application just starts the transmission or the reception of an isochronous data flow on its own AV device by connecting one of its output or input plugs respectively to an isochronous channel. The relationship between one output plug and one isochronous channel is called a *broadcast-out connection*. The relationship between one input plug and one isochronous channel is called a *broadcast-in connection*. Broadcast-out and broadcast-in connections are collectively called *broadcast connections*. A broadcast connection can be established only by the AV device on which the plug is located but it can be broken by any device. The concept of connections is illustrated in Figure 8.

Only one broadcast-out connection can exist in an output plug and only one broadcast-in connection can exist in an input plug. One broadcast connection and multiple point-to-point connections can exist simultaneously in one plug. This can be achieved by overlaying a connection over existing connections in the same input or output plug. Note that all connections that exist in one plug use the same isochronous channel and transport the same isochronous data flow. Multiple independent applications can create point-to-point connections between the same input and output plug.

7.4 Plug states

A plug can be in four states as described in Figure 9: idle, ready, active and suspended.

A plug is either *on-line* or *off-line*. Only a plug that is on-line is capable of transmitting or receiving an isochronous data flow.

NOTE 1 Being capable does not mean that the plug is actually transmitting or receiving an isochronous data flow.

A plug may be off-line, for example, because it relies on resources that are (temporarily) unpowered or otherwise unavailable.

NOTE 2 The reasons that cause a plug to switch between on- and off-line are internal to the AV device on which the plug is located and do not fall within the scope of this standard.

A plug to which no connections exist is called *unconnected*. A plug to which one or more connections exist is called *connected*. A plug that is connected and on-line is called *active*. Only an active plug shall transmit or receive an isochronous data flow except in the case of a bus reset where the isochronous data flow is resumed immediately after the bus-reset according to the procedures described in 7.10. A plug shall cease transmitting an isochronous data flow within 250 μ s after becoming unconnected via transition **d** shown in Figure 9.

In Figure 9, all possible transitions from one state to another are given. Transitions are atomic and are effected by modifying the corresponding plug control register as described in 7.9.

NOTE 3 In order to ensure that the contents of plug registers are reliable, any intermediate results which may occur during a state transition should not be made available. A technique to achieve this is to disable access to the plug registers (for example by masking relevant interrupt mechanisms) once a state transition is invoked, and to ensure that the state transition is completed as an indivisible process without being interrupted, suspended or modified in any way. Under these conditions, a transition is said to be atomic.

7.5 OUTPUT_MASTER_PLUG register definition

The format of the OUTPUT_MASTER_PLUG register is shown in Figure 10.

The number of output plug fields contains the number of output plugs an AV device implements as defined in 7.2.

The persistent and non-persistent extension fields are defined for future extensions.

The data rate capability is a constant, depending on the AV device concerned, that indicates the maximum speed at which an isochronous data flow can be transmitted by an AV device. The data rate capability is encoded as specified in Table 6.

The broadcast channel base determines the isochronous channel number when a broadcast-out connection is established to an output plug while there exists no point-to-point connection to that plug. The relationship between the broadcast channel base and the channel number is expressed in the following formula:

$B < 63$: $N[i] = (B+i) \bmod 63$

$B = 63$: $N[i] = 63$

where

B is the value of broadcast channel base field;

$N[i]$ is the isochronous channel number for broadcast connection using OUTPUT_PLUG_CONTROL[i].

In this way, the output plugs on an AV device use consecutive channel numbers if the broadcast channel base is not equal to 63 and they all use channel 63 if the broadcast channel base equals 63.

7.6 INPUT_MASTER_PLUG register definition

The format of the INPUT_MASTER_PLUG register is shown in Figure 11.

The number of input plugs contains the number of input plugs that an AV device implements, as defined in 7.2.

The persistent and non-persistent extension fields are defined for future extensions.

The data rate capability is a constant, depending on the AV device concerned, that indicates the maximum speed at which an isochronous data flow can be received by an AV device. The data rate capability is encoded as specified in Table 6.

7.7 OUTPUT_PLUG_CONTROL register definition

The format of the OUTPUT_PLUG_CONTROL register is shown in Figure 12.

The on-line bit always indicates whether the corresponding output plug is on-line (value one) or off-line (value zero).

The broadcast connection counter always indicates whether a broadcast-out connection to the output plug exists (value one) or not (value zero). The point-to-point connection counter always indicates the number of point-to-point connections that exist to the output plug.

For a suspended output plug, the channel indicates the channel number that the output plug shall use to transmit the isochronous data flow when it is activated. For an active output plug it indicates the actual channel number that the output plug uses to transmit the isochronous data flow. For an unconnected output plug it has no meaning.

For a suspended output plug, the data rate indicates the bit rate that the output plug shall use to transmit the isochronous packets of an isochronous data flow when it is activated. For an active output plug whose data rate value does not exceed the data rate capability of the OUTPUT_MASTER_PLUG register, it indicates the actual bit rate that the output plug uses to transmit the isochronous packets of an isochronous data flow. An active output plug whose data rate value exceeds the data rate capability of the OUTPUT_MASTER_PLUG register or indicates the value "reserved" (see Table 6) shall not transmit isochronous packets. For an unconnected plug, the data rate value is undefined. The data rate is encoded as an index in Table 6 that gives the corresponding IEEE 1394 bit rate value (see IEEE 1394).

The payload indicates the maximum number of quadlets that the output plug shall transmit in one isochronous packet of an isochronous data flow when it is activated. The value zero corresponds to 1 024 quadlets. The payload does not include the header, the header_CRC and the data_CRC that are required by IEEE 1394 to transmit an isochronous packet in addition to the data itself.