

Integrated circuits — Manufacturing line approval application guideline

The European Standard EN 61943:1999 has the status of a
British Standard

ICS 31.200

National foreword

This British Standard is the English language version of EN 61943:1999. It is identical with IEC 61943:1999. This standard is a harmonized specification within the IEC quality assessment system for electronic components (IECQ). In the IECQ system, this specification is numbered QC 211001.

The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors, which has the responsibility to:

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Summary of pages

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English version

**Integrated circuits - Manufacturing line approval application guideline
(IEC 61943:1999)**

Circuits intégrés - Guide d'application
pour l'agrément des lignes de fabrication
(CEI 61943:1999)

Integrierte Schaltkreise
Anwendungsleitfaden für die
Anerkennung von Fertigungslinien
(IEC 61943:1999)

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Foreword

The text of document 47A/533/FDIS, future edition 1 of IEC 61943, prepared by SC 47A, Integrated circuits, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61943 on 1999-08-01.

The following dates were fixed:

- latest date by which the EN has to be implemented
at national level by publication of an identical
national standard or by endorsement (dop) 2000-05-01
- latest date by which the national standards conflicting
with the EN have to be withdrawn (dow) 2002-08-01

Annexes designated "normative" are part of the body of the standard.
In this standard, annex ZA is normative.
Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 61943:1999 was approved by CENELEC as a European Standard without any modification.

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INTEGRATED CIRCUITS – MANUFACTURING LINE APPROVAL APPLICATION GUIDELINE

1 General

1.1 Scope and object

This International Standard defines how to apply the principles and requirements given in IEC 61739 to monolithic integrated circuits. The standard is applicable to those manufacturers of integrated circuits (ICs) who apply for manufacturing line approval.

The objective of this applicators guideline is to establish consistency in the requirements used by manufacturers and auditors for techniques related to integrated circuit manufacturing.

Each manufacturer may use his own methods for satisfying the requirements of this standard, provided that the required level of control in the manufacturing line is reached.

1.2 Normative reference

The following normative document contains provisions which, through reference in this text, constitute provisions of this International Standard. For dated references, subsequent amendments to, or revisions of, this publication do not apply. However, parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the normative document indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 61739:1996, *Integrated circuits – Procedures for manufacturing line approval and quality management*

2 Definitions

For the purpose of this Guideline the following definitions apply (see 1.4 of IEC 61739):

2.1

demonstration vehicle

normal product or product specifically designed to demonstrate that all critical process parameters are under control and repeatable within the defined technology

2.2

parametric monitor (PM)

structure for measuring electrical parameters

2.3

qualified manufacturer list QML

list used for the procedure associated with manufacturing line approval as defined in IEC 61739

2.4

standard evaluation component (SEC)

structure used to monitor the fabrication process and to serve as a surrogate product for reliability testing and failure rate evaluation. It can be an actual device of the technology under consideration

2.5

task

activity or sequence of activities that form a stage in manufacturing the product

2.6

technological vehicle (TV)

hybrid structure that demonstrates process repeatability and involved characteristics

2.7

technology characterization vehicle (TCV)

structure to study intrinsic failure mechanisms and their distribution

2.8

technology review board (TRB) or equivalent organization

primary organization for the manufacturing line or task. A TRB will consist of representatives of all functions described in total quality management (TQM) Plan, such as marketing, sales, design, technology development, fabrication, testing and quality assurance as applicable

3 Principles for qualified manufacturer list (QML) approval

QML listed manufacturers shall be able to produce products utilizing an approved manufacturing line without the need for extensive qualification testing and end-of-manufacturing quality conformance inspections on each product.

The primary organization for control of the qualified manufacturing line shall be the TRB or equivalent organization.

The qualifying manufacturer shall ensure and document that any tasks to be performed by a subcontractor meet the requirements of IEC 61739.

As the technology matures and reliability and quality data are accumulated, the manufacturer, through the total quality management (TQM) plan and technology review board (TRB) may modify, substitute or delete tests and/or screens. The national supervising inspectorate (NSI) shall be notified of such actions through the status report.

3.1 Identification and definition of tasks

This guideline identifies six tasks with interfaces which detail the specific requirements for the design and manufacturing of ICs.

3.1.1 Process design (see clause 4)

This is the design of the semiconductor process including modification and publication of the process parameters and related process design rules in the form of written text and/or computer files.

3.1.2 IC design (see clause 5)

This is the design of integrated circuits in accordance with customer requests as defined by product or other specifications.

3.1.3 Wafer fabrication (see clause 6)

This is the physical realization of ICs on substrates under TQM.

3.1.4 Process characterization (see clause 7)

Process characterization is the extraction of all the information required to confirm the process design.

3.1.5 Assembly and packaging (see clause 8)

This includes a series of operations from receipt of wafers or chips to supply of packaged products.

3.1.6 Test (see clause 9)

This is verification of conformance to specifications.

3.2 Product specifications

For standard or catalog products, manufacturers shall publish specifications stating what processes are employed. They shall also maintain a register of products with their NSI. Such specifications may be any registered IEC detail specification (DS) or any published manufacturer's data sheet.

A custom IC specification may be published only upon agreement between the supplier and customer.

4 Process design (task 1)

4.1 Field of application

The system of process design quality management shall be fully documented. The process design center shall be responsible for the management of quality and shall have established the necessary organization, including a TRB and tools for this purpose. The supplier shall be able to so demonstrate to the satisfaction of the NSI with objective results.

4.2 Description of activities

The manufacturer shall define and document procedures and activities of the process design center, including design rules and outputs, archiving, verification and validation.

4.3 Interfaces and subcontracting procedures

4.3.1 Customer interfaces

Customer interface requirements and procedures shall be documented.

4.3.2 Subcontracting

Subcontracting of any work shall comply with the requirements of the QML.

4.3.3 Mask making or equivalent activity (if applicable)

All mask makers approved by the process design center shall be identified.

4.3.4 Test laboratories

Where external test laboratories are employed, their identification, scope and limits of capability and qualifications shall be documented.

4.3.5 Wafer-fabricant

The process design center shall list all wafer-fabricants for which they design processes, together with identification of the processes for each of these.

The qualifications of each wafer-fabricant shall be documented together with the procedures, specifications and interface requirements. This shall include identification of the relevant design rules, test vehicles, process characterization and control methods and results, critical dimensions, and process transfer specifications.

4.3.6 Assembly/packaging

All requirements for assembly/packaging shall be detailed in the design rules.

4.4 Procedures for design and verification of models

The procedures for creation, verification and validation, as well as the integration of design rules and library elements, shall be stated for each tool qualified.

4.4.1 Creation

Descriptions of the processes for creation and installation of new library elements (and blocks, cells, arrays, etc.) shall be documented in the applicable design manuals for library, layout, and circuit design.

4.4.2 Verification

The procedures employed for verification and validation of characteristics and application rules for library elements shall be specified.

4.5 Procedures for integration and validation

4.5.1 Integration

The methodology used to verify, validate and integrate a new library element shall be specified. It identifies the tools, the operating mode and the quality assurance procedures related to the described process.