

Integrated circuits — Memory devices pin configurations

The European Standard EN 61964:1999 has the status of a
British Standard

ICS 31.200

National foreword

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The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors, which has the responsibility to:

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Summary of pages

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English version

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(IEC 61964:1999)**

Circuits intégrés - Configuration
de broches de mémoires
(CEI 61964:1999)

Integrierte Schaltungen
Kontaktanordnungen für
Speicherbauelemente
(IEC 61964:1999)

This European Standard was approved by CENELEC on 1999-05-01. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Foreword

The text of document 47A/535/FDIS, future edition 1 of IEC 61964, prepared by SC 47A, Integrated circuits, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61964 on 1999-05-01.

The following dates were fixed:

- latest date by which the EN has to be implemented
at national level by publication of an identical
national standard or by endorsement (dop) 2000-02-01
- latest date by which the national standards conflicting
with the EN have to be withdrawn (dow) 2002-05-01

Annexes designated "normative" are part of the body of the standard.
Annexes designated "informative" are given for information only.
In this standard, annex ZA is normative and annex A is informative.
Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 61964:1999 was approved by CENELEC as a European Standard without any modification.

In the official version, for annex A, Bibliography, the following note has to be added for the standard indicated:

IEC 60749 NOTE: Harmonized as EN 60749:1999 (not modified).

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INTRODUCTION

The registration and standardization of the mechanical outlines for integrated memory circuit devices is an ongoing activity covered in the IEC 60191 series.

Due to the fact that the same mechanical package can house different types of memory devices, and because the same memory device can be incorporated into different types of mechanical packages, the number of such configurations has to be limited to minimum required by the electronics industry. Registration and standardization of such electrical pinout configurations also helps to establish and maintain compatibility of devices from different vendors and in different applications.

Owing to the nature of the integrated memory circuits business, in which there is ongoing potential for the development of new density generations and new electrical functions, this International Standard has to take the form of an open Standard. In the present context, this signifies that the new items can be added at any time to any of its clauses. New subclauses may be created as new types of memory devices come into usage in the industry.

Additions, deletions and any changes will be subject to agreement in order to become effective for publication.

INTEGRATED CIRCUITS – MEMORY DEVICES PIN CONFIGURATIONS

1 Scope

This International Standard applies to pinout package configurations of solid state integrated circuit memory devices. The purpose of this standard is to establish a registration procedure for such configurations.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this International Standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 60191-2:1996, *Mechanical standardization of semiconductor devices – Part 2: Dimensions*

IEC 60748-1:1984, *Semiconductor devices – Integrated circuits – Part 1: General*

3 Terms and definitions

For the purpose of this International Standard, the following terms and definitions apply. This contains definitions of a number of terms that are needed for a clear understanding of the standard.

Most of these terms have been developed within the semiconductor memory industry. They are given for quick reference and are not intended to supersede any existing definitions in previous IEC publications such as IEC 60748-1.

The following pin names and functional descriptions apply uniformly to all devices covered by this standard. Where a pin has a dual function, and those functions are invoked at substantially different times, the names and symbols for these functions are separated by a slash (/) (e.g. $V_{PP}/G\backslash$). Where a pin has multiple functions which are used simultaneously, the slash is omitted (e.g. DQ). Where multiple pins have a similar function, a number symbolised as (n) is appended to the symbol. Where the pin function has an inverted logic sense, that is, the function is true or invoked for a low signal, the reverse slash (\) is appended to the symbol. Where alternative functions are permitted by this standard, these authorized functions are listed and separated by commas. Where common usage has resulted in two terms being used interchangeably, both are listed but the less favoured term is enclosed in parentheses.

3.1 Device pin names

3.1.1 A(n), ADDRESS INPUTS

Those inputs that select (address) a particular cell or set of cells within a memory array for storage of data or for presentation of the stored data on the device outputs.

The integer (n) serves to differentiate the address inputs one from another.

3.1.2 AL, AL\, ADDRESS LATCH ENABLE

An input that, when true, allows the input address to be entered into a register, and when false, causes the address state previously entered to be latched.

3.1.3 BA, BANK ADDRESS

In a RAM that has multiple banks in its architecture, the BANK ADDRESS is used, at any instant of time, to select any one of the available banks.

3.1.4 CA, COLUMN ADDRESS

In an address multiplexed DRAM (dynamic RAM), the address field that is captured by the COLUMN ENABLE clock CAS\.

3.1.5 CAS, CAS\, COLUMN ENABLE

An enable signal that on some dynamic RAMs actuates only the column-oriented internal circuits and the data input/output circuits. Most devices normally require the RAS\ signal to be present for the CAS\ signal to be effective. In some newer designs, however, special sequences of the RAS\ and CAS\ signals are used to actuate certain special device control functions.

3.1.6 CK, CK\, INPUT AND OUTPUT CLOCK

An input that controls the activation of both input and output circuitry, normally storage registers or latches.

3.1.7 CKE, CLOCK ENABLE

In certain synchronous memory devices, a logic level input that enables the clock input and allows it to fulfill its defined function.

3.1.8 D(n), DATA INPUT

Those inputs whose state represents the value of data that is to be written into the selected address on a write cycle of an alterable memory device.

3.1.9 DQ(n), DATA INPUT/OUTPUT

The pins that serve as data output(s) when in the read mode and as data input(s) when in the write mode. When the device is not selected or enabled, the output(s) are in a floating state.