

Integrated circuits — Measurement of electromagnetic emissions, 150 kHz to 1 GHz —

Part 6: Measurement of conducted emissions — Magnetic probe method

ICS 31.200

National foreword

This British Standard is the UK implementation of EN 61967-6:2002+A1:2008. It is identical with IEC 61967-6:2002, incorporating amendment 1:2008. It supersedes BS EN 61967-6:2002 which is withdrawn.

The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors.

A list of organizations represented on this committee can be obtained on request to its secretary.

This publication does not purport to include all the necessary provisions of a contract. Users are responsible for its correct application.

Compliance with a British Standard cannot confer immunity from legal obligations.

This British Standard was published under the authority of the Standards Policy and Strategy Committee on 24 October 2002

© BSI 2010

ISBN 978 0 580 72986 7

Amendments/corrigenda issued since publication

Date	Comments
30 September 2008	Implementation of IEC amendment 1:2008 with CENELEC endorsement A1:2008. Annex E added and Bibliography amended
31 December 2010	Implementation of IEC corrigendum August 2010: Corrections to Figure 3 and A.4

**Integrated circuits -
Measurement of electromagnetic emissions,
150 kHz to 1 GHz
Part 6: Measurement of conducted emissions -
Magnetic probe method
(IEC 61967-6:2002)**

Circuits intégrés -
Mesure des émissions
électromagnétiques, 150 kHz à 1 GHz
Partie 6: Mesure des émissions
conduites -
Méthode de la sonde magnétique
(CEI 61967-6:2002)

Integrierte Schaltungen -
Messung von elektromagnetischen
Ausstrahlungen im Frequenzbereich
von 150 kHz bis 1 GHz
Teil 6: Messung der leitungsgeführten
Ausstrahlungen -
Magnetsondenverfahren
(IEC 61967-6:2002)

This European Standard was approved by CENELEC on 2002-09-01. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Czech Republic, Denmark, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Luxembourg, Malta, Netherlands, Norway, Portugal, Slovakia, Spain, Sweden, Switzerland and United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Foreword

The text of document 47A/645/FDIS, future edition 1 of IEC 61967-6, prepared by SC 47A, Integrated circuits, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61967-6 on 2002-09-01.

This European Standard should be read in conjunction with EN 61967-1:2002.

The following dates were fixed:

- latest date by which the EN has to be implemented
at national level by publication of an identical
national standard or by endorsement (dop) 2003-06-01
- latest date by which the national standards conflicting
with the EN have to be withdrawn (dow) 2005-09-01

Annexes designated "normative" are part of the body of the standard.

Annexes designated "informative" are given for information only.

In this standard, annexes A and ZA are normative and annexes B, C and D are informative.

Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 61967-6:2002 was approved by CENELEC as a European Standard without any modification.

Foreword to amendment A1

The text of document 47A/781/FDIS, future amendment 1 to IEC 61967-6:2002, prepared by SC 47A, Integrated circuits, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as amendment A1 to EN 61967-6:2002 on 2008-04-01.

The following dates were fixed:

- latest date by which the amendment has to be
implemented at national level by publication of
an identical national standard or by endorsement (dop) 2009-01-01
- latest date by which the national standards conflicting
with the amendment have to be withdrawn (dow) 2011-04-01

Endorsement notice

The text of amendment 1:2008 to the International Standard IEC 61967-6:2002 was approved by CENELEC as an amendment to the European Standard without any modification.

CONTENTS

1	Scope	5
2	Normative references	5
3	Definitions	5
4	General	5
4.1	Measurement philosophy	5
4.2	Measurement principle	6
5	Test conditions	6
5.1	General	6
5.2	Frequency range	6
6	Test equipment	6
6.1	General	6
6.2	Magnetic probe	6
6.3	Probe spacing fixture and placement	6
7	Test set-up	9
7.1	General	9
7.2	Probe calibration	9
7.3	Modifications to standardized IC test board	9
7.3.1	Layer arrangement	9
7.3.2	Layer thickness	9
7.3.3	Decoupling capacitors	9
7.3.4	I/O pin loading	10
8	Test procedure	14
8.1	General	14
8.2	Test technique	14
9	Test report	14
9.1	General	14
9.2	Documentation	14
	Annex A (normative) Probe calibration procedure – Microstrip line method	16
	Annex B (informative) Measurement principle and calibration factor	19
	Annex C (informative) Spatial resolution of magnetic probe	23
	Annex D (informative) Angle pattern of probe placement	24
	Annex E (informative) Advanced magnetic probe	25
	Annex ZA (normative) Normative references to international publications with their corresponding European publications	43
	Bibliography	42

Figure 1 – Magnetic probe	7
Figure 2 – Magnetic probe 1 st and 3 rd layers	7
Figure 3 – Magnetic probe 2 nd layer	8
Figure 4 – Magnetic probe – layer construction	8
Figure 5 – Standardized IC test board (sectional view 1)	10
Figure 6 – Standardized IC test board (sectional view 2 – measurement line)	10
Figure 7 – Power line pattern on the standardized IC test board – Bottom layer	11
Figure 8 – I/O signal line pattern on the standardized IC test board – Bottom layer	12
Figure 9 – Multi-power lines on the standardized IC test board – Bottom layer	12
Figure 10 – Measurement set-up	13
Figure 11 – Measurement circuit schematic	13
Figure 12 – Transfer constant for current calculation as a function of insulator thickness of microstrip board	15
Figure A.1 – Cross-sectional view of a microstrip line for calibration	16
Figure A.2 – Measurement set-up for probe calibration	18
Figure B.1 – Cross-sectional view of a microstrip line	19
Figure B.2 – Measurement of magnetic probe output	21
Figure B.3 – Example of calibration factor for the magnetic probe specified in figures 1, 2, 3 and 4	22
Figure C.1 – Diagram for measuring a magnetic field distribution	23
Figure C.2 – Magnetic field distribution across the microstrip line (800 MHz)	23
Figure D.1 – Diagram for measuring an angle pattern of probe placement	24
Figure D.2 – Probe output to angle φ	24

INTEGRATED CIRCUITS – MEASUREMENT OF ELECTROMAGNETIC EMISSIONS, 150 kHz TO 1 GHz –

Part 6: Measurement of conducted emissions – Magnetic probe method

1 Scope

This part of the IEC 61967 specifies a method for evaluating RF currents on the pins of an integrated circuit (IC) by means of non-contact current measurement using a miniature magnetic probe. This method is capable of measuring the RF currents generated by the IC over a frequency range of 0,15 MHz to 1 000 MHz. This method is applicable to the measurement of a single IC or a chip set of ICs on the standardized test board for characterization and comparison purposes. It is also usable to evaluate the electromagnetic characteristics of an IC or group of ICs on an actual application PCB for emission reduction purposes. This method is called the "magnetic probe method".

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61967-1, *Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part 1: General conditions and definitions*

IEC 61967-4, *Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part 4: Measurement of conducted emissions – 1 Ω /150 Ω direct coupling method*³

3 Definitions

For the purposes of this part of IEC 61967 the definitions found in IEC 61967-1 apply.

4 General

4.1 Measurement philosophy

The emissions radiated from a PCB are, in part, caused by RF current generated by the onboard IC which drives PCB traces, PCB ground and supply planes, and cables connected to the PCB. All of these can act as RF antennas to radiate the emissions. The emission level is proportional to the driving RF current, and is also affected significantly by PCB design, radiation effectiveness of the pseudo-antennas, and noise coupling path coefficients from the IC to the pseudo-antennas.

For this emission mechanism, the driving force of the IC can be a significant parameter for both users and manufacturers to estimate and predict the electromagnetic characteristics of a PCB, module, or system. A measure of the emission driving force can be obtained by measuring the RF currents generated by the IC under test. Thus, the measured RF noise current can be regarded as an indicator of the undesirable electromagnetic emission driving force generated by the IC.

³ To be published.

4.2 Measurement principle

Using this test method, the RF current on the power supply pins and I/O pins of an IC under test can be measured using a miniature triplate-structured magnetic probe. This probe measures the magnetic field at a specified height over a power supply or I/O strip conductor on the standardized test board in a controlled manner. The RF current is calculated from the measured magnetic field using the formula described in 8.2. With accurate mechanical placement of the magnetic probe, this method provides a high degree of repeatability. In addition, the frequency range of this method can be extended subject to the limitations described in 5.2. Higher frequencies can be obtained without a substantial influence on accuracy. The estimation of the RF current over the power supply or I/O strip conductor is an easy and handy way of characterizing and comparing the ICs.

5 Test conditions

5.1 General

General test conditions are described in IEC 61967-1.

5.2 Frequency range

The effective frequency range of this measurement method is 0,15 MHz to 1 000 MHz. The maximum frequency can be extended, if desired, subject to the limitations of the test set-up. The upper limit of the frequency range is directly related to high frequency characteristics of the magnetic probe and its distance from the line under test as described in annex B. At a low frequency region of 0,15 MHz to 10 MHz, however, it may be advisable to use a low noise pre-amplifier to improve dynamic range of the measurement.

6 Test equipment

6.1 General

For general information on test equipment see IEC 61967-1.

6.2 Magnetic probe

The magnetic probe shall be a triplate-structured strip line composed of a three-layer PCB. Recommended probe construction details are shown in figures 1, 2, 3 and 4.

An SMA connector is attached at the edge of the PCB opposite to the rectangular loop portion of the probe as shown in the figures. Attachment pads for the SMA connector are on layers 1 and 3, which are connected to each other through four vias. The strip conductor pattern is on layer 2, which is connected to the centre pin of the SMA connector.

6.3 Probe spacing fixture and placement

The probe output voltage depends on the distance between the probe tip and the strip conductor under measurement. This makes it very critical to maintain a 1 mm space between the strip conductor and the magnetic probe tip during this measurement. Therefore, a probe spacing fixture shall be used to maintain $1,0 \text{ mm} \pm 0,1 \text{ mm}$ spacing between the bottom of the rectangular loop portion of the probe and strip line on the IC test board, or the entire probe can be molded into a piece of fixing block which houses the probe so as to maintain the specified space precisely as shown in figure 10.

In addition, the probe output voltage depends on probe placement angle (φ) to direction of microstrip line under measurement. According to an experimental measurement on angle patterns of probe directional placement, the angle shall be less than 15° for amplitude error to be less than -2 dB. See annex D for details.

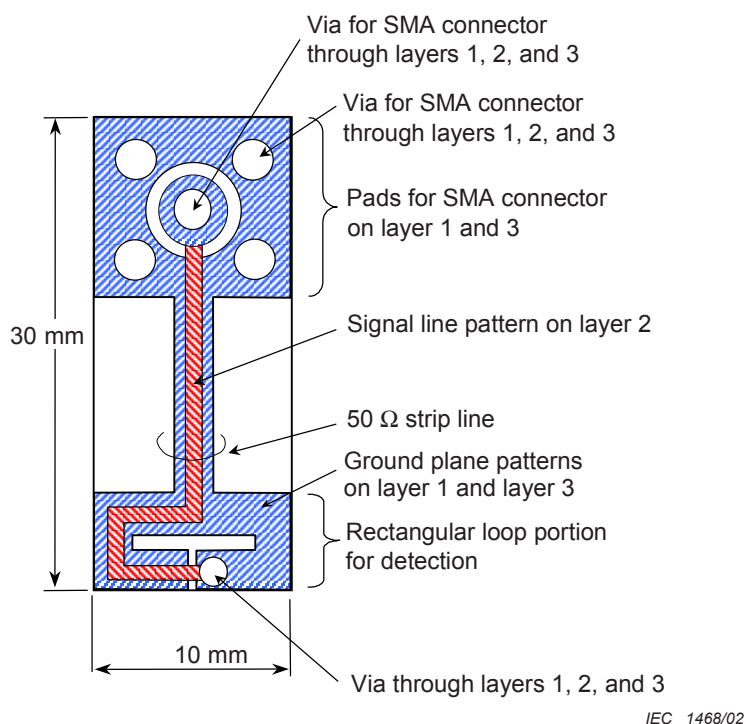


Figure 1 – Magnetic probe

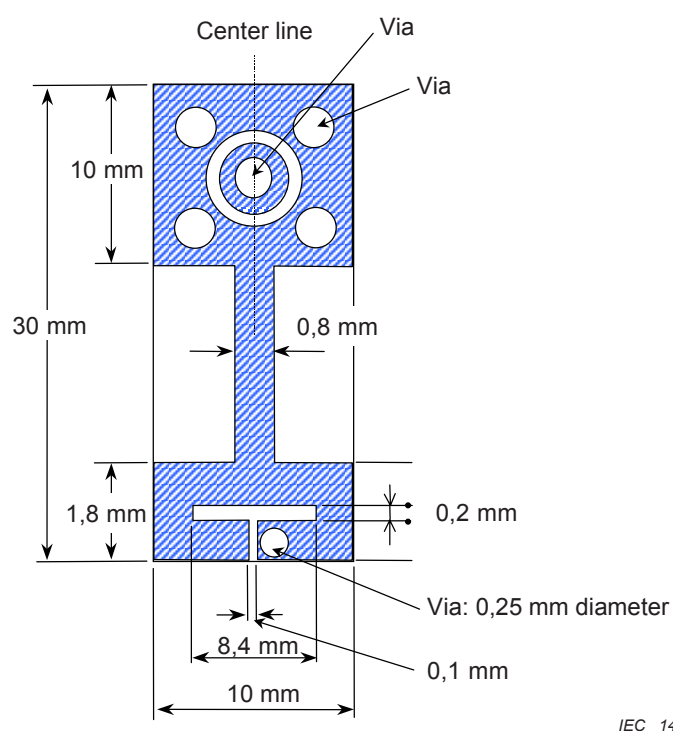


Figure 2 – Magnetic probe – First and third layers

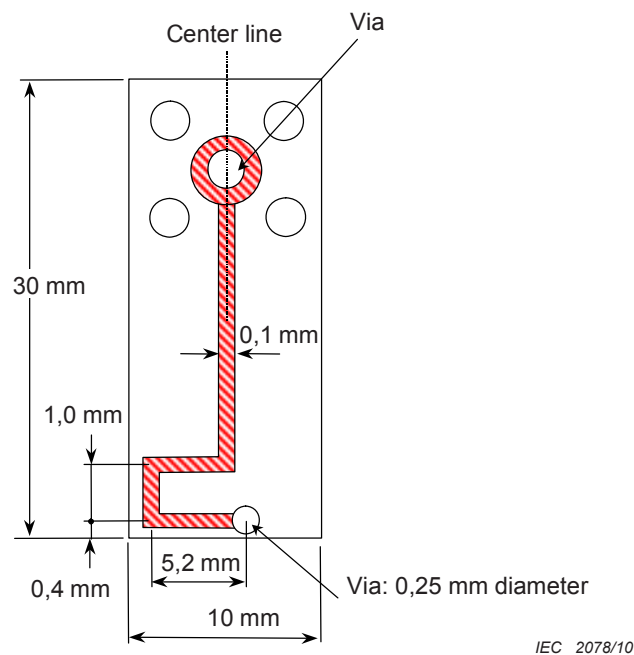


Figure 3 – Magnetic probe – Second layer

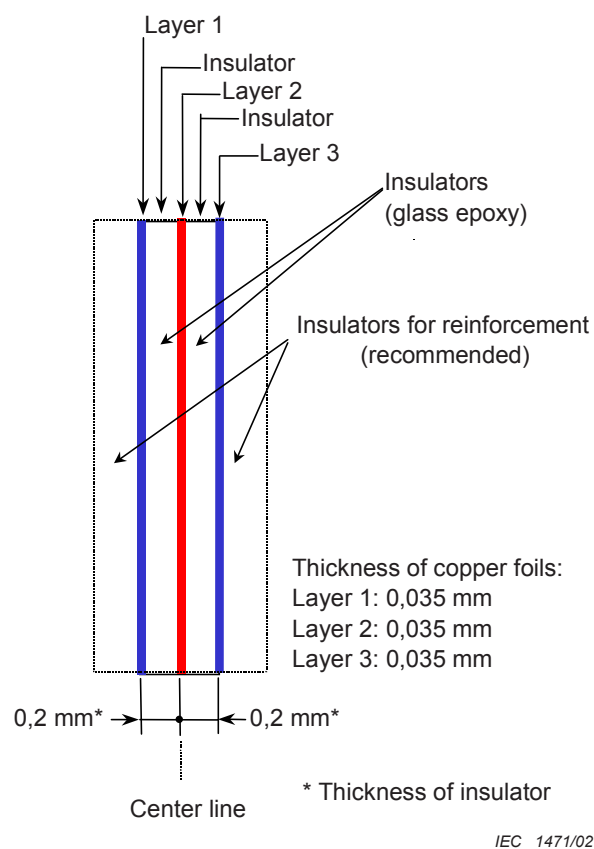


Figure 4 – Magnetic probe – Layer construction

7 Test set-up

7.1 General

General test set-up requirements are described in IEC 61967-1.

The measurement set-up and circuit schematic of the magnetic probe measurement method are shown in figures 10 and 11, respectively.

7.2 Probe calibration

The magnetic probe used shall be calibrated to obtain accurate correlation between the measured magnetic field intensity and the estimated RF current. The probe calibration shall be in accordance with the method described in annex A (microstrip line method).

7.3 Modifications to standardized IC test board

The standardized IC test board described in IEC 61967-1 shall be used. However, it shall be adapted as shown in figures 5, 6, 7, 8, and 9.

7.3.1 Layer arrangement

The IC test board shall have a minimum of four layers. It is recommended to use a four-layer IC test board as shown in figures 5 and 6. If necessary, additional layers may be inserted between the top layer and the microstrip ground layer to accommodate additional signal and/or power routing. The construction of the IC test board shall be as specified in IEC 61967-1, except as noted below in the case of n layers in general.

- 1) Top layer (layer 1): The IC under test shall be put on layer 1. See IEC 61967-1.
- 2) Layer next to the bottom layer (layer $n-1$): A ground plane area shall be formed on layer $n-1$ to provide a reference for the microstrip structures on the bottom layer. The ground plane can cover the entire layer or can be limited to the area under the microstrip structures as shown in the dotted line area of figures 7 and 8. This ground plane area shall have a minimum width of 11 mm and a minimum length of 14 mm.
- 3) Bottom layer (layer n): The microstrip conductor lines for measurement and peripheral ground planes shall be on layer n . The microstrip conductor lines shall be in accordance with figures 7 and 8 for power lines and I/O lines, respectively. The width of the strip conductor line shall be 1,0 mm at maximum to achieve a high spatial resolution. See annex C for details. The length of the microstrip conductor lines should be between 14 mm and 25 mm in length to avoid standing waves.

7.3.2 Layer thickness

The PCB insulator thickness of 0,6 mm between layer $n-1$ and layer n is strongly recommended. The coplanar gap between the measurement line and coplanar ground planes shall be at least 2,0 mm and shall be at least three times the insulator thickness.

7.3.3 Decoupling capacitors

Decoupling capacitors (C1, C2) shall be used between the power supply lines and ground planes on the test board as shown in figure 11. The capacitor (C2) shall be placed as close as possible to the measurement area of the power supply line to provide low RF impedance. The distance between C2 and the via to the V_{DD} land shall be no more than 25 mm as shown in figure 7. The capacitor (C1) shall be placed between the IC V_{DD} land and the IC ground as shown in figure 9.

7.3.4 I/O pin loading

This measurement can be used to measure the RF current of a single I/O pin. The I/O pin current shall be measured pin by pin. The layout of the pin loading shall be in accordance with figures 8 and 9. This pin should be loaded with an impedance matching network with a resistance of $150\ \Omega$ as shown in figure 11. The impedance matching network should be loaded by a $50\ \Omega$ resistor (R3) or a $50\ \Omega$ input impedance of normal measurement equipment (receiver).

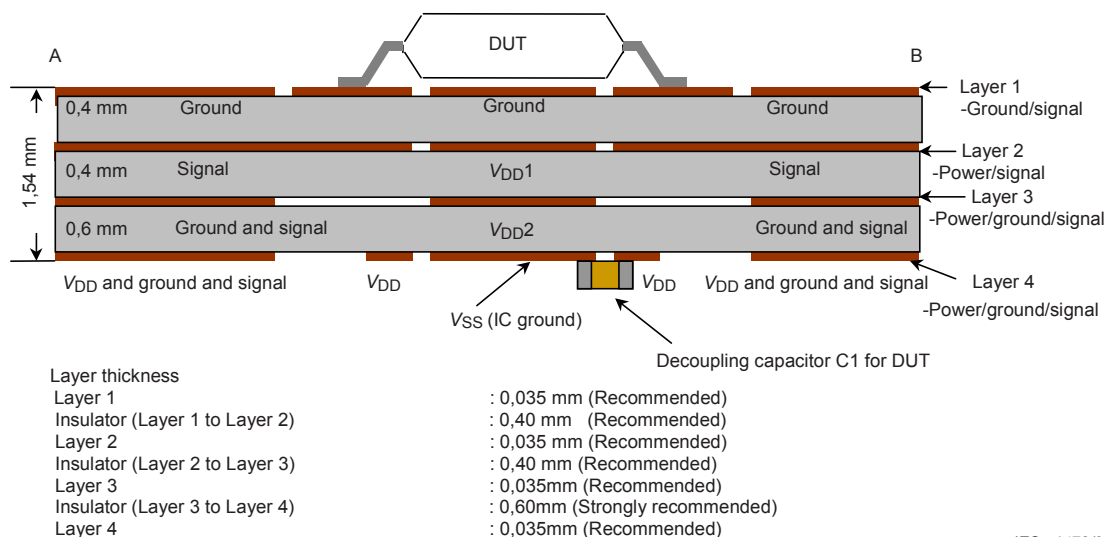


Figure 5 – Standardized IC test board – Sectional view 1

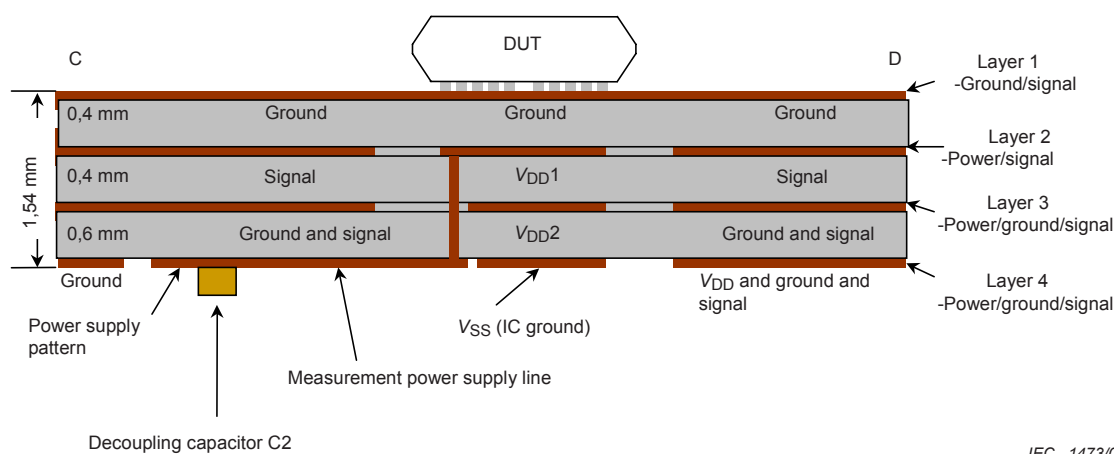
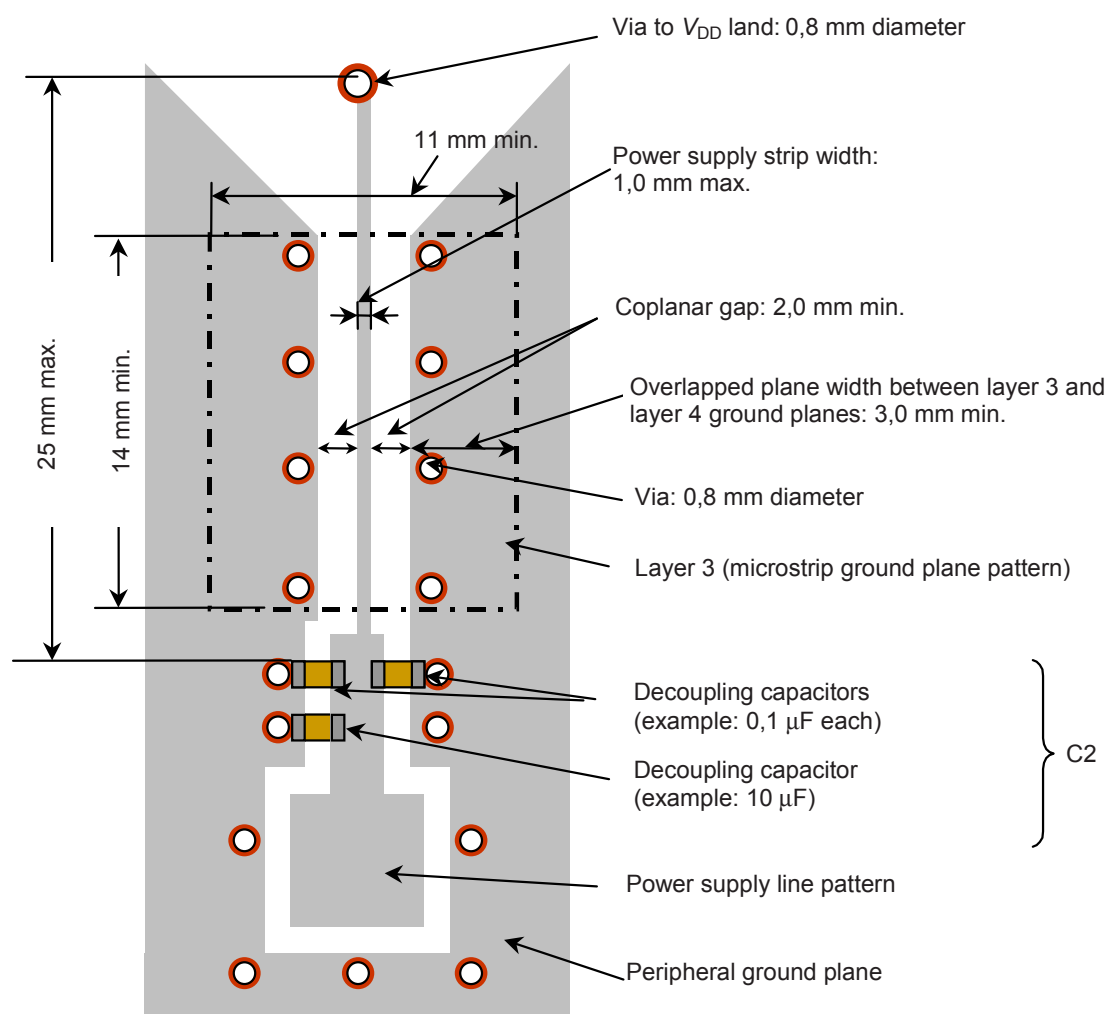
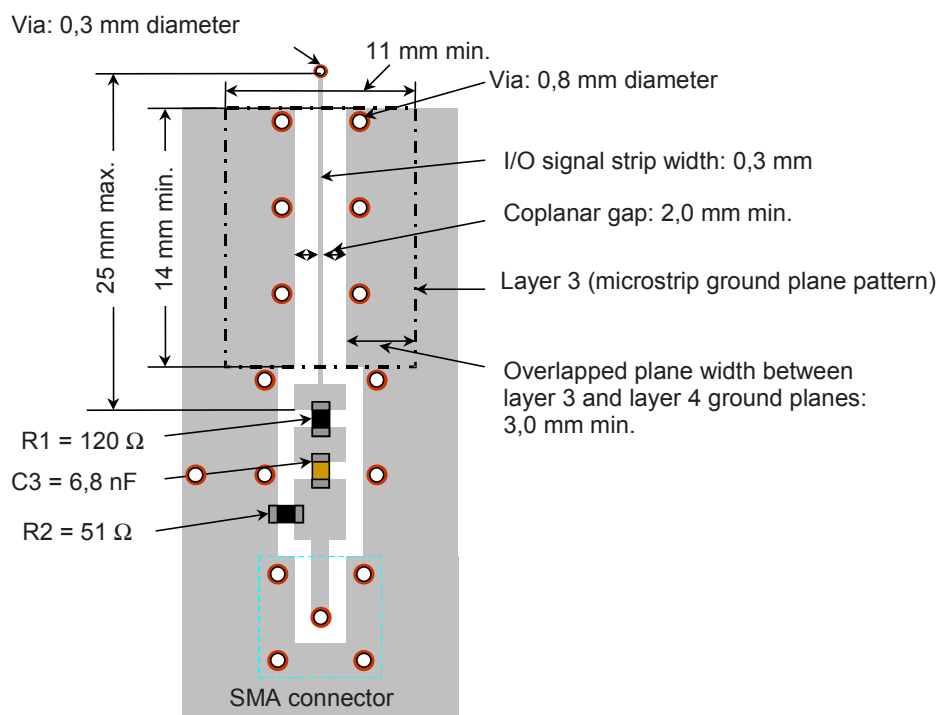


Figure 6 – Standardized IC test board – Sectional view 2 – Measurement line



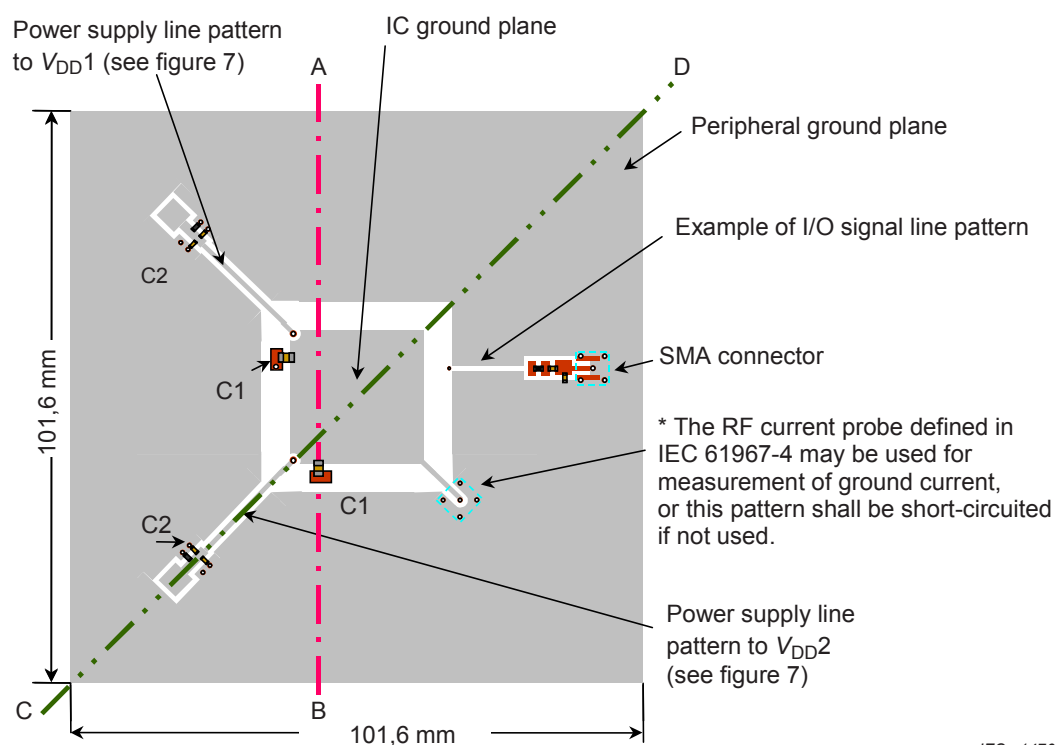
IEC 1474/02

Figure 7 – Power line pattern on the standardized IC test board – Bottom layer



IEC 1475/02

Figure 8 – I/O signal line pattern on the standardized IC test board – Bottom layer



IEC 1476/02

Figure 9 – Multi-power lines on the standardized IC test board – Bottom layer