



BSI Standards Publication

# Low-voltage switchgear and controlgear — Controller-device interfaces (CDIs)

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Part 2: Actuator sensor interface (AS-i)

## National foreword

This British Standard is the UK implementation of EN 62026-2:2013+A1:2019. It is derived from IEC 62026-2:2008, incorporating amendment 1:2019. It supersedes BS EN 62026-2:2013, which will be withdrawn on 13 December 2022.

The CENELEC common modifications have been implemented at the appropriate places in the text. The start and finish of each common modification is indicated in the text by tags [C] [C].

The start and finish of text introduced or altered by amendment is indicated in the text by tags. Tags indicating changes to IEC text carry the number of the IEC amendment. For example, text altered by IEC amendment 1 is indicated by [A1] [A1].

The UK participation in its preparation was entrusted to Technical Committee PEL/121/1, Low voltage switchgear and controlgear.

A list of organizations represented on this committee can be obtained on request to its secretary.

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| Date            | Text affected                                                           |
|-----------------|-------------------------------------------------------------------------|
| 31 January 2020 | Implementation of IEC amendment 1:2019 with CENELEC endorsement A1:2019 |

English Version

**Low-voltage switchgear and controlgear - Controller-device  
interfaces (CDIs) - Part 2: Actuator sensor interface (AS-i)  
(IEC 62026-2:2008, modified)**

Appareillage à basse tension - Interfaces appareil de  
commande-appareil (CDI) - Partie 2: Interface capteur-  
actionneur (AS-i)  
(CEI 62026-2:2008, modifiée)

Niederspannungsschaltgeräte - Steuerung-Geräte-  
Netzwerke (CDIs) - Teil 2: Aktuator Sensor Interface (AS-i)  
(IEC 62026-2:2008, modifiziert)

This European Standard was approved by CENELEC on 2012-12-03. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the CEN-CENELEC Management Centre or to any CENELEC member.

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European Committee for Electrotechnical Standardization  
Comité Européen de Normalisation Electrotechnique  
Europäisches Komitee für Elektrotechnische Normung

**CEN-CENELEC Management Centre: Rue de la Science 23, B-1040 Brussels**

**European foreword**

This document (EN 62026-2:2013) consists of the text of IEC 62026-2:2008 prepared by IEC/SC 17B "Low-voltage switchgear and controlgear" of IEC/TC 17 "Switchgear and controlgear", together with the common modifications prepared by CLC/TC 17B "Low-voltage switchgear and controlgear".

The following dates are fixed:

- latest date by which this document has to be implemented (dop) 2013-12-03  
at national level by publication of an identical  
national standard or by endorsement
- latest date by which the national standards conflicting (dow) 2015-12-03  
with this document have to be withdrawn

EN 62026-2:2013 replaces EN 50295:1999 with the same technical content, in the intention to cover world-wide requirements for AS-i standard under the same scope.

Clauses, subclauses, notes, tables, figures and annexes which are additional to those in IEC 62026-2:2008 are prefixed "Z".

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC [and/or CEN] shall not be held responsible for identifying any or all such patent rights.

This document has been prepared under a mandate given to CENELEC by the European Commission and the European Free Trade Association, and supports essential requirements of EU Directive(s).

For the relationship with EU Directive 2004/108/EC, see informative Annex ZZ, which is an integral part of this document.

This standard covers the Principle Elements of the Safety Objectives for Electrical Equipment Designed for Use within Certain Voltage Limits (LVD - 2006/95/EC).

**Endorsement notice**

The text of the International Standard IEC 62026-2:2008 was approved by CENELEC as a European Standard with agreed common modifications.

**Foreword to amendment A1**

The text of document 121A/297/FDIS, future IEC 62026-2:2008/A1, prepared by SC 121A "Low-voltage switchgear and controlgear" of IEC/TC 121 "Switchgear and controlgear and their assemblies for low voltage" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 62026-2:2013/A1:2019.

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level by publication of an identical national standard or by endorsement
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**Endorsement notice**

The text of the International Standard IEC 62026-2:2008/A1:2019 was approved by CENELEC as a European Standard without any modification.

## Annex ZA (normative)

### Normative references to international publications with their corresponding European publications

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 When an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: [www.cenelec.eu](http://www.cenelec.eu)

| <u>Publication</u>                   | <u>Year</u>          | <u>Title</u>                                                                                                                  | <u>EN/HD</u>                     | <u>Year</u>          |
|--------------------------------------|----------------------|-------------------------------------------------------------------------------------------------------------------------------|----------------------------------|----------------------|
| CISPR 11                             | 2015                 | Industrial scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement | EN 55011 (modified)              | 2016                 |
| +A1                                  | 2016                 |                                                                                                                               | +A1                              | 2017                 |
| IEC 60068-2-6                        | –                    | Environmental testing - Part 2-6: Tests - Test Fc: Vibration (sinusoidal)                                                     | EN 60068-2-6                     | 2008                 |
| IEC 60068-2-27                       | –                    | Environmental testing – Part 2-7: Tests - Test Ea and guidance: Shock                                                         | EN 60068-2-27                    | 2009                 |
| IEC 60204-1                          | 2016                 | Safety of machinery - Electrical equipment of machines - Part 1: General requirements                                         | EN 60204-1 (modified)            | 2018                 |
| IEC 60227-2<br>+ corr. April<br>+ A1 | 1997<br>1998<br>2003 | Polyvinyl chloride insulated cables of rated voltages up to and including 450/750 V - Part 2: Test methods                    | -                                | -                    |
| IEC 60228                            | 2004                 | Conductors of insulated cables                                                                                                | EN 60228<br>+ corr. May          | 2005<br>2005         |
| IEC 60304                            | 1982                 | Standard colours for insulation for low-frequency cables and wires                                                            | HD 402 S2                        | 1984                 |
| IEC 60352-6                          | 1997                 | Solderless connections - Part 6: Insulation piercing connections - General requirements, test methods and practical guidance  | EN 60352-6                       | 1997                 |
| IEC 60364-4-41                       | –                    | Low-voltage electrical installations                                                                                          | HD 60364-4-41 (modified)<br>+A11 | 2017<br>2017         |
| IEC 60529                            | –                    | Degrees of protection provided by enclosures (IP Code)                                                                        | EN 60529<br>+A1<br>+A2           | 1991<br>2000<br>2013 |
| IEC 60947-1<br>+A1                   | 2007<br>2010         | Low-voltage switchgear and controlgear - Part 1: General rules                                                                | EN 60947-1<br>+A1                | 2007<br>2011         |
| IEC 60947-4-1                        | 2018                 | Low-voltage switchgear and controlgear - Part 4-1: Contactors and motor-starters                                              | EN 60947-4-1                     | 2019                 |

## EN 62026-2:2013+A1:2019 (E)

| <u>Publication</u> | <u>Year</u> | <u>Title</u>                                                                                                                                                         | <u>EN/HD</u> | <u>Year</u> |
|--------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-------------|
| IEC 60947-4-2      | 2011        | Low-voltage switchgear and controlgear - Part 4-2: Contactors and motor-starters - AC semiconductor motor controllers and starters                                   | EN 60947-4-2 | 2012        |
| IEC 60947-5-2      | 2007        | Low-voltage switchgear and controlgear - Part 5-2: Control circuit devices and switching elements - Proximity switches                                               | EN 60947-5-2 | 2007        |
| +A1                | 2012        |                                                                                                                                                                      | +A1          | 2012        |
| IEC 61000-4-2      | 2008        | Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test                                           | EN 61000-4-2 | 2009        |
| IEC 61000-4-3      | 2006        | Electromagnetic compatibility (EMC) - Part 4-3: Testing and measurement techniques - Radiated, radio-frequency, electromagnetic field immunity test                  | EN 61000-4-3 | 2006        |
| +A1                | 2007        |                                                                                                                                                                      | +A1          | 2008        |
| +A2                | 2010        |                                                                                                                                                                      | +A2          | 2010        |
| IEC 61000-4-4      | 2012        | Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test                                   | EN 61000-4-4 | 2012        |
| IEC 61000-4-6      | 2008        | Electromagnetic compatibility (EMC) - Part 4-6: Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields           | EN 61000-4-6 | 2009        |
| IEC 61000-4-6      | 2013        | Electromagnetic compatibility (EMC) - Part 4-6: Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields           | EN 61000-4-6 | 2014        |
|                    |             |                                                                                                                                                                      | + AC         | 2015        |
| IEC 61131-2        | –           | Industrial-process measurement and control - Programmable controllers - Part 2: Equipment requirements and tests                                                     | EN 61131-2   | 2007        |
| IEC 61140          | –           | Protection against electric shock - Common aspects for installation and equipment                                                                                    | EN 61140     | 2016        |
| IEC 61508          | series      | Functional safety of electrical/electronic/programmable electronic safety-related systems                                                                            | EN 61508     | series      |
| IEC 61800-2        | –           | Adjustable speed electrical power drive systems - Part 2: General requirements - Rating specifications for low voltage adjustable frequency a.c. power drive systems | EN 61800-2   | 2015        |
| IEC 61915          | series      | Low-voltage switchgear and controlgear – Device profiles for networked industrial devices                                                                            | EN 61915     | series      |
| IEC 62026-1        | 2007        | Low-voltage switchgear and controlgear - Controller-device interfaces (CDIs) - Part 1: General rules                                                                 | EN 62026-1   | 2007        |

## Annex ZZ (informative)

### Relationship between this European standard and the essential requirements of Directive 2014/30/EU [2014 OJ L96] aimed to be covered

This European standard has been prepared under the European Commission standardisation request C(2016) 7641 final of 30.11.2016<sup>1</sup>, ('M/552'), as regards harmonised standards in support of Directive 2014/30/EU relating to electromagnetic compatibility, to provide one voluntary means of conforming to essential requirements of Directive 2014/30/EU of the European Parliament and of the Council of 26 February 2014 on the harmonisation of the laws of the Member States relating to electromagnetic compatibility [2014 OJ L96].

Once this standard is cited in the Official Journal of the European Union under that Directive, compliance with the normative clauses of this standard given in Table ZZ.1 confers, within the limits of the scope of this standard, a presumption of conformity with the corresponding essential requirements of that Directive, and associated EFTA regulations.

**Table ZZ.1 – Correspondence between this European standard and the Essential Requirements set out in Directive 2014/30/EU [2014 OJ L96]**

| Essential requirements of Directive 2014/30/EU | Clause(s) / sub-clause(s) of this EN                    | Remarks / Notes |
|------------------------------------------------|---------------------------------------------------------|-----------------|
| Annex I. 1(a) (electromagnetic disturbances)   | 8.6.1, 8.6.3, 9.1.2, 9.5.9.1, 9.5.9.5                   |                 |
| Annex I. 1(b) (electromagnetic immunity)       | 8.6.1, 8.6.2, 9.1.2, 9.5.9.1, 9.5.9.2, 9.5.9.3, 9.5.9.4 |                 |

**WARNING 1:** Presumption of conformity stays valid only as long as a reference to this European standard is maintained in the list published in the Official Journal of the European Union. Users of this standard should consult frequently the latest list published in the Official Journal of the European Union.

**WARNING 2:** Other Union legislation may be applicable to the product(s) falling within the scope of this standard.

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<sup>1</sup> COMMISSION IMPLEMENTING DECISION C(2016) 7641 final of 30.11.2016 on a standardisation request to the European Committee for Standardisation, to the European Committee for Electrotechnical Standardisation and to the European Telecommunications Standards Institute as regards harmonised standards in support of Directive 2014/30/EU of the European Parliament and of the Council of 26 February 2014 on the harmonisation of the laws of the Member States relating to electromagnetic compatibility.

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## CONTENTS

|                                                                                                                                       |     |
|---------------------------------------------------------------------------------------------------------------------------------------|-----|
| FOREWORD.....                                                                                                                         | 7   |
| 1 Scope and object.....                                                                                                               | 9   |
| 2 Normative references .....                                                                                                          | 9   |
| 3 Terms, definitions, symbols and abbreviations.....                                                                                  | 11  |
| 4 Classification .....                                                                                                                | 18  |
| 5 Characteristics .....                                                                                                               | 21  |
| 6 Product information .....                                                                                                           | 60  |
| 7 Normal service, mounting and transport conditions.....                                                                              | 62  |
| 8 Constructional and performance requirements.....                                                                                    | 63  |
| 9 Tests .....                                                                                                                         | 90  |
| Annex A (normative) Slave profiles .....                                                                                              | 135 |
| Annex B (normative) Master profiles .....                                                                                             | 213 |
| Figure 1 – AS-i components and interfaces.....                                                                                        | 19  |
| Figure 2 – Transmission coding .....                                                                                                  | 21  |
| Figure 3 – Receiver requirements .....                                                                                                | 23  |
| Figure 4 – AS-i power supply .....                                                                                                    | 24  |
| Figure 5 – Equivalent schematic of symmetrization and decoupling circuit .....                                                        | 25  |
| Figure 6 – Model of the AS-i transmission medium.....                                                                                 | 26  |
| Figure 7 – Transactions .....                                                                                                         | 28  |
| Figure 8 – Master and slave pause as viewed from master/slave point of view.....                                                      | 28  |
| Figure 9 – Representation of the master pause.....                                                                                    | 29  |
| Figure 10 – Structure of a master request.....                                                                                        | 31  |
| Figure 11 – Structure of a slave response.....                                                                                        | 34  |
| Figure 12 – Structure of a data exchange request (top: standard address mode;<br>bottom: extended address mode).....                  | 34  |
| Figure 13 – Structure of the slave response (Data_Exchange).....                                                                      | 35  |
| Figure 14 – Structure of the Write_Parameter request (top: standard addressing mode;<br>bottom: extended addressing mode).....        | 35  |
| Figure 15 – Structure of the slave response (Write_Parameter) .....                                                                   | 35  |
| Figure 16 – Structure of the Address_Assignment request.....                                                                          | 36  |
| Figure 17 – Structure of the slave response (Address_Assignment).....                                                                 | 36  |
| Figure 18 – Structure of the Write_Extended_ID-Code_1 request .....                                                                   | 36  |
| Figure 19 – Structure of the slave response (Write_Extended_ID-Code_1) .....                                                          | 36  |
| Figure 20 – Structure of the Reset_Slave request (top: standard addressing mode;<br>bottom: extended addressing mode) .....           | 37  |
| Figure 21 – Structure of the slave response (Reset_Slave).....                                                                        | 37  |
| Figure 22 – Structure of the Delete_Address request (top: standard addressing mode;<br>bottom: extended addressing mode) .....        | 37  |
| Figure 23 – Structure of the slave response (Delete_Address).....                                                                     | 37  |
| Figure 24 – Structure of the Read_I/O_Configuration request (top: standard<br>addressing mode; bottom: extended addressing mode)..... | 38  |

|                                                                                                                                                                      |    |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| Figure 25 – Structure of the slave response (Read_I/O_Configuration) .....                                                                                           | 38 |
| Figure 26 – Structure of Read_Identification_Code request (top: standard addressing mode; bottom: extended addressing mode).....                                     | 39 |
| Figure 27 – Structure of the slave response (Read_Identification_Code) .....                                                                                         | 39 |
| Figure 28 – Structure of Read_Extended_ID-Code_1/2 Request (top: standard addressing mode; bottom: extended addressing mode).....                                    | 40 |
| Figure 29 – Structure of the slave response Read_Extended_ID-Code_1/2.....                                                                                           | 40 |
| Figure 30 – Structure of Read_Status request (top: standard addressing mode; bottom: extended addressing mode) .....                                                 | 41 |
| Figure 31 – Structure of the slave response (Read_Status) .....                                                                                                      | 41 |
| Figure 32 – Structure of R1 request (top: standard addressing mode; bottom: extended addressing mode).....                                                           | 41 |
| Figure 33 – Structure of the slave response (R1) .....                                                                                                               | 41 |
| Figure 34 – Structure of the Broadcast (Reset) request.....                                                                                                          | 42 |
| Figure 35 – Definition of the I/O data bits in combined transaction type 1 .....                                                                                     | 43 |
| Figure 36 – Definition of the parameter bits in combined transaction type 1 .....                                                                                    | 43 |
| Figure 37 – Function sequence to Read ID, Read Diagnosis, Read Parameter in combined transaction type 1 .....                                                        | 46 |
| Figure 38 – Function sequence to Write Parameter in combined transaction type 1 .....                                                                                | 47 |
| Figure 39 – Behaviour of the slave receiving a complete parameter string from the master in combined transaction type 1 .....                                        | 48 |
| Figure 40 – Definition of the I/O data bits in combined transaction type 2 .....                                                                                     | 49 |
| Figure 41 – Typical combined transaction type 2 signals as viewed by an oscilloscope (both data channels run idle) .....                                             | 50 |
| Figure 42 – Typical combined transaction type 2 signals (the master transmits the byte 10101011 <sub>Bin</sub> , the slave transmits 01110101 <sub>Bin</sub> ):..... | 51 |
| Figure 43 – Definition of the I/O data bits in combined transaction type 3 (4I/4O) .....                                                                             | 52 |
| Figure 44 – Definition and state diagram of the slave for combined transaction type 3 .....                                                                          | 53 |
| Figure 45 – Definition of the I/O data bits in combined transaction type 4 .....                                                                                     | 55 |
| Figure 46 – AS-i standard cable for field installation .....                                                                                                         | 63 |
| Figure 47 – AS-i cabinet cable .....                                                                                                                                 | 64 |
| Figure 48 – Equivalent schematic of decoupling circuit .....                                                                                                         | 68 |
| Figure 49 – Decoupling circuit using a transformer .....                                                                                                             | 68 |
| Figure 50 – Typical timing diagram for bidirectional input/outputs (D1, .. D3 = voltage level at respective data port).....                                          | 70 |
| Figure 51 – Main state diagram of an AS-i slave .....                                                                                                                | 73 |
| Figure 52 – Equivalent circuit of a slave for frequencies in the range of 50 kHz to 300 kHz .....                                                                    | 81 |
| Figure 53 – A slave with C3 to compensate for $Z_1 = Z_2$ .....                                                                                                      | 82 |
| Figure 54 – Status indication on slaves.....                                                                                                                         | 84 |
| Figure 55 – Structure of an AS-i master .....                                                                                                                        | 86 |
| Figure 56 – Impedances of the master .....                                                                                                                           | 87 |
| Figure 57 – Equivalent circuit of a master for frequencies in the range of 50 kHz to 300 kHz .....                                                                   | 87 |
| Figure 58 – Transmission control state machine .....                                                                                                                 | 88 |
| Figure 59 – AS-i interfaces .....                                                                                                                                    | 89 |

|                                                                         |     |
|-------------------------------------------------------------------------|-----|
| Figure 60 – Test circuit for impedance measurement .....                | 92  |
| Figure 61 – Adjustable current sink (test circuit: NT_MODSENKE).....    | 93  |
| Figure 62 – Indicator (test circuit NT_IMPSYM) .....                    | 93  |
| Figure 63 – Display (part of test circuit NT_IMPSYM) .....              | 94  |
| Figure 64 – Test set-up for symmetry measurement.....                   | 94  |
| Figure 65 – Test circuit for noise emission .....                       | 96  |
| Figure 66 – Filter A (low-pass filter 0 Hz to 10 kHz) .....             | 96  |
| Figure 67 – Filter B (bandpass filter 10 kHz to 500 kHz) .....          | 96  |
| Figure 68 – Test circuit for start-up behaviour.....                    | 97  |
| Figure 69 – Measurement set-up for impedance measurement .....          | 99  |
| Figure 70 – Test circuit for symmetry measurement .....                 | 101 |
| Figure 71 – Test circuit (detail 1) .....                               | 102 |
| Figure 72 – Test circuit (detail 2) .....                               | 102 |
| Figure 73 – Bandpass (10 kHz ... 500 kHz) .....                         | 102 |
| Figure 74 – Procedure for symmetry test .....                           | 103 |
| Figure 75 – Test circuit for interoperability in AS-i networks.....     | 104 |
| Figure 76 – Additional test circuit 1 for repeater.....                 | 105 |
| Figure 77 – Additional test circuit 2 for repeater.....                 | 105 |
| Figure 78 – Test circuit .....                                          | 106 |
| Figure 79 – Test circuit decoupling network .....                       | 107 |
| Figure 80 – Test circuit .....                                          | 108 |
| Figure 81 – Test circuit decoupling network .....                       | 108 |
| Figure 82 – Test circuit (equivalent of 10 m AS-i line) .....           | 108 |
| Figure 83 – Test circuit (bandpass 10 kHz to 500 kHz) .....             | 109 |
| Figure 84 – Test circuit .....                                          | 110 |
| Figure 85 – Constant current source .....                               | 110 |
| Figure 86 – Test circuit .....                                          | 112 |
| Figure 87 – Test circuit .....                                          | 114 |
| Figure 88 – Test circuit (detail 1) .....                               | 114 |
| Figure 89 – Test circuit (detail 2) .....                               | 115 |
| Figure 90 – Procedure for symmetry test .....                           | 116 |
| Figure 91 – Test circuit AS-i network .....                             | 117 |
| Figure 92 – Test circuit for safety related slaves .....                | 118 |
| Figure 93 – Test circuit for current consumption test.....              | 120 |
| Figure 94 – Decoupling network, ammeter and power supply.....           | 121 |
| Figure 95 – Test circuit noise emission AS-i master .....               | 122 |
| Figure 96 – Decoupling network.....                                     | 122 |
| Figure 97 – Bandpass 10 kHz to 500 kHz .....                            | 122 |
| Figure 98 – Equivalent circuit of the 10 m AS-i line .....              | 122 |
| Figure 99 – Test circuit impedance measurement .....                    | 125 |
| Figure 100 – Master connection for symmetry measurement.....            | 126 |
| Figure 101 – Test circuit symmetry measurement of the AS-i master ..... | 127 |
| Figure 102 – Bandpass 10 kHz to 500 kHz.....                            | 127 |

|                                                                                                               |     |
|---------------------------------------------------------------------------------------------------------------|-----|
| Figure 103 – Procedure for symmetry test.....                                                                 | 128 |
| Figure 104 – Test circuit – On-delay .....                                                                    | 129 |
| Figure 105 – Oscillogram on-delay (example) .....                                                             | 129 |
| Figure 106 – Block circuit diagram current consumption measurement of the AS-i master .....                   | 130 |
| Figure 107 – Constant current source with trigger output (KONST_I) .....                                      | 130 |
| Figure 108 – Oscillogram current consumption (example) .....                                                  | 130 |
| Figure 109 – Test circuit for checking start-up operation .....                                               | 131 |
| Figure 110 – Test circuit for checking normal operation .....                                                 | 132 |
| Figure 111 – Test circuit .....                                                                               | 134 |
| Figure A.1 – Definition of the extended ID2 code bits for S-7.3 .....                                         | 180 |
| Figure A.2 – Definition of the extended ID2 code bits for S-7.4 .....                                         | 184 |
| Figure A.3 – Data structure of the ID string (S-7.4) .....                                                    | 189 |
| Figure A.4 – Data structure of the diagnostic string (S-7.4) .....                                            | 193 |
| Figure A.5 – Data structure of the parameter string (S-7.4) .....                                             | 194 |
| Figure A.6 – Definition of the extended ID1 code bits for S-7.A.8 and S-7.A.9 .....                           | 204 |
| Figure A.7 – Connection of mechanical switches .....                                                          | 211 |
| Table 1 – AS-i power supply specifications .....                                                              | 24  |
| Table 2 – Symmetrization and decoupling circuit specifications .....                                          | 25  |
| Table 3 – Bit strings of the master requests .....                                                            | 31  |
| Table 4 – Master requests (standard addressing mode) .....                                                    | 32  |
| Table 5 – Master requests in the extended addressing mode .....                                               | 33  |
| Table 6 – Bit strings of the slave responses .....                                                            | 34  |
| Table 7 – I/O Codes (IN = Input; OUT = Output; TRI = Tristate; I/O = Input/Output or Bidirectional (B)) ..... | 39  |
| Table 8 – List of combined transaction types .....                                                            | 42  |
| Table 9 – Data transfer from slave to master in combined transaction type 1 .....                             | 44  |
| Table 10 – Data transfer from master to slave in combined transaction type 1 .....                            | 44  |
| Table 11 – Definition of serial clock and data in combined transaction type 2 .....                           | 50  |
| Table 12 – Data transfer in combined transaction type 2 .....                                                 | 50  |
| Table 13 – Definition of the ID2 code in combined transaction type 5 .....                                    | 56  |
| Table 14 – Input states of safety related input slaves .....                                                  | 59  |
| Table 15 – Connection and wiring identification .....                                                         | 61  |
| Table 16 – AS-i power supply marking .....                                                                    | 62  |
| Table 17 – Environmental conditions (minimum conditions) .....                                                | 66  |
| Table 18 – General requirements for an AS-i power supply .....                                                | 67  |
| Table 19 – Physical and logical ports of an AS-i slave .....                                                  | 70  |
| Table 20 – Limits for R, L and C of the equivalent circuit of a slave .....                                   | 82  |
| Table 21 – Limits for R, L and C of the equivalent circuit of a master .....                                  | 87  |
| Table A.1 – Overview of existing slave profiles for standard slaves .....                                     | 137 |
| Table A.2 – List of existing profiles for standard slaves .....                                               | 137 |
| Table A.3 – Overview of existing slave profiles with extended address .....                                   | 138 |

|                                                                                        |     |
|----------------------------------------------------------------------------------------|-----|
| Table A.4 – List of existing profiles for slaves in extended address mode (ID=A) ..... | 138 |
| Table A.5 – Profile catalogue of S-7.D profiles .....                                  | 158 |
| Table A.6 – Overview of data of S-7.D profiles .....                                   | 158 |
| Table A.7 – Profile catalogue of S-7.E profile .....                                   | 163 |
| Table A.8 – Overview of data of S-7.E profiles .....                                   | 163 |
| Table A.9 – Commands for combined transaction type 2 .....                             | 197 |
| Table A.10 – Acyclic write service request (Type 2) .....                              | 198 |
| Table A.11 – Acyclic read service request (Type 2) .....                               | 198 |
| Table A.12 – Acyclic write service response (Type 2) .....                             | 198 |
| Table A.13 – Acyclic read service response (Type 2) .....                              | 198 |
| Table A.14 – List of index 0 (mandatory): ID object (R) .....                          | 199 |
| Table A.15 – List of index 1 (mandatory): diagnosis object (R) .....                   | 199 |

## INTERNATIONAL ELECTROTECHNICAL COMMISSION

### LOW-VOLTAGE SWITCHGEAR AND CONTROLGEAR – CONTROLLER-DEVICE INTERFACES (CDIs) –

#### Part 2: Actuator sensor interface (AS-i)

#### FOREWORD

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International Standard IEC 62026-2 has been prepared by subcommittee 17B: Low-voltage switchgear and controlgear, of IEC technical committee 17: Switchgear and controlgear.

This second edition of IEC 62026-2 cancels and replaces the first edition published in 2000. This second edition constitutes a technical revision.

The main changes with respect to the previous edition are listed below:

- doubling the number of slaves from 31 to 62 by introduction of sub-addresses;
- introduction of AS-I safety system.

The text of this standard is based on the third edition and the following documents:

| FDIS          | Report on voting |
|---------------|------------------|
| 17B/1579/FDIS | 17B/1584/RVD     |

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62026 series, under the general title *Low-voltage switchgear and controlgear – Controller-device interfaces (CDIs)*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under “<http://webstore.iec.ch>” in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

## LOW-VOLTAGE SWITCHGEAR AND CONTROLGEAR – CONTROLLER-DEVICE INTERFACES (CDIs) –

### Part 2: Actuator sensor interface (AS-i)

#### 1 Scope and object

This part of IEC 62026 specifies a method for communication between a single control device and switching elements, and establishes a system for the interoperability of components with the specified communication interfaces. The complete system is called “Actuator Sensor interface (AS-i)”.

This standard describes a method for connecting switching elements, such as low-voltage switchgear and controlgear, standardized within IEC 60947, and controlling devices. The method may also be applied for connecting other devices and elements.

Where inputs and outputs I/O are described in this standard, their meaning is regarding the master, the meaning regarding the application is the opposite.

The object of this standard is to specify the following requirements for control circuit devices and switching elements:

- requirements for a transmission system and for interfaces between a slave, a master and electromechanical structures;
- requirements for a complete interoperability of different devices within any network, when meeting this standard;
- requirements for an interchangeability of devices within a network, when fulfilling the profiles of this standard;
- normal service conditions for the slaves, electromechanical devices and master;
- constructional and performance requirements;
- tests to verify conformance to requirements.

#### 2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

**[A1]** IEC 60068-2-6, *Environmental testing – Part 2-6: Tests – Test Fc: Vibration (sinusoidal)*

IEC 60068-2-27, *Environmental testing – Part 2-27: Tests – Test Ea and guidance: Shock*

IEC 60204-1:2016, *Safety of machinery – Electrical equipment of machines – Part 1: General requirements*

IEC 60227-2:1997, *Polyvinyl chloride insulated cables of rated voltages up to and including 450/750 V – Part 2: Test methods*  
Amendment 1 (2003)

IEC 60228:2004, *Conductors of insulated cables*

IEC 60304:1982, *Standard colours for insulation for low-frequency cables and wires*

IEC 60352-6:1997, *Solderless connections – Part 6: Insulation piercing connections – General requirements, test methods and practical guidance*

IEC 60364-4-41, *Low-voltage electrical installations – Part 4-41: Protection for safety – Protection against electric shock*

IEC 60529, *Degrees of protection provided by enclosures (IP code)*

IEC 60947-1:2007, *Low-voltage switchgear and controlgear – Part 1: General rules*  
IEC 60947-1:2007/AMD1:2010

IEC 60947-4-1:2018, *Low-voltage switchgear and controlgear – Part 4-1: Contactors and motor-starters – Electromechanical contactors and motor-starters*

IEC 60947-4-2:2011, *Low-voltage switchgear and controlgear – Part 4-2: Contactors and motor-starters – AC semiconductor motor controllers and starters*

IEC 60947-5-2:2007, *Low-voltage switchgear and controlgear – Part 5-2: Control circuit devices and switching elements – Proximity switches*  
IEC 60947-5-2:2007/AMD1:2012

IEC 61000-4-2:2008, *Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test*

IEC 61000-4-3:2006, *Electromagnetic compatibility (EMC) – Part 4-3: Testing and measurement techniques – Radiated, radio-frequency, electromagnetic field immunity test*  
IEC 61000-4-3:2006/AMD1:2007  
IEC 61000-4-3:2006/AMD2:2010

IEC 61000-4-4:2012, *Electromagnetic compatibility (EMC) – Part 4-4: Testing and measurement techniques – Electrical fast transient/burst immunity test*

IEC 61000-4-6:2013, *Electromagnetic compatibility (EMC) – Part 4-6: Testing and measurement techniques – Immunity to conducted disturbances, induced by radio-frequency fields*

IEC 61131-2, *Industrial-process measurement and control – Programmable controllers – Part 2: Equipment requirements and tests*

IEC 61140, *Protection against electric shock – Common aspects for installation and equipment*

IEC 61508 (all parts), *Functional safety of electrical/electronic/programmable electronic safety-related systems*

IEC 61800-2, *Adjustable speed electrical power drive systems – Part 2: General requirements – Rating specifications for low voltage adjustable speed a.c. power drive systems*

IEC 61915 (all parts), *Low-voltage switchgear and controlgear – Device profiles for networked industrial devices*

IEC 62026-1:2007, *Low-voltage switchgear and controlgear – Controller-device interfaces (CDIs) – Part 1: General rules*

CISPR 11:2015, *Industrial, scientific and medical (ISM) equipment – Radio-frequency disturbance characteristics – Limits and methods of measurement*

CISPR 11:2015/AMD1:2016 

-  EN 61000-4-6:2009, *Electromagnetic compatibility (EMC) – Part 4-6: Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields (IEC 61000-4-6:2008)* 

### 3 Terms, definitions, symbols and abbreviations

For the purposes of this document, the terms, definitions, symbols and abbreviations given in IEC 62026-1 as well as the following apply.

#### 3.1 Terms and definitions

*Alphabetical index of definitions*

*Reference*

| A                                       |        |
|-----------------------------------------|--------|
| Active slave .....                      | 3.1.1  |
| Actuator Sensor interface (AS-i) .....  | 3.1.2  |
| Address .....                           | 3.1.3  |
| Address assignment .....                | 3.1.4  |
| Analogue input data image (AIDI) .....  | 3.1.5  |
| Analogue output data image (AODI) ..... | 3.1.6  |
| AS-i cycle .....                        | 3.1.7  |
| AS-i input .....                        | 3.1.8  |
| AS-i line .....                         | 3.1.9  |
| AS-i master .....                       | 3.1.10 |
| AS-i network .....                      | 3.1.11 |
| AS-i output .....                       | 3.1.12 |
| AS-i power supply .....                 | 3.1.13 |
| AS-i slave .....                        | 3.1.14 |
| B                                       |        |
| Bit time (effective) .....              | 3.1.15 |
| C                                       |        |
| Configuration data (CD) .....           | 3.1.16 |
| Configuration data image (CDI) .....    | 3.1.17 |
| Controller .....                        | 3.1.18 |
| Controller interface .....              | 3.1.19 |
| D                                       |        |
| Data exchange phase .....               | 3.1.20 |
| Decoupling circuit .....                | 3.1.21 |
| Detection phase .....                   | 3.1.22 |
| E                                       |        |
| Earth fault detector .....              | 3.1.23 |
| Execution control .....                 | 3.1.24 |
| Extended addressing mode .....          | 3.1.25 |
| F                                       |        |
| Field devices .....                     | 3.1.26 |
| I                                       |        |
| I/O configuration (I/O code) .....      | 3.1.27 |
| Identification code (ID code) .....     | 3.1.28 |
| Input data image (IDI) .....            | 3.1.29 |
| L                                       |        |
| List of activated slaves (LAS) .....    | 3.1.30 |
| List of detected slaves (LDS) .....     | 3.1.31 |
| List of peripheral faults (LPF) .....   | 3.1.32 |
| List of projected slaves (LPS) .....    | 3.1.33 |

|                                |        |
|--------------------------------|--------|
| M                              |        |
| Master .....                   | 3.1.34 |
| Master pause .....             | 3.1.35 |
| Master request .....           | 3.1.36 |
| N                              |        |
| Non-volatile stored data ..... | 3.1.37 |
| O                              |        |
| Operation address .....        | 3.1.38 |
| Output current limit .....     | 3.1.39 |
| Output data image (ODI) .....  | 3.1.40 |
| P                              |        |
| Parameter image (PI) .....     | 3.1.41 |
| P-fault .....                  | 3.1.42 |
| R                              |        |
| Repeater .....                 | 3.1.43 |
| S                              |        |
| Select bit .....               | 3.1.44 |
| Send pause .....               | 3.1.45 |
| Slave .....                    | 3.1.46 |
| Slave pause .....              | 3.1.47 |
| Slave response .....           | 3.1.48 |
| Symmetrizing circuit .....     | 3.1.49 |
| T                              |        |
| Transaction .....              | 3.1.50 |
| Transmission control .....     | 3.1.51 |
| V                              |        |
| Volatile stored data .....     | 3.1.52 |
| Z                              |        |
| Zero address .....             | 3.1.53 |

### 3.1.1

#### **active slave**

slave connected to the AS-i line and capable to communicate properly

### 3.1.2

#### **Actuator Sensor interface (AS-i)**

set of interfaces and serial communication method for the connection of low-voltage switchgear and controlgear, and other simple field devices with a controller

### 3.1.3

#### **address**

numerical parameter out of the address space of the AS-i slaves which specifies a node of an AS-i network

NOTE Address 0 is reserved for slaves which have not had an address assigned.

### 3.1.4

#### **address assignment**

replacement of the existing address of the AS-i slave with a new address

### 3.1.5

#### **Analogue Input Data Image (AIDI)**

input data stored in the master, containing the latest actual copies of the received data from the inputs of all active slaves using combined transactions type 1 to 5

### 3.1.6

#### **Analogue Output Data Image (AODI)**

output data stored in the master to be transmitted cyclically to the active slaves with outputs using combined transactions types 1 to 5

### 3.1.7

#### **AS-i cycle**

set of up to 33 transactions

NOTE 1 A cycle may, in case of a detected communication failure, include one message retransmission.

NOTE 2 In the case of extended addressing mode, two cycles will be needed for data transfer of all slaves that are in extended addressing mode.

### 3.1.8

#### **AS-i input**

physical or logical slave port providing an input from the process

### 3.1.9

#### **AS-i line**

two-wire line for transferring information and power to the AS-i slaves and the AS-i master

### 3.1.10

#### **AS-i master**

unit on the AS-i line that manages the communication between the slaves and the controller

### 3.1.11

#### **AS-i network**

network composed of an AS-i control circuit, interfaces and switching elements, for example master, slaves, power supply, cable, taps, repeaters

### 3.1.12

#### **AS-i output**

physical or logical slave port providing an output to the process

### 3.1.13

#### **AS-i power supply**

special power supply combining a d.c. supply and a symmetrizing and decoupling circuit needed in an AS-i network

### 3.1.14

#### **AS-i slave**

physical and logical means to connect the application devices (actuator, sensor, or other components) to the AS-i line

NOTE A slave may be a stand alone device or part of another device.

### 3.1.15

#### **bit time**

$T_{\text{Bit}}$

duration of the transmission of one bit

### **3.1.16**

#### **configuration data (CD)**

value of the I/O configuration and the identification code (optional extended identification codes) of a specific slave

### **3.1.17**

#### **configuration data image (CDI)**

image of the configuration data of all slaves, stored in the AS-i master

### **3.1.18**

#### **controller**

host or operator of the master, for example a programmable logic controller, a personal computer, a gateway, or a human operator

### **3.1.19**

#### **controller interface**

logical interface between the master and the controller

### **3.1.20**

#### **data exchange phase**

period of time during which the master sends output data to the slaves and receives input data from the slaves

### **3.1.21**

#### **decoupling circuit**

part of the AS-i power supply for decoupling the d.c. source and the physical data transmission within the AS-i network

### **3.1.22**

#### **detection phase**

period of time when the execution control of the master tries to find all slaves connected and operating

NOTE All slaves found are listed in the list of detected slaves (LDS).

### **3.1.23**

#### **earth-fault detector**

special insulation monitoring device compatible with the requirements of the AS-i transmission system which allows to detect the asymmetrical deterioration of the insulation between the AS-i network and ground

### **3.1.24**

#### **execution control**

master function that controls the message exchange and provides several functions to the controller interface

### **3.1.25**

#### **extended addressing mode**

doubles the maximum number of slaves from 31 (addresses in the range of 1 to 31) to 62 (addresses in the range of 1A/1B to 31A/31B)

### **3.1.26**

#### **field devices**

items connected to the AS-i slave, for example actuators, sensors, push-buttons, indicator lights, etc.

NOTE "intelligent" field devices also include integrated AS-i circuitry.

### **3.1.27**

#### **I/O-configuration (I/O-code)**

set of four bits which defines the direction of data flow at the slave I/O ports

### **3.1.28**

#### **identification code (ID-code)**

set of four bits which defines the type of slave for a given I/O-configuration (optional: extended ID-codes consisting of additional 2x4bits)

### **3.1.29**

#### **input data image (IDI)**

input data stored in the master, received from the slaves

### **3.1.30**

#### **list of active slaves (LAS)**

list of all slaves at the AS-i line that are activated and capable of communicating properly with the master

NOTE The list is available in the master.

### **3.1.31**

#### **list of detected slaves (LDS)**

list of all slaves actually detected by the master

NOTE The list is available in the master.

### **3.1.32**

#### **list of peripheral faults (LPF)**

list of all slaves with peripheral fault bit set to "1"

NOTE The list is available in the master.

### **3.1.33**

#### **list of projected slaves (LPS)**

list of all configured slaves of the interface system as the target configuration

NOTE The list is available in the master and it includes the configuration data (CD) of all configured slaves.

### **3.1.34**

#### **master**

control unit on the AS-i line that communicates serially with the slaves

### **3.1.35**

#### **master pause**

time between the last bit of a master request and the first bit of the slave response, measured at the master ports

### **3.1.36**

#### **master request**

data or parameter or function sent from the master to a single slave (exception: broadcast)

NOTE The content of this master request is either data (to be moved to the output ports of the slave), parameters or a command

### **3.1.37**

#### **non-volatile stored data**

data that remains unchanged after power interruption

### **3.1.38**

#### **operation address**

address of the AS-i slave other than the zero address

### **3.1.39**

#### **output current limit**

$I_{Lim}$

output current of the power supply not to be exceeded under all environmental and load conditions

### **3.1.40**

#### **output data image**

ODI

output data stored in the master to be transferred to the AS-i slaves

### **3.1.41**

#### **parameter image**

PI

parameters (sets of 4 bits) that define the functionality of all the different slaves in the AS-i network

### **3.1.42**

#### **p-fault**

appliance in a slave for signalling peripheral faults to the master

NOTE In case of a peripheral fault and a "Read\_Status\_Request" of the master the slave response will be "1" in S1 bit.

### **3.1.43**

#### **repeater**

device that regenerates the AS-i signal and provides galvanic separation between parts of the AS-i network so that network lengths of more than 100 m are possible

### **3.1.44**

#### **select bit**

bit in the master request used in extended address mode to distinguish between the A-slave and B-slave

### **3.1.45**

#### **send pause**

period after receipt of the slave response during which no subsequent transmission occurs

### **3.1.46**

#### **slave**

network device or part of another device that provides an interface to the AS-i line and communicates with the master

### **3.1.47**

#### **slave pause**

time between the last bit of a slave response and the start of sending the first bit of the next master request, measured at the master ports

### **3.1.48**

#### **slave response**

message from the slave to the master after a master request has been received and processed without error

NOTE The content of this response is either data or the result of a command.

### **3.1.49**

#### **symmetrizing circuit**

part of the AS-i power supply for conditioning the physical data transmission within the AS-i network

### **3.1.50**

#### **transaction**

(single) comprises a master request and a slave response within the master pause

NOTE Distinction is made between a single transaction, as defined above, and combined transactions of various types. The latter are combined of a series of several single transactions in which the information content is related in a well-defined way.

### **3.1.51**

#### **transmission control**

master function that controls the data transmission, transmission pauses and retransmissions in case of failures (e.g. transmission failures, missing response from the slave, invalid response received, etc.)

### **3.1.52**

#### **volatile stored data**

data that may change following power interruption

### **3.1.53**

#### **zero address**

special address reserved for the online assignment of a new address to an AS-i slave

## **3.2 Symbols and abbreviations**

|           |                                                       |
|-----------|-------------------------------------------------------|
| AIDI      | Analogue Input Data Image                             |
| AODI      | Analogue Output Data Image                            |
| APF       | AS-i power failure                                    |
| APM       | Alternating pulse modulation                          |
| APO       | AS-i power ON                                         |
| AS-i      | Actuator Sensor Interface                             |
| ASI+      | positive potential of the AS-i network                |
| ASI-      | negative potential of the AS-i network                |
| CB        | control bit                                           |
| CD        | configuration data                                    |
| CDI       | configuration data image                              |
| EB        | end bit                                               |
| IDI       | input data image                                      |
| $I_e$     | rated current of AS-i power supply                    |
| $I_{lim}$ | current limit of AS-i power supply                    |
| LAS       | list of active slaves                                 |
| LDS       | list of detected slaves                               |
| LPF       | list of slaves that signal peripheral fault condition |
| LPS       | list of projected slaves                              |
| MAN       | Manchester II code                                    |
| ODI       | output data image                                     |
| PB        | parity bit                                            |

|                   |                                                                                                  |
|-------------------|--------------------------------------------------------------------------------------------------|
| PCD               | permanent configuration data                                                                     |
| PI                | parameter image                                                                                  |
| PP                | permanent parameter                                                                              |
| PSK               | phase shift keying                                                                               |
| SEL               | Select Bit used for extended addressing                                                          |
| ST                | start bit                                                                                        |
| $T_{\text{Bit}}$  | bit time                                                                                         |
| TS                | transaction status                                                                               |
| $00_{\text{Hex}}$ | hexadecimal representation of values, for example $1F_{\text{Hex}} = 31$ , $F_{\text{Hex}} = 15$ |
| $00_{\text{Bin}}$ | binary representation of values, for example $1100_{\text{Bin}} = 12$ , $0110_{\text{Bin}} = 6$  |

## 4 Classification

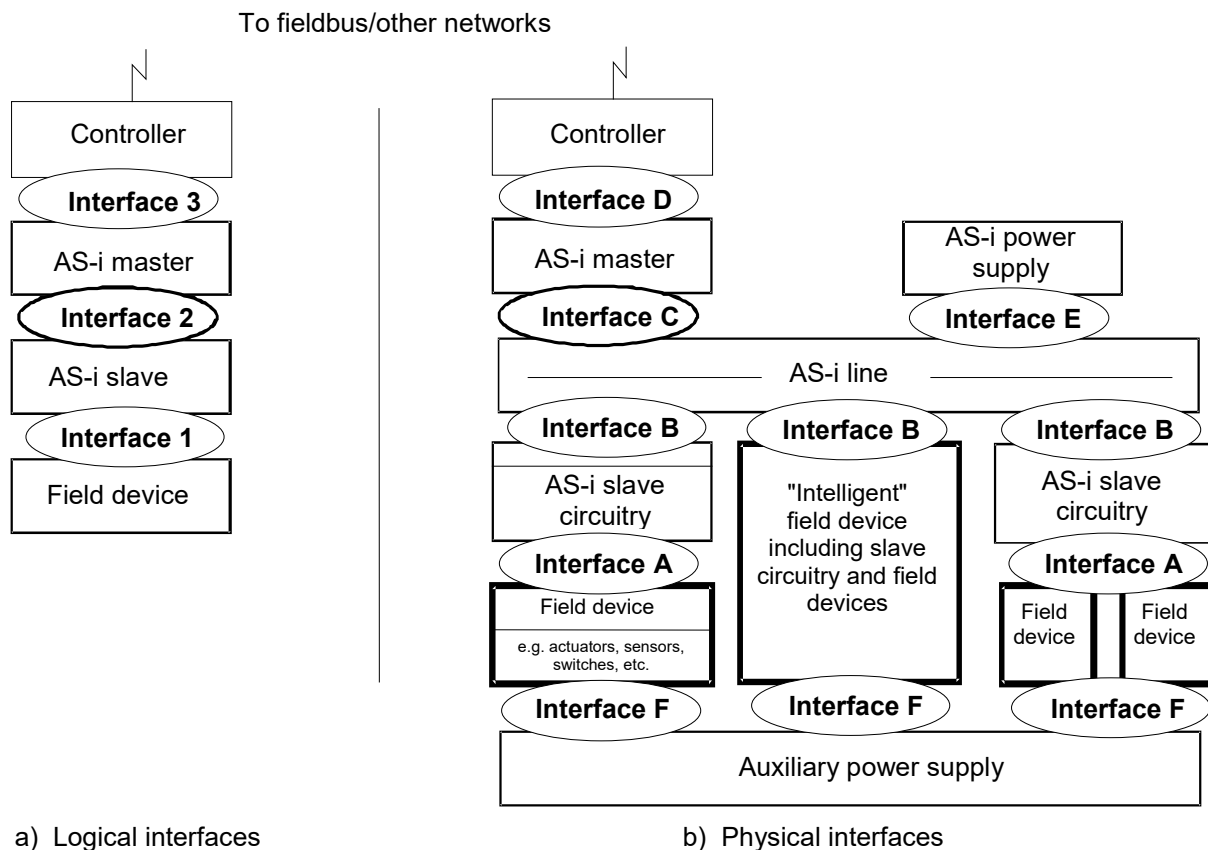
### 4.1 Overview

The Actuator Sensor Interface system will be applied mainly at the lowest level of a multi-level automation hierarchy. AS-i concentrates on the typical requirements for connecting binary elements with a controlling device. Thus, AS-i meets the requirements in machinery and plant construction, where real-time processing, cost effective design, installation, operating, maintenance, and service are essential.

AS-i can be used as an interface physically integrated into actuators, sensors, or other devices and elements themselves, opening an option for "intelligent" binary actuators, sensors, or other devices and elements. AS-i may, as well, be used in separate modules providing an interface for typically four conventional actuators, sensors or other devices and elements already available on the market.

To connect this variety of actuators, sensors, or other devices and elements with a controlling device, AS-i is embedded in a structure of two different units which present three interfaces as shown in Figure 1.

Logically, the AS-i system is a master-slave communication system composed of a single master and up to 31 (62 with extended addressing) slaves. The master sends data and parameters to a specific slave. The slave passes the data to the output ports or processes the requested procedure (e.g. Reset\_Slave) and returns the input data or the result of the successful processed procedure to the master, respectively.



IEC 1145/2000

**Figure 1 – AS-i components and interfaces**

The AS-i concept is independent of the specific type of actuators, sensors, or other devices and elements. It defines the mechanisms and all the components for the communication with a controlling device and it offers electromechanical structures for a standardized "plug and play technique" for installing very simply actuators, sensors, or other devices and elements into an AS-i-network.

The annexes define slave and master profiles of common types of actuators, sensors, or other devices and elements, that will often be used in AS-i systems.

## 4.2 Components and interfaces

As shown in Figure 1, the AS-i system comprises the following components and interfaces.

### 4.2.1 Components

**AS-i slave** The unit that can be accessed by the master via the AS-i line for data exchange, parametrization, and monitoring. The slave has a well-defined logical and functional behaviour. It responds immediately with slave response to a specific request from the master and it ensures that a malfunction of the attached actuator, sensor or other device or of the slave itself will not disturb the communication between the master and the other slaves in the network.

**NOTE 1** The definition of an AS-i slave is logical in nature, but covers the physical requirements for data transmission through the AS-i network, too. The concrete realization of a slave depends on the implementation; for example a specific pinout of an integrated slave chip is not defined in this standard.

**AS-i master** The unit that organizes and monitors the network and schedules the exchange of data, parameters and commands with the AS-i slaves via the AS-i line. The master has a well-defined logical and functional behaviour. It sends master requests to the AS-i slaves and receives the immediate slave responses from them.

NOTE 2 The definition of an AS-i master is mainly logical in nature but covers the physical requirements on data transmission through the AS-i network, too. The concrete realization of a master depends on its implementation. The 'Master Profiles' in Annex B define minimal sets of functions and commands of different master types.

**AS-i power supply** Provides power to the AS-i network and includes the decoupling circuitry.

**AS-i repeater** The unit that regenerates the AS-i signal and provides galvanic separation between parts of the AS-i network so that network lengths of more than 100 m are possible.

**AS-i line** Provides the signalling and d.c. power connections between the AS-i devices.

#### 4.2.2 Logical interfaces

**Interface 1** The slave interface to connect the AS-i slave with the actuators, sensors, or other devices and elements. It is characterized by several ports, which define the input, output or bi-directional input/output behaviour and the parametrization behaviour of the AS-i slave, the timing of the signals, and the power supply for actuators, sensors, or other devices and elements.

NOTE 1 Interface 1 is only a concept. The concrete representation of the interface depends mainly on the implementation. Only by the more restrictive slave profiles given in Annex A it is defined to some further extent.

**Interface 2** The interface that provides all logical, physical, and mechanical requirements for data exchange and power distribution. It comprises signalling of encoded information, the AS-i transactions, mechanical and electrical requirements on the network and the AS-i power supply.

NOTE 2 Interface 2 is concrete in nature. It comprises the bus structure. The requirements of interface 2 are defined in this standard to ensure the interoperability of all components.

**Interface 3** The interface between the controller and the AS-i master that provides all functions used by the controller to access the AS-i master for sending and receiving data to and from slaves, sending a cyclical command to a slave, to set or to obtain flags and values for several lists in the master. This interface allows the controller to manage the master's behaviour and thus the behaviour of the AS-i system. Supported functions are classically "set something" in the master, "get some information" from the master.

NOTE 3 Interface 3 is only a concept. The concrete representation of the interface depends on the implementation. To a large extent, it depends on features of the specific controller system.

#### 4.2.3 Physical interfaces

**Interface A** Defines the physical connection between the field device and the AS-i slave circuitry including physical interface, signal levels and power requirements if any.

**Interface B** Defines the physical connection of the AS-i slave circuitry to the AS-i line including physical interface (mechanical/electrical), signal characteristics and power requirements.

**Interface C** Defines the physical connection of the AS-i master circuitry to the AS-i line including physical interface (mechanical/electrical), signal characteristics and power requirements.

**Interface D** Definition of the physical interface is outside of the scope of this standard and shall be provided by the manufacturer.

**Interface E** Defines the physical connection of the AS-i power supply including the signal decoupling circuit, to the AS-i line.

**Interface F** Defines the physical interface between the field device and an external auxiliary power supply if any.

## 5 Characteristics

### 5.1 Overview

The AS-i system defines digital, serial, multidrop data communication of a master with actuators and sensors or other devices including a power supply. Data and energy are transmitted on the same 2-wire cable.

The AS-i system is designed for protection class III (PELV) according to IEC 61140 (see 8.2). Therefore all components shall meet the corresponding requirements.

The AS-i transmission system provides the communication between up to 62 AS-i slaves and a single AS-i master, i.e. it represents the interface 2 between a master and the slaves (see Figure 1). The AS-i master shall call the individual slaves and get their responses immediately.

Subclauses 5.2 to 5.4 define the physical requirements and 5.5 to 5.7 the logical requirements of this transmission system (messages to be exchanged).

Additional requirements specific for the transmission medium (8.1), for the power supply (8.2), for the repeater and other components (8.3), for the slave (8.4) and for the master (8.5) are defined in the subclauses below.

### 5.2 Signal characteristics

The characteristics of the transmitted signal and the modulation are defined in this subclause.

#### 5.2.1 Transmission coding

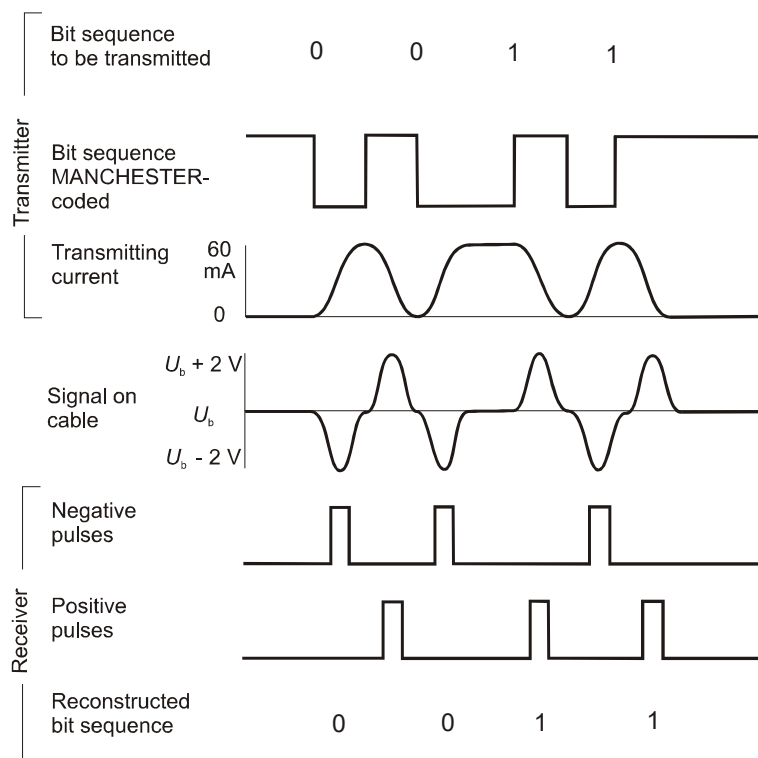


Figure 2 – Transmission coding

NOTE Because the information signal is superimposed on a d.c. supply voltage, a modulation must be employed that does not contain a d.c. voltage part. The transmission is asynchronous. To simplify synchronization of the slave a serially embedded synchronization information in the data signal flow is provided.

All messages are encoded in Manchester II format. Each message includes a start and an end bit. The idle state is represented by a "1". A "0" is encoded by a half bit time with high level followed by a half bit time of low level. A "1" is encoded by a half bit time of low level followed by a half bit time of high level.

The modulation shall be realized by the alternating pulse modulation (APM) with a  $\sin^2$  signal wave form. The rising edge of the Manchester II format shall be represented as a positive and the falling edge as a negative pulse.

The transmission encoding and decoding is shown in Figure 2.

### 5.2.2 Transfer speed

The bit time ( $T_{\text{Bit}}$ ) is defined as 6  $\mu\text{s}$ . Thus, the bit sequence frequency shall be  $166^{2/3}$  kBit/s.

### 5.2.3 Transmitter requirements

The transmitter in both the master and the slave shall be implemented as a current sink. The current signal is superimposed on the d.c. voltage of the AS-i network. A falling edge of the Manchester II coded signal shall cause a current of

$$i(t) = I_{\text{send}} * \left( \frac{t}{3\mu\text{s}} - \frac{1}{2\pi} \sin\left(\frac{2\pi}{3\mu\text{s}} t\right) \right)$$

A rising edge shall cause a current of

$$i(t) = I_{\text{send}} * \left( 1 - \frac{t}{3\mu\text{s}} + \frac{1}{2\pi} \sin\left(\frac{2\pi}{3\mu\text{s}} t\right) \right)$$

The amplitude  $I_{\text{send}}$  of the modulation current shall be between 55 mA and 68 mA.

The maximum deviation from the nominal bit time shall be less or equal to  $\pm 0,1$  % for the master and  $\pm 0,2$  % for the slave.

### 5.2.4 Receiver requirements

Together with the decoupling inductances of the decoupling circuit in the power supply, the send current waveform as defined in 5.2.3 will lead to a negative (positive) voltage pulse at each rising (falling) edge. The waveform of the pulses will be ideally

$$u(t) \approx \pm U_{\text{send}} * \sin^2\left(\frac{2\pi}{6\mu\text{s}} t\right)$$

with  $U_{\text{send}} = \text{const} \approx 2 \text{ V}$

NOTE 1 In a real AS-i System, the declining edge of the pulses is flattened due to the characteristics of the decoupling circuit. In addition, amplitudes and waveform will be influenced by the physical properties of the AS-i line. The receivers therefore must be able to detect a more complex pulse spectrum.

The receiver shall be able to receive and decode a message as described below (see Figure 3).

The maximum pulse amplitude  $U_{\text{max}}$  of a message may vary between 1,5 V peak and 4 V peak.

NOTE 2 The differences in the amplitude  $U_{\max}$  between consecutive Master requests will not vary in one configuration. Shown are the extreme values in different configurations and locations of the slave on the AS-i line. In a constant configuration, the relation of  $U_{\max}$  between two slave responses at different locations of the line is up to 1:1,5.

- The amplitude of a valid pulse within a message may vary from 65 % to 100 % of the maximum amplitude  $U_{\max}$ .

NOTE 3 For slaves according to previous versions of this standard it may vary from 80 % to 100 %.

Valid pulses start in a time window from  $(n * 3 \mu\text{s})_{-0,5 \mu\text{s}}^{+1,0 \mu\text{s}}$  in relation to the initial pulse  $U_{\text{init}}$ . These pulses shall be accepted by the receiver.

Pulses outside a window from  $(n * 3 \mu\text{s})_{-0,8 \mu\text{s}}^{+1,6 \mu\text{s}}$  shall not be accepted by the receiver.

Pulses (noise, ringing) of up to 30 % of  $U_{\max}$  shall not disturb the message reception.

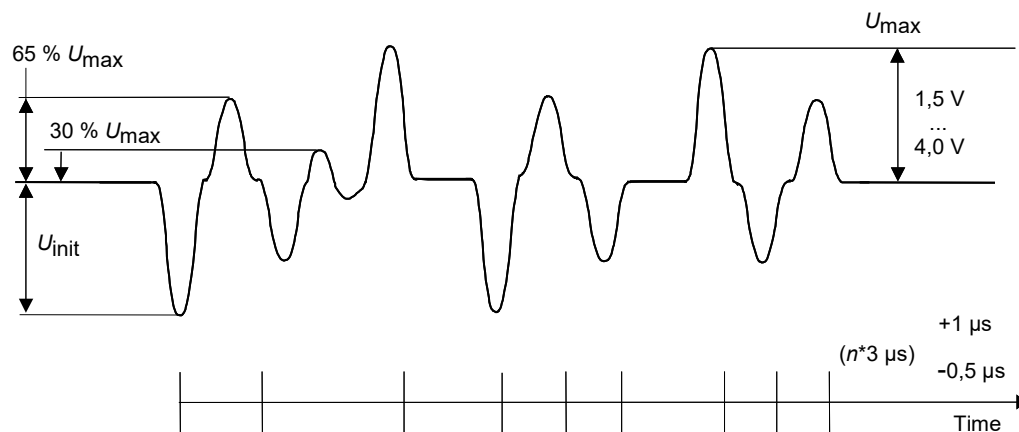


Figure 3 – Receiver requirements

NOTE 4 Pulse deviations from -0,8  $\mu\text{s}$  up to +1,6  $\mu\text{s}$  may occur due to a combination of different effects, for example capacitive load on the AS-i line, deviations from the oscillator frequency in the transmitter and in the receiver.

## 5.3 Power and data distribution

### 5.3.1 General

The simultaneous transmission of data and power on the AS-i line requires technical provisions for decoupling data and power.

The AS-i power supply has to provide the d.c. power for the whole network. On the other hand, it has to realise the conditioning of physical data transmission within the system. This feature comprises symmetrization and forming and adapting transmission signals according to the signal requirements defined in 5.2. The adapting circuit will furthermore be called "decoupling circuit".

Although the functions of these components are independent, it is useful to combine them for practical reasons.

The combination of a d.c. power supply, a symmetrization circuit and a decoupling circuit is called "AS-i power supply".

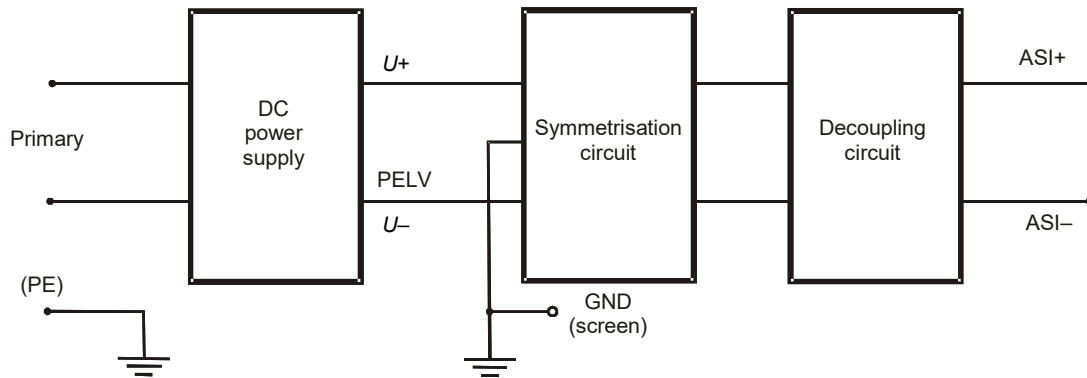


Figure 4 – AS-i power supply

### 5.3.2 AS-i power supply requirements

The AS-i power supply requirements are shown in Table 1:

Table 1 – AS-i power supply specifications

| Characteristic                                                                                         | Specification                                                                                               |
|--------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|
| Output voltage at ASI+/ASI- (over the whole load range)                                                | $U_{ASI} = 29,5 \text{ V d.c. to } 31,6 \text{ V d.c.}$                                                     |
| Rated output current                                                                                   | $I_e$ as stated by the manufacturer                                                                         |
| Additional current to meet charging processes for connecting additional slaves during normal operation | $I_a = 0,4 \text{ A}$ (12,5 mA for each standard slave / 6,5 mA for each slave in extended addressing mode) |
| Current limit                                                                                          | $I_{lim} > I_e + I_a$                                                                                       |
| Amplitude noise in the current range (measured at ASI+/ASI-)                                           | 50 mV <sub>pp</sub> within 10 kHz to 500 kHz (visible noise band on oscilloscope)                           |
| Low frequency ripple (except overload)                                                                 | 300 mV <sub>pp</sub> in the frequency range of 0 kHz to 10 kHz                                              |
| Power on delay                                                                                         | ≤ 2 s after reaching 5 V at output terminals                                                                |

NOTE Any regulation of input and load changes should not affect the communication on the AS-i line; the AS-i transmission activity should not affect the power supply. The total effect on the AS-i line should not exceed the value of 50 mV<sub>pp</sub> or 300 mV<sub>pp</sub>, respectively, see above.

### 5.3.3 Start-up behaviour

Within 2 s after reaching 5 V the first time, the voltage level shall reach the maximum value of the master starting voltage (26,5 V). The time span between the minimum master starting voltage (22,5 V – 1 V, see 8.5.2.1) and the min. AS-i voltage level (29,5 V) shall be less than 1 s. The voltage level has to increase steadily from 5 V up to normal operation voltage (29,5 V to 31,6 V).

NOTE The second demand is important because the master begins to work if the voltage exceeds its starting voltage of 22,5 V ± 1 V.

During start-up the power supply shall supply an increased current to meet the charging process in the system. This additional load will be equal to a capacitance of 15 mF.

Beginning from a voltage level of 5 V, the power supply shall give the rated output current  $I_e$  plus an additional current to load the above mentioned capacitance of 15 mF to meet the time restrictions.

### 5.3.4 Symmetrization and decoupling circuit

The symmetrization and decoupling circuit ensures several functions of the AS-i transmission system:

- providing the d.c. power to the AS-i line;
- signal shaping;
- terminating impedance (for the physical line);
- symmetrizing the AS-i line with respect to GND;
- rejection of common mode noise.

The equivalent decoupling network consists of two inductances and two resistors as well as the symmetrizing capacitors  $C_s$  as shown in Figure 5.

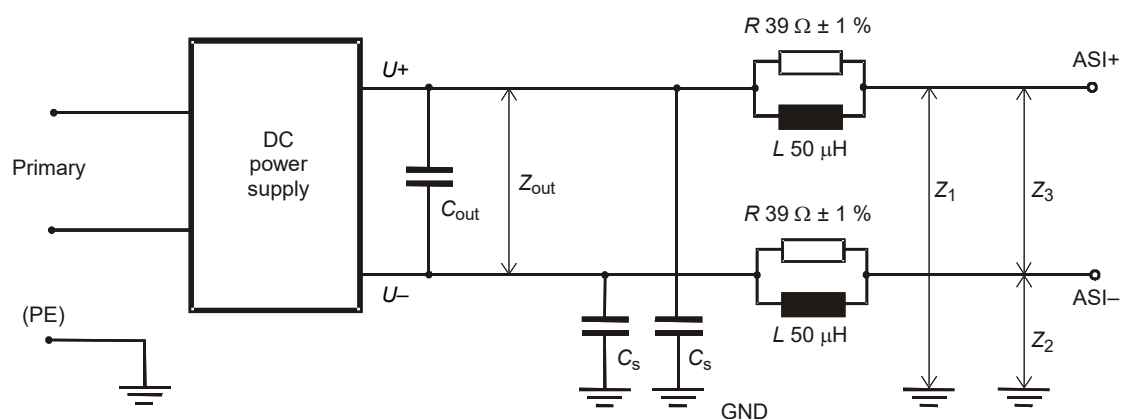


**Figure 5 – Equivalent schematic of symmetrization and decoupling circuit**

The symmetry capacitors  $C_s$  shall be located as close as possible to the decoupling circuit. These capacitances provide a symmetrical relation of ASI+/ASI- to ground. Equal values of at least 100 nF are recommended.

**Table 2 – Symmetrization and decoupling circuit specifications**

| Characteristic                 | Specification                                                                                                   |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------|
| Inductance between ASI+/ASI-   | $100 \mu\text{H} \pm 10 \% \quad (I_L=0 \text{ to } I_{L\text{max}})$                                           |
| Short circuit / overload       | May be applied for infinite time without causing defects in the decoupling circuit                              |
| Symmetry of ASI+/- against GND | $0,98 \leq  Z_1  /  Z_2  \leq 1,02$<br>within the frequency range of 10 kHz to 300 kHz and the whole load range |
| Source impedance               | $ Z_{\text{out}}  < 0,5 \Omega$ in the range of 10 kHz to 300 kHz                                               |
| Decoupling impedance ( $C_s$ ) | $ Z_s  < 5 \Omega$ in the range above 300 kHz                                                                   |

## 5.4 AS-i topology and other components

### 5.4.1 AS-i line (minimum requirements)

The AS-i transmission medium can be any cable, shielded or non-shielded at which the following characteristics shall be provided for the full operating range:

at a frequency of 167 kHz:

|        |                                            |
|--------|--------------------------------------------|
| $R'$ : | $< 90 \text{ m}\Omega/\text{m}$            |
| $C'$ : | $< 80 \text{ pF/m}$                        |
| $Z$ :  | $70 \Omega \text{ to } 140 \Omega$         |
| $G'$ : | $\leq 5 \mu\text{S/m}$                     |
| $L'$ : | $400 \text{ nH/m to } 1\,300 \text{ nH/m}$ |
| $t'$ : | $\leq 8,3 \text{ ns/m}$                    |

The recommended cross-section is  $2 \times 1,5 \text{ mm}^2$ .

For short trunk lines without further branching cables with other specifications are tolerable, if the d.c. voltage drop on these lines does not affect the function of the connected devices.

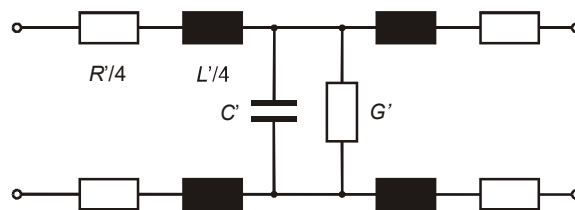


**Figure 6 – Model of the AS-i transmission medium**

NOTE 1 The characteristic impedance  $Z$  of a transmission line is defined by its distributed constants  $R'$ ,  $L'$ ,  $C'$ ,  $G'$  and the frequency in use by the equation

$$Z = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}}$$

The distributed constants can be measured at an electrical short length of the transmission line with open ( $G'$ ,  $C'$ ) respectively, shorted ( $R'$ ,  $L'$ ) end. The additional limitations of  $Z$  and the propagation delay time  $t'$  result from excluding such combinations of distributed constants which would lead to unfavourable high or low values of the characteristic impedance.

NOTE 2 Any cable that meets the above mentioned data may be used as the AS-i line. Nevertheless, several requirements and tolerances of this standard are intended to meet a total voltage drop (d.c.) along the AS-i transmission medium of up to 3 V. It is recommend to use a cross-section so that no higher voltage drop will occur. If a cable is to be used as the AS-i-line that does not meet the above-mentioned data, the total length of 100 m for the complete network may be affected.

NOTE 3 The propagation delay of a signal on the AS-i line is defined by the equation

$$t' = \sqrt{L'C' - \frac{R'G'}{\omega^2}}$$

and is typically  $0,6 \mu\text{s}/100 \text{ m}$  in one direction.

#### 5.4.2 AS-i topology

The AS-i topology is the tree structure. The total length of the AS-i line shall not exceed 100 m. This length shall be calculated as the sum of all trunk lines.

There shall be no connection to GND in the network apart from the port GND at the power supply.

NOTE AS-i has been designed as a symmetrical system. The better the symmetry, the better the rejection of undesirable emission of AS-i signal components as well as incidence of AS-i relevant noise, even if the system is relatively large and distributed. This is important because the network is unshielded and may act as an antenna.

During normal operation, a voltage drop between the power supply and any point of the network of more than 3 V shall not occur unless a possibly higher voltage drop is specified in the product documentation of a particular slave.

#### 5.4.3 AS-i repeater

The total length of the AS-i line is restricted to 100 m. An AS-i repeater regenerates the AS-i signal and provides galvanic separation between parts of the AS-i network so that network lengths of more than 100 m are possible.

Because of timing restrictions, it is not allowed to connect more than two repeaters in series. It is possible, however, to use several repeaters in parallel as long as they are connected to different branches of the tree structure of the network.

#### 5.4.4 AS-i earth-fault detector

**A1)** In accordance with IEC 60204-1, insulation faults on any control circuit shall not cause unintentional starting, potentially hazardous motions or prevent stopping of the machine. To fulfil this requirement, IEC 60204-1 indicates that control circuits that are not connected to the protective bonding circuit shall be provided with an insulation monitoring device that either interrupts the circuit automatically after detecting an earth fault or indicates an earth fault to initiate a signalling at the machine.

If an AS-i network is used to control potentially dangerous movements of a machine and IEC 60204-1 applies, an insulation monitoring device shall be installed. If the AS-i network is composed of separate parts that are isolated from each other, an insulation monitoring device shall be used for each isolated part of the network. **A1)**

The insulation monitoring device used in AS-i networks shall be compatible with the requirements of the AS-i transmission system. Details are given in 8.3.2.

### 5.5 Communication

#### 5.5.1 Communication principles

The AS-i system is a master-slave communication system composed of a single master and up to 31 (62 with extended addressing) slaves. Each slave shall have a unique address in the range of 1 to 31 (1A/1B to 31A/31B with extended addressing). This address is called operation address. The operation address shall be stored non-volatile. Only slaves with an operation address shall respond to data and parameter requests from the master.

The zero address is used during the change of a slave address. Normally, the zero address is stored volatile, except in factory new slaves. For details see 8.4.

A single transaction is composed of a master request and a slave response. A combined transaction is composed of several single transactions.

#### 5.5.2 Transmission control

The exchange of data between the single master and up to 31 (62 with extended addressing) slaves is implemented by the processing of transactions (see Figure 7). A transaction starts with a master request. The master expects a slave response within a certain time. If the master does not receive a valid response from the slave within this time, it shall interpret this as a negative response. It may retransmit the master request once more. After receiving a valid response, the master shall start the next transaction after the send pause has elapsed. A slave shall not respond if it detects a faulty master request or if the master issues an unsupported request. The slave shall not give any negative response.

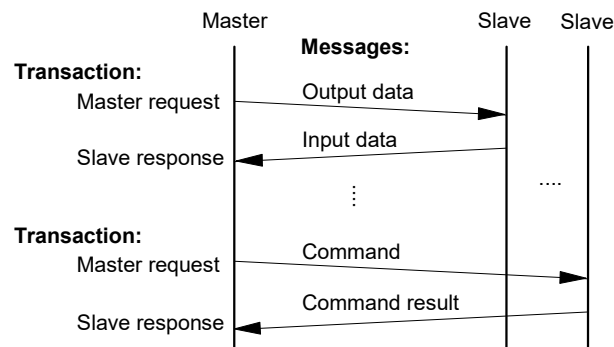


Figure 7 – Transactions

### 5.5.3 Timing requirements

All times specified in this paragraph are related to the signals on the AS-i line at the location of the master terminals.

An example of how to measure the master pause is shown in Figure 9. Other pauses shall be measured respectively. Both the master request and the slave response start with a zero as the first bit. Due to the Manchester II format this start bit leads only to a negative voltage pulse in the second half of the first bit time.

NOTE 1 Each receiver samples the voltage pulses with a certain threshold value. Therefore, and due to analogue filters, the start of the internal bit times may vary from those shown in Figure 9.

NOTE 2 The “master pause” is controlled by the slave and the “slave pause” is controlled by the master. These names, although illogical, are maintained for historical reasons.

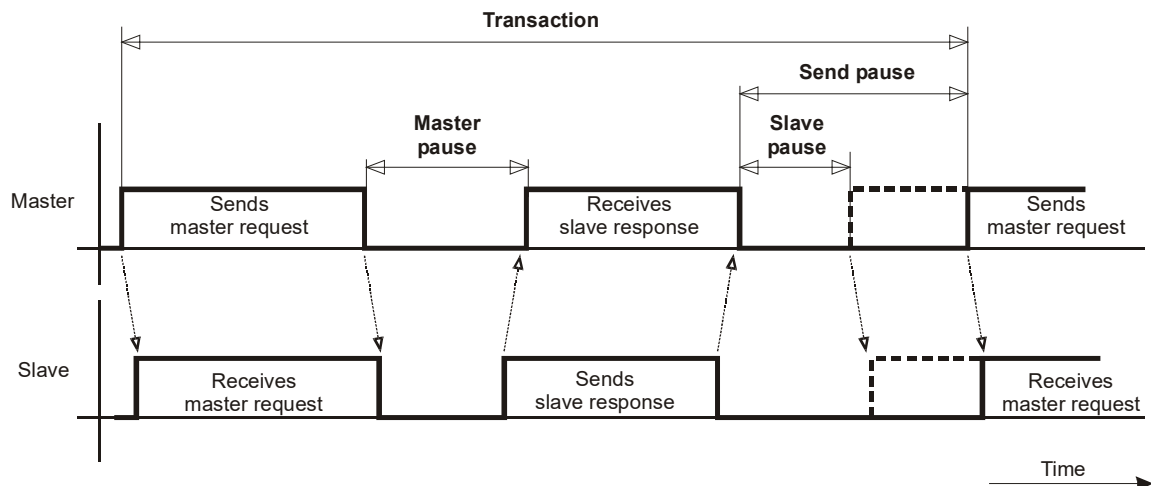


Figure 8 – Master and slave pause as viewed from master/slave point of view

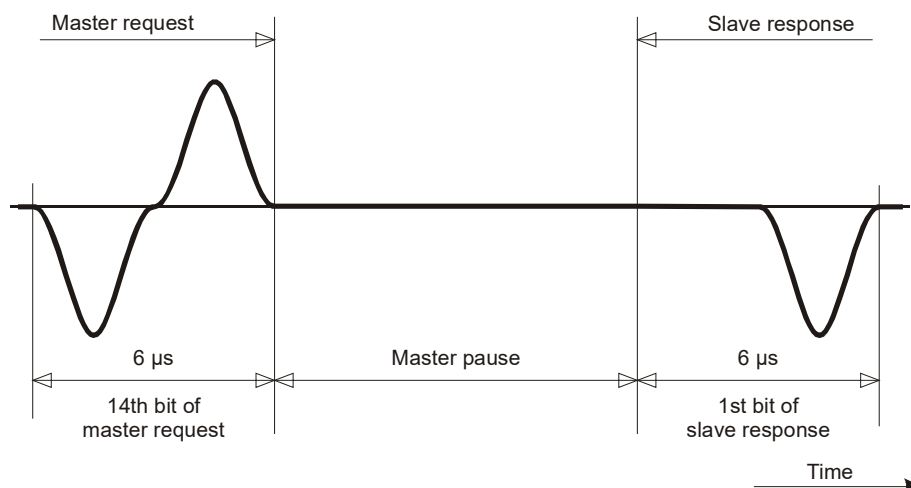


**Figure 9 – Representation of the master pause**

A transaction is split into two actions (master request and slave response) and two time intervals (master pause and send pause). A slave response time-out monitors a possible absence of a slave response:

1. **Master request:** sending a message from the master to a single slave and expecting a response from the slave.
2. **Master pause:** During this time the slave processes the requested function, produces the response data and starts within this time to send the response to the master. If a slave responds to a master request, it shall start its response within a period of 2 to 5 bit times after the end of a master request. The master shall be able to accept the start of a slave response within a period of 12 to 63 μs after the end of its request.

NOTE 3 For optimized noise suppression the AS-i master receiver should be switched off during the master pause for  $\geq 1,5$  bit times.

3. **Slave response:** Sending the slave data or the command result to the master.
4. **Slave pause:** After receipt of the slave response there shall be a minimum period during which a subsequent transmission shall not occur. The duration of this pause shall be 1,5 to 2 bit times. The slave shall be able to accept the start of a master request after a slave pause of 6 μs.
5. **Send pause:** After receipt of the slave response there shall be a minimum period during which a subsequent transmission does not occur. During normal operation the time of this pause shall be one slave pause in case of more than 30 transactions per AS-i cycle. In the case of 30 or less transactions per AS-i cycle the send pause may be prolonged to a maximum of 500 μs; but in this case the AS-i cycle time shall not be longer than 5 ms, including management and inclusion phase.
6. **Slave response time-out:** In case of no response from the slave in a certain time interval (the slave response time-out), the master shall end the transaction or repeat the transmission. This time shall be 11 bit times  $\frac{+0 \mu s}{-3 \mu s}$ .

NOTE 4 This is with respect to propagation delay on the line and the possible use of repeaters.

The time-out timer shall be started at the end of the transmission of the master request.

NOTE 5 Within the slave response time-out the master expects the beginning of a response telegram from the slave. After this time, the transmission function determines the absence of a slave response.

7. **Delay time for repeater:** The maximum delay time for a repeater shall be less than or equal to 7 μs for each direction.

NOTE 6 The master pause has to be less than or equal to 63  $\mu$ s (see slave response time out). In the case of two repeaters in series, an asynchronous slave behind the second repeater and a propagation delay time of a 300 m line of about 5  $\mu$ s appears. The maximum delay time for one repeater is 7  $\mu$ s for each direction. The delay time of a repeater is to be measured as the time between a certain incoming voltage pulse to the respective outgoing voltage pulse on the other line.

NOTE 7 With presently available components, a stated AS-i cycle time shall be calculated as follows:

$$\begin{array}{rclclcl}
 & & & & & \text{If } n = 33 & \\
 n * \text{Master request} & = & n * (14 \text{ Bit}) & = & n * 84 \mu\text{s} & = & 2\,772 \mu\text{s} \\
 + n * \text{Master pause} & = & n * (3 \text{ Bit}) & = & n * 16 \mu\text{s (synchr. slave)} & = & 528 \mu\text{s} \\
 + n * \text{Slave response} & = & n * (7 \text{ Bit}) & = & n * 42 \mu\text{s} & = & 1\,386 \mu\text{s} \\
 + n * \text{Send pause} & = & n * (2 \text{ Bit}) & = & n * 12 \mu\text{s (min.)} & = & 396 \mu\text{s} \\
 \hline
 = T_{\text{cycle}} & = & n * (26 \text{ Bit}) & = & n * 154 \mu\text{s (min.)} & = & 5\,082 \mu\text{s}
 \end{array}$$

where  $n$  is the number of all AS-i requests during data exchange in the AS-i cycle and in the inclusion phase, including one repetition. In normal operation,  $n$  will be the number of activated slaves plus 2. This calculation is not affected by use of up to 62 slaves in extended addressing mode.

## 5.6 AS-i single transactions

### 5.6.1 Summary of transactions

Four single transaction types support data exchange, parametrization, network management and diagnostics. All master requests and all slave responses have the same structure and the same length of 14 bits (master) and 7 bits (slave), respectively.

A master may be able to issue all or some of the master requests listed in Tables 4 and 5 to start a transaction. Any slave shall be able to process and respond to all those master requests with the possible exception of the Address\_Assignment request and R1 request. (For details see Annex B, AS-i Master Profiles).

### 5.6.2 Definition of master requests

The following types of master requests are defined:

**Data\_Exchange** Serves for delivering and/or receiving the bit pattern to/from the data output/input of the slave.

**Write\_Parameter** Serves for delivering and/or receiving the bit pattern to/from the parameter ports of the slave.

**Address\_Assignment** Serves for assigning a non-volatile address (0...31 for standard addressing mode / 0,1A/1B,...31A/31B for extended addressing mode) to the slave with a zero address.

**Commands** Serve for miscellaneous functions like reset, reading the configuration, and reading the status of the slave.

A summary of all master requests is given in Tables 4 and 5. All other possible codes (not yet used in this standard) are reserved and shall not be implemented by any master or slave implementation used for AS-i networks.

### 5.6.3 Structure and semantics of the master requests

The requests sent by the master and received by the slave are composed of six elements as follows:

|           |             |         |             |            |         |
|-----------|-------------|---------|-------------|------------|---------|
| Start bit | Control bit | Address | Information | Parity bit | End bit |
|-----------|-------------|---------|-------------|------------|---------|

The bits of a master request shall be as follows:

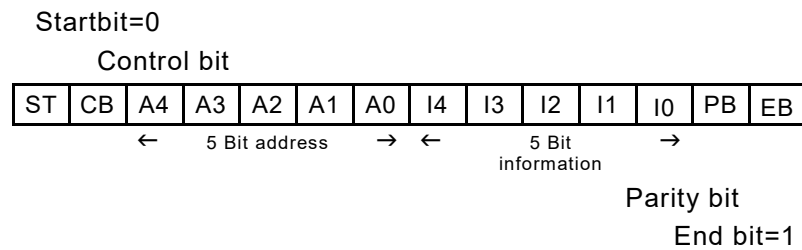


**Figure 10 – Structure of a master request**

**Table 3 – Bit strings of the master requests**

| Bit string | Semantic        | Comments                                                                                                                                                                                                                                                                                                                             |
|------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ST:        | Start bit       | Identifies the beginning of the master request always: ST = 0                                                                                                                                                                                                                                                                        |
| CB:        | Control bit     | Identifies the type of request in the information cell;<br>0 = data/parameter transmission/address assignment;<br>1 = command transmission                                                                                                                                                                                           |
| A4..A0:    | Address (5 bit) | To address the listed slaves<br>00 <sub>Hex</sub> = zero address.<br>01 <sub>Hex</sub> .. 1F <sub>Hex</sub> = slave 1 through 31                                                                                                                                                                                                     |
| I4..I0:    | INFORMATION     | These 5 bits contain the information to be transferred to the slave for every request type. Individual bits are described by the respective call type.<br><br>For extended addressing I3 is used as an address extension (Sel-bit) to address the A- and B-slaves.<br><br>Definition of Sel-bit:      Sel=0 A-slave<br>Sel=1 B-slave |
| PB:        | Parity bit      | Part of verification of the correctness of the master request at the slave. A correct message has even parity.<br><br>0 = even count of "1"-symbols in (CB, A4..A0, I4..I0)<br>1 = odd count of the "1"-symbols in (CB, A4..A0, I4..I0)                                                                                              |
| EB:        | End bit         | Identifies the end of the master request always: EB = 1                                                                                                                                                                                                                                                                              |

**Table 4 – Master requests (standard addressing mode)**

|                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    |                       |    |      |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|-----------------------|----|------|------|------|------|----|----|--|----|----|----|----|----|----|----|----|----|------|------|------|------|----|----|-------------------|--|--|--|--|--|-----------------------|--|--|--|--|--|--|--|
| Data_Exchange            | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=0</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>PB</td><td>=1</td></tr><tr><td colspan="6">← 5 Bit Address →</td><td colspan="6">← 5 Bit Information →</td><td colspan="2"></td></tr></table>         | ST | CB |    |    |                       |    |      | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =0 | A4 | A3 | A2 | A1 | A0 | =0 | D3   | D2   | D1   | D0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                              |    |    |    |    |                       | I4 | I3   | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| =0                       | =0                                                                                                                                                                                                                                                                                                                                                                                                                                                              | A4 | A3 | A2 | A1 | A0                    | =0 | D3   | D2   | D1   | D0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    | ← 5 Bit Information → |    |      |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| Write_Parameter          | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td>P3</td><td>P2</td><td>P1</td><td>P0</td><td>PB</td><td>=1</td></tr><tr><td colspan="6">← 5 Bit Address →</td><td colspan="6">← 5 Bit Information →</td><td colspan="2"></td></tr></table>         | ST | CB |    |    |                       |    |      | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =0 | A4 | A3 | A2 | A1 | A0 | =1 | P3   | P2   | P1   | P0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                              |    |    |    |    |                       | I4 | I3   | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| =0                       | =0                                                                                                                                                                                                                                                                                                                                                                                                                                                              | A4 | A3 | A2 | A1 | A0                    | =1 | P3   | P2   | P1   | P0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    | ← 5 Bit Information → |    |      |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| Address_Assignment       | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>PB</td><td>=1</td></tr><tr><td colspan="6">← 5 Bit Address →</td><td colspan="6">← 5 Bit Information →</td><td colspan="2"></td></tr></table>         | ST | CB |    |    |                       |    |      | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =0 | =0 | =0 | =0 | =0 | =0 | A4 | A3   | A2   | A1   | A0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                              |    |    |    |    |                       | I4 | I3   | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| =0                       | =0                                                                                                                                                                                                                                                                                                                                                                                                                                                              | =0 | =0 | =0 | =0 | =0                    | A4 | A3   | A2   | A1   | A0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    | ← 5 Bit Information → |    |      |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| Write_Extended_ID-Code_1 | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>ID 3</td><td>ID 2</td><td>ID 1</td><td>ID 0</td><td>PB</td><td>=1</td></tr><tr><td colspan="6">← 5 Bit Address →</td><td colspan="6">← 5 Bit Information →</td><td colspan="2"></td></tr></table> | ST | CB |    |    |                       |    |      | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | =0 | =0 | =0 | =0 | =0 | =0 | ID 3 | ID 2 | ID 1 | ID 0 | PB | =1 | ← 5 Bit Address → |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                              |    |    |    |    |                       | I4 | I3   | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                              | =0 | =0 | =0 | =0 | =0                    | =0 | ID 3 | ID 2 | ID 1 | ID 0 | PB | =1 |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    | ← 5 Bit Information → |    |      |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| Delete_Address           | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>PB</td><td>=1</td></tr><tr><td colspan="6">← 5 Bit Address →</td><td colspan="6">← 5 Bit Information →</td><td colspan="2"></td></tr></table>         | ST | CB |    |    |                       |    |      | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =0 | =0   | =0   | =0   | =0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                              |    |    |    |    |                       | I4 | I3   | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                              | A4 | A3 | A2 | A1 | A0                    | =0 | =0   | =0   | =0   | =0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    | ← 5 Bit Information → |    |      |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| Reset_Slave              | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td>=1</td><td>=1</td><td>=0</td><td>=0</td><td>PB</td><td>=1</td></tr><tr><td colspan="6">← 5 Bit Address →</td><td colspan="6">← 5 Bit Information →</td><td colspan="2"></td></tr></table>         | ST | CB |    |    |                       |    |      | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =1 | =1   | =1   | =0   | =0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                              |    |    |    |    |                       | I4 | I3   | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                              | A4 | A3 | A2 | A1 | A0                    | =1 | =1   | =1   | =0   | =0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    | ← 5 Bit Information → |    |      |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| Read_I/O-Configuration   | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>PB</td><td>=1</td></tr><tr><td colspan="6">← 5 Bit Address →</td><td colspan="6">← 5 Bit Information →</td><td colspan="2"></td></tr></table>         | ST | CB |    |    |                       |    |      | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =1 | =0   | =0   | =0   | =0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                              |    |    |    |    |                       | I4 | I3   | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                              | A4 | A3 | A2 | A1 | A0                    | =1 | =0   | =0   | =0   | =0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    | ← 5 Bit Information → |    |      |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| Read_ID-Code             | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td>=0</td><td>=0</td><td>=0</td><td>=1</td><td>PB</td><td>=1</td></tr><tr><td colspan="6">← 5 Bit Address →</td><td colspan="6">← 5 Bit Information →</td><td colspan="2"></td></tr></table>         | ST | CB |    |    |                       |    |      | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =1 | =0   | =0   | =0   | =1   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                              |    |    |    |    |                       | I4 | I3   | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                              | A4 | A3 | A2 | A1 | A0                    | =1 | =0   | =0   | =0   | =1   | PB | =1 |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    | ← 5 Bit Information → |    |      |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| Read_Extended_ID-Code_1  | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td>=0</td><td>=0</td><td>=1</td><td>=0</td><td>PB</td><td>=1</td></tr><tr><td colspan="6">← 5 Bit Address →</td><td colspan="6">← 5 Bit Information →</td><td colspan="2"></td></tr></table>         | ST | CB |    |    |                       |    |      | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =1 | =0   | =0   | =1   | =0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                              |    |    |    |    |                       | I4 | I3   | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                              | A4 | A3 | A2 | A1 | A0                    | =1 | =0   | =0   | =1   | =0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    | ← 5 Bit Information → |    |      |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| Read_Extended_ID-Code_2  | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td>=0</td><td>=0</td><td>=1</td><td>=1</td><td>PB</td><td>=1</td></tr><tr><td colspan="6">← 5 Bit Address →</td><td colspan="6">← 5 Bit Information →</td><td colspan="2"></td></tr></table>         | ST | CB |    |    |                       |    |      | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =1 | =0   | =0   | =1   | =1   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                              |    |    |    |    |                       | I4 | I3   | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                              | A4 | A3 | A2 | A1 | A0                    | =1 | =0   | =0   | =1   | =1   | PB | =1 |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    | ← 5 Bit Information → |    |      |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| Read_Status              | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td>=1</td><td>=1</td><td>=1</td><td>=0</td><td>PB</td><td>=1</td></tr><tr><td colspan="6">← 5 Bit Address →</td><td colspan="6">← 5 Bit Information →</td><td colspan="2"></td></tr></table>         | ST | CB |    |    |                       |    |      | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =1 | =1   | =1   | =1   | =0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                              |    |    |    |    |                       | I4 | I3   | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                              | A4 | A3 | A2 | A1 | A0                    | =1 | =1   | =1   | =1   | =0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    | ← 5 Bit Information → |    |      |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| R1                       | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td>=1</td><td>=1</td><td>=1</td><td>=1</td><td>PB</td><td>=1</td></tr><tr><td colspan="6">← 5 Bit Address →</td><td colspan="6">← 5 Bit Information →</td><td colspan="2"></td></tr></table>         | ST | CB |    |    |                       |    |      | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =1 | =1   | =1   | =1   | =1   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                              |    |    |    |    |                       | I4 | I3   | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                              | A4 | A3 | A2 | A1 | A0                    | =1 | =1   | =1   | =1   | =1   | PB | =1 |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    | ← 5 Bit Information → |    |      |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| Broadcast                | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>=1</td><td>=1</td><td>=1</td><td>=1</td><td>=1</td><td>=1</td><td>=0</td><td>=1</td><td>=0</td><td>=1</td><td>PB</td><td>=1</td></tr><tr><td colspan="6">← 5 Bit Address →</td><td colspan="6">← 5 Bit Information →</td><td colspan="2"></td></tr></table>         | ST | CB |    |    |                       |    |      | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | =1 | =1 | =1 | =1 | =1 | =1 | =0   | =1   | =0   | =1   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                              |    |    |    |    |                       | I4 | I3   | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                              | =1 | =1 | =1 | =1 | =1                    | =1 | =0   | =1   | =0   | =1   | PB | =1 |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    | ← 5 Bit Information → |    |      |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |      |      |      |      |    |    |                   |  |  |  |  |  |                       |  |  |  |  |  |  |  |

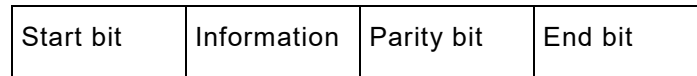
**Table 5 – Master requests in the extended addressing mode**

|                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |    |    |    |    |    |                       |                         |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|-----------------------|-------------------------|------|------|------|----|----|--|----|----|----|----|----|----|----|----|----|-------------------------|------|------|------|----|----|-------------------|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|
| Data_Exchange            | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=0</td><td><math>\overline{\text{Sel}}</math></td><td>D2</td><td>D1</td><td>D0</td><td>PB</td><td>=1</td></tr><tr><td colspan="7">← 5 Bit Address →</td><td colspan="7">← 5 Bit Information →</td></tr></table> | ST | CB |    |    |    |                       |                         | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =0 | A4 | A3 | A2 | A1 | A0 | =0 | $\overline{\text{Sel}}$ | D2   | D1   | D0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    |    | I4                    | I3                      | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| =0                       | =0                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | A4 | A3 | A2 | A1 | A0 | =0                    | $\overline{\text{Sel}}$ | D2   | D1   | D0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |    |    |    |    |    | ← 5 Bit Information → |                         |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| Write_Parameter          | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td><math>\overline{\text{Sel}}</math></td><td>P2</td><td>P1</td><td>P0</td><td>PB</td><td>=1</td></tr><tr><td colspan="7">← 5 Bit Address →</td><td colspan="7">← 5 Bit Information →</td></tr></table> | ST | CB |    |    |    |                       |                         | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =0 | A4 | A3 | A2 | A1 | A0 | =1 | $\overline{\text{Sel}}$ | P2   | P1   | P0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    |    | I4                    | I3                      | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| =0                       | =0                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | A4 | A3 | A2 | A1 | A0 | =1                    | $\overline{\text{Sel}}$ | P2   | P1   | P0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |    |    |    |    |    | ← 5 Bit Information → |                         |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| Address_Assignment       | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>PB</td><td>=1</td></tr><tr><td colspan="7">← 5 Bit Address →</td><td colspan="7">← 5 Bit Information →</td></tr></table>                                 | ST | CB |    |    |    |                       |                         | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =0 | =0 | =0 | =0 | =0 | =0 | A4 | A3                      | A2   | A1   | A0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    |    | I4                    | I3                      | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| =0                       | =0                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | =0 | =0 | =0 | =0 | =0 | A4                    | A3                      | A2   | A1   | A0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |    |    |    |    |    | ← 5 Bit Information → |                         |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| Write_Extended_ID-Code_1 | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>=0</td><td>ID 3</td><td>ID 2</td><td>ID 1</td><td>ID 0</td><td>PB</td><td>=1</td></tr><tr><td colspan="7">← 5 Bit Address →</td><td colspan="7">← 5 Bit Information →</td></tr></table>                         | ST | CB |    |    |    |                       |                         | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | =0 | =0 | =0 | =0 | =0 | =0 | ID 3                    | ID 2 | ID 1 | ID 0 | PB | =1 | ← 5 Bit Address → |  |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    |    | I4                    | I3                      | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | =0 | =0 | =0 | =0 | =0 | =0                    | ID 3                    | ID 2 | ID 1 | ID 0 | PB | =1 |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |    |    |    |    |    | ← 5 Bit Information → |                         |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| Delete_Address           | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=0</td><td><math>\overline{\text{Sel}}</math></td><td>=0</td><td>=0</td><td>=0</td><td>PB</td><td>=1</td></tr><tr><td colspan="7">← 5 Bit Address →</td><td colspan="7">← 5 Bit Information →</td></tr></table> | ST | CB |    |    |    |                       |                         | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =0 | $\overline{\text{Sel}}$ | =0   | =0   | =0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    |    | I4                    | I3                      | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | A4 | A3 | A2 | A1 | A0 | =0                    | $\overline{\text{Sel}}$ | =0   | =0   | =0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |    |    |    |    |    | ← 5 Bit Information → |                         |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| Reset_Slave              | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td><math>\overline{\text{Sel}}</math></td><td>=1</td><td>=0</td><td>=0</td><td>PB</td><td>=1</td></tr><tr><td colspan="7">← 5 Bit Address →</td><td colspan="7">← 5 Bit Information →</td></tr></table> | ST | CB |    |    |    |                       |                         | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =1 | $\overline{\text{Sel}}$ | =1   | =0   | =0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    |    | I4                    | I3                      | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | A4 | A3 | A2 | A1 | A0 | =1                    | $\overline{\text{Sel}}$ | =1   | =0   | =0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |    |    |    |    |    | ← 5 Bit Information → |                         |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| Read_I/O-Configuration   | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td><math>\overline{\text{Sel}}</math></td><td>=0</td><td>=0</td><td>=0</td><td>PB</td><td>=1</td></tr><tr><td colspan="7">← 5 Bit Address →</td><td colspan="7">← 5 Bit Information →</td></tr></table> | ST | CB |    |    |    |                       |                         | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =1 | $\overline{\text{Sel}}$ | =0   | =0   | =0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    |    | I4                    | I3                      | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | A4 | A3 | A2 | A1 | A0 | =1                    | $\overline{\text{Sel}}$ | =0   | =0   | =0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |    |    |    |    |    | ← 5 Bit Information → |                         |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| Read_ID-Code             | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td><math>\overline{\text{Sel}}</math></td><td>=0</td><td>=0</td><td>=1</td><td>PB</td><td>=1</td></tr><tr><td colspan="7">← 5 Bit Address →</td><td colspan="7">← 5 Bit Information →</td></tr></table> | ST | CB |    |    |    |                       |                         | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =1 | $\overline{\text{Sel}}$ | =0   | =0   | =1   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    |    | I4                    | I3                      | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | A4 | A3 | A2 | A1 | A0 | =1                    | $\overline{\text{Sel}}$ | =0   | =0   | =1   | PB | =1 |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |    |    |    |    |    | ← 5 Bit Information → |                         |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| Read_Extended_ID-Code_1  | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td><math>\overline{\text{Sel}}</math></td><td>=0</td><td>=1</td><td>=0</td><td>PB</td><td>=1</td></tr><tr><td colspan="7">← 5 Bit Address →</td><td colspan="7">← 5 Bit Information →</td></tr></table> | ST | CB |    |    |    |                       |                         | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =1 | $\overline{\text{Sel}}$ | =0   | =1   | =0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    |    | I4                    | I3                      | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | A4 | A3 | A2 | A1 | A0 | =1                    | $\overline{\text{Sel}}$ | =0   | =1   | =0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |    |    |    |    |    | ← 5 Bit Information → |                         |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| Read_Extended_ID-Code_2  | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td><math>\overline{\text{Sel}}</math></td><td>=0</td><td>=1</td><td>=1</td><td>PB</td><td>=1</td></tr><tr><td colspan="7">← 5 Bit Address →</td><td colspan="7">← 5 Bit Information →</td></tr></table> | ST | CB |    |    |    |                       |                         | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =1 | $\overline{\text{Sel}}$ | =0   | =1   | =1   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    |    | I4                    | I3                      | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | A4 | A3 | A2 | A1 | A0 | =1                    | $\overline{\text{Sel}}$ | =0   | =1   | =1   | PB | =1 |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |    |    |    |    |    | ← 5 Bit Information → |                         |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| Read_Status              | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td><math>\overline{\text{Sel}}</math></td><td>=1</td><td>=1</td><td>=0</td><td>PB</td><td>=1</td></tr><tr><td colspan="7">← 5 Bit Address →</td><td colspan="7">← 5 Bit Information →</td></tr></table> | ST | CB |    |    |    |                       |                         | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =1 | $\overline{\text{Sel}}$ | =1   | =1   | =0   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    |    | I4                    | I3                      | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | A4 | A3 | A2 | A1 | A0 | =1                    | $\overline{\text{Sel}}$ | =1   | =1   | =0   | PB | =1 |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |    |    |    |    |    | ← 5 Bit Information → |                         |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| R1                       | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>=1</td><td><math>\overline{\text{Sel}}</math></td><td>=1</td><td>=1</td><td>=1</td><td>PB</td><td>=1</td></tr><tr><td colspan="7">← 5 Bit Address →</td><td colspan="7">← 5 Bit Information →</td></tr></table> | ST | CB |    |    |    |                       |                         | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | A4 | A3 | A2 | A1 | A0 | =1 | $\overline{\text{Sel}}$ | =1   | =1   | =1   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    |    | I4                    | I3                      | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | A4 | A3 | A2 | A1 | A0 | =1                    | $\overline{\text{Sel}}$ | =1   | =1   | =1   | PB | =1 |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |    |    |    |    |    | ← 5 Bit Information → |                         |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| Broadcast                | <table><tr><td>ST</td><td>CB</td><td></td><td></td><td></td><td></td><td></td><td>I4</td><td>I3</td><td>I2</td><td>I1</td><td>I0</td><td></td><td>EB</td></tr><tr><td>=0</td><td>=1</td><td>=1</td><td>=1</td><td>=1</td><td>=1</td><td>=1</td><td>=1</td><td>=0</td><td>=1</td><td>=0</td><td>=1</td><td>PB</td><td>=1</td></tr><tr><td colspan="7">← 5 Bit Address →</td><td colspan="7">← 5 Bit Information →</td></tr></table>                                 | ST | CB |    |    |    |                       |                         | I4   | I3   | I2   | I1 | I0 |  | EB | =0 | =1 | =1 | =1 | =1 | =1 | =1 | =1 | =0                      | =1   | =0   | =1   | PB | =1 | ← 5 Bit Address → |  |  |  |  |  |  | ← 5 Bit Information → |  |  |  |  |  |  |
| ST                       | CB                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    |    | I4                    | I3                      | I2   | I1   | I0   |    | EB |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| =0                       | =1                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | =1 | =1 | =1 | =1 | =1 | =1                    | =0                      | =1   | =0   | =1   | PB | =1 |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |
| ← 5 Bit Address →        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |    |    |    |    |    | ← 5 Bit Information → |                         |      |      |      |    |    |  |    |    |    |    |    |    |    |    |    |                         |      |      |      |    |    |                   |  |  |  |  |  |  |                       |  |  |  |  |  |  |

NOTE Sel denotes the Select Bit,  $\overline{\text{Sel}}$  the inverted Select Bit.

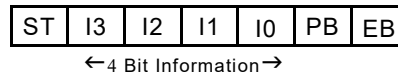
#### 5.6.4 Structure and semantics of the slave responses

The responses sent by the slave have no control bit and no address and are composed of 4 elements as follows:



The bits of a slave response shall be as follows:

Start bit=0



Parity bit

End bit=1

**Figure 11 – Structure of a slave response**

**Table 6 – Bit strings of the slave responses**

| Bit string | Semantic    | Comments                                                                                                                                                                                          |
|------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ST:        | Start bit   | Identifies the beginning of the slave response always: ST = 0                                                                                                                                     |
| I3..I0:    | Information | These 4 bits contain the information to be transferred to the master for every response type. Individual bits are described by the respective call type                                           |
| PB:        | Parity bit  | Part of verification of the correctness of the slave response. Each correct message has even parity.<br>0 = even count of "1"-symbols in (I3..I0)<br>1 = odd count of the "1"-symbols in (I3..I0) |
| EB:        | End bit     | Identifies the end of the slave response always: EB = 1                                                                                                                                           |

#### 5.6.5 Individual single transactions

##### 5.6.5.1 Data\_Exchange

The "Data\_Exchange Request" shall be used by the master to transfer 4 bits of data (I3..I0) (3 bits of data plus Sel-Bit in case of extended addressing mode) to the data output register of the slave and to obtain 4 bits of data from the slave inputs. (For the behaviour of the input/output ports of the slave see 8.4).

The data exchange request shall have the following structure:

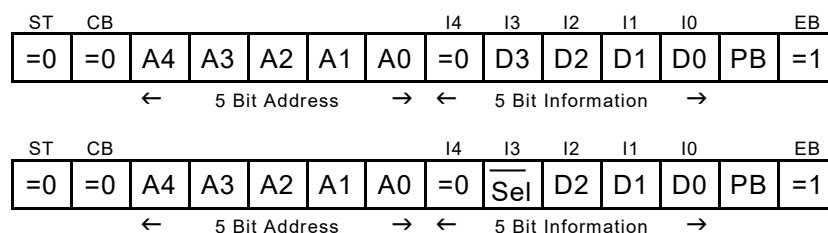


**Figure 12 – Structure of a data exchange request (top: standard address mode; bottom: extended address mode)**

The bits A4..A0 shall contain an operation address (1..31).

The slave response shall have the following structure:

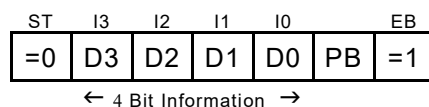


**Figure 13 – Structure of the slave response (Data\_Exchange)**

If the slave is not activated, no answer shall be generated.

#### 5.6.5.2 Write\_Parameter

The "Write\_Parameter Request" shall be used by the master to transfer the 4 parameter bits (I3..I0) to the parameter output register of the slave and to obtain 4 bits of data from the slave parameter inputs. (For the behaviour of the parameter input/output ports of the slave see 8.4).

The Write\_Parameter request shall have the following structure:

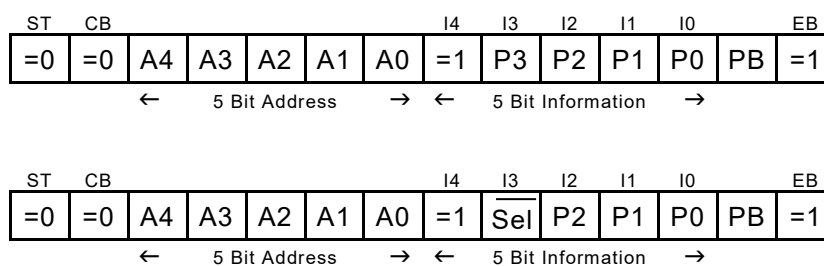


**Figure 14 – Structure of the Write\_Parameter request (top: standard addressing mode; bottom: extended addressing mode)**

The bits A4..A0 shall contain an operation address (1..31).

The slave response shall have the following structure:

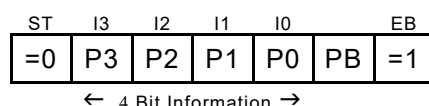


**Figure 15 – Structure of the slave response (Write\_Parameter)**

The Write\_Parameter request may affect the slave's state machine (see 8.4 for further details).

#### 5.6.5.3 Address\_Assignment

The "Address\_Assignment request" shall be used by the master to enforce the slave to store the given address (I4..I0) non-volatile and to use this address when responding to master requests.

The address\_assignment request shall have the following structure:

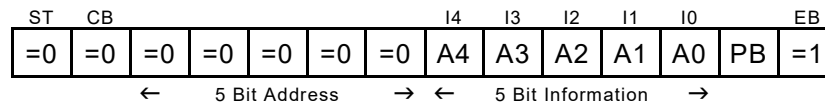


**Figure 16 – Structure of the Address\_Assignment request**

The bits A4..A0 shall contain the zero address (00<sub>Hex</sub>).

The slave response shall have the following structure:

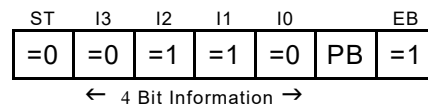


**Figure 17 – Structure of the slave response (Address\_Assignment)**

After a successful Address\_Assignment, a slave shall respond under the new address.

#### 5.6.5.4 Write\_Extended\_ID-Code\_1

The "Write\_Extended\_ID-Code\_1" request is a command request and shall be used by the master to write the variable ID-Code nibble of the slave with address =0.

The "Write\_Extended\_ID-Code\_1" command shall have the following structure:

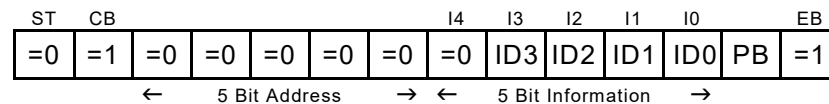


**Figure 18 – Structure of the Write\_Extended\_ID-Code\_1 request**

For compatibility reasons with previous versions of this standard the response of a slave to this command is optional. After a successful Write\_Extended\_ID-Code\_1 command, the slave response shall have the following structure:

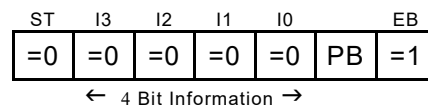


**Figure 19 – Structure of the slave response (Write\_Extended\_ID-Code\_1)**

The new ID-Code nibble shall be stored non-volatile.

In extended addressing mode it is permitted for the manufacturer to block the write access by the user to the extended ID-Code 1. This allows to distinguish between more specific products. The manufacturer shall set all bits of the blocked extended ID Code 1 to "1" or as it is defined in the profile. Some ID-Code 1 may be fixed in specific profiles. In case of ID\_Code2=F<sub>Hex</sub> and ID\_Code1=F<sub>Hex</sub> the ID-Code 1 may be blocked by the manufacturer.

**NOTE 1** If the slave is in the process of storing the new ID-Code nibble into the non-volatile memory (processing the "Write\_Extended\_ID-Code\_1" request), a new "Write\_Extended\_ID-Code\_1" request should not be issued by the master. The result of the storage process would otherwise be undefined.

**NOTE 2** If the slave is used in Extended Address Mode ID3 is used as SEL to select A and B address. In this mode the user programmable part of the Extended ID-Code\_1 (ID2..ID0) is limited to the range of 0 to 7.

### 5.6.5.5 Reset\_Slave

The "Reset\_Slave request" is a command request and shall be used by the master to reset a specific slave.

The Reset\_Slave command shall have the following structure:

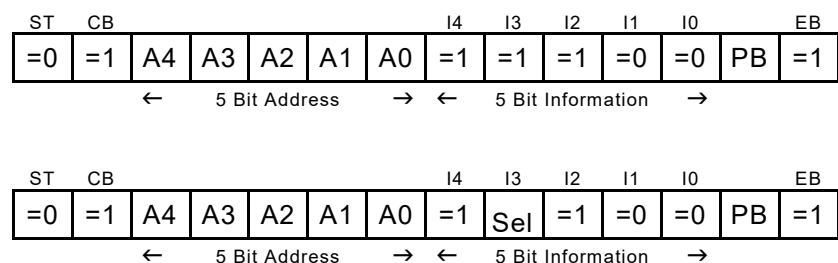


**Figure 20 – Structure of the Reset\_Slave request (top: standard addressing mode; bottom: extended addressing mode)**

The slave response shall have the following structure:

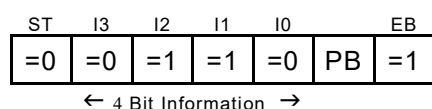


**Figure 21 – Structure of the slave response (Reset\_Slave)**

The Reset\_Slave request affects the slave's state machine. (See 8.4 for further details).

### 5.6.5.6 Delete\_Address

The "Delete\_Address request" is a command request and shall be used by the master to delete the operation address of a specific slave.

The Delete\_Address command shall have the following structure:

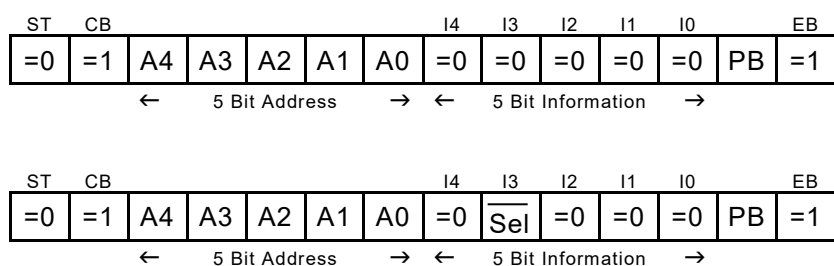


**Figure 22 – Structure of the Delete\_Address request (top: standard addressing mode; bottom: extended addressing mode)**

The slave response shall have the following structure:

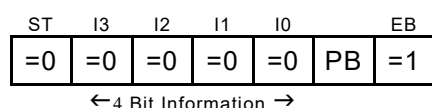


**Figure 23 – Structure of the slave response (Delete\_Address)**

After a successful Delete\_Address command, a slave shall respond with the zero address. This request does not cause the slave to store the address non-volatile.

The Delete\_Address request does not affect the slave's state machine.

NOTE 1 A "Delete\_Address" request to a slave with a zero address is identical to the "Write\_Extended\_ID-Code\_1" request (see 5.6.5.4).

NOTE 2 If the slave is in the process of storing its address into the non-volatile memory (processing the "Address\_Assignment" request), a "Delete\_Address" request should not be issued by the master. The result of the storage process would be undefined.

### 5.6.5.7 Read\_I/O\_Configuration

The "Read\_I/O\_Configuration Request" is a command request and shall be used by the master to read the I/O configuration of a specific slave.

The Read\_I/O\_Configuration request shall have the following structure:

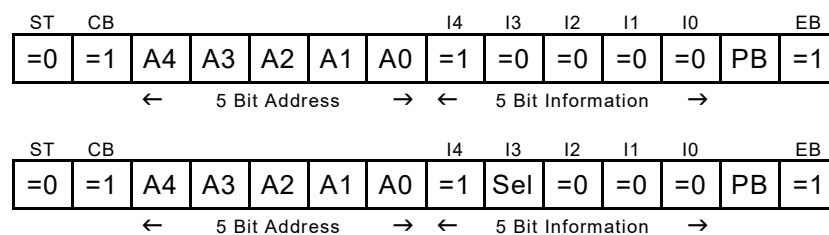


**Figure 24 – Structure of the Read\_I/O\_Configuration request**  
(top: standard addressing mode; bottom: extended addressing mode)

The slave response shall contain the I/O-Code and shall have the following structure:

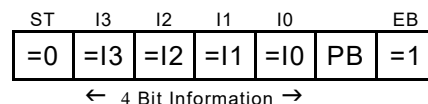


**Figure 25 – Structure of the slave response (Read\_I/O\_Configuration)**

The input/output data bits are configured to function as input only, as output only, as bi-directional input/output, or as tristate. This configuration depends on the environment and the required functionality. It is fixed for any particular slave, therefore. 16 different configurations as shown in Table 7 are defined. They are identified by the Identification Code, which shall be stored non-volatile in the slave.

The encoding of the I/O configuration shall be as follows:

NOTE 1 I/O configuration examples include:

- 4-bit input data to transmit the switching signals of 4 binary sensors,
- 4-bit output data to activate four actuators,
- 2-bit output plus 2-bit input to activate and monitor a double working actuator (e.g. bi-directional pneumatic valve that also transmits the sensor signals indicating the end positions).

**Table 7 – I/O Codes (IN = Input; OUT = Output; TRI = Tristate;  
I/O = Input/Output or Bidirectional (B))**

| I/O Code<br>(4-Bit) | I/O-Configuration |     |     |     |
|---------------------|-------------------|-----|-----|-----|
|                     | D0                | D1  | D2  | D3  |
| 0 <sub>Hex</sub>    | IN                | IN  | IN  | IN  |
| 1 <sub>Hex</sub>    | IN                | IN  | IN  | OUT |
| 2 <sub>Hex</sub>    | IN                | IN  | IN  | I/O |
| 3 <sub>Hex</sub>    | IN                | IN  | OUT | OUT |
| 4 <sub>Hex</sub>    | IN                | IN  | I/O | I/O |
| 5 <sub>Hex</sub>    | IN                | OUT | OUT | OUT |
| 6 <sub>Hex</sub>    | I/O               | I/O | I/O | I/O |
| 7 <sub>Hex</sub>    | I/O               | I/O | I/O | I/O |
| 8 <sub>Hex</sub>    | OUT               | OUT | OUT | OUT |
| 9 <sub>Hex</sub>    | OUT               | OUT | OUT | IN  |
| A <sub>Hex</sub>    | OUT               | OUT | OUT | I/O |
| B <sub>Hex</sub>    | OUT               | OUT | IN  | IN  |
| C <sub>Hex</sub>    | OUT               | OUT | I/O | I/O |
| D <sub>Hex</sub>    | OUT               | IN  | IN  | IN  |
| E <sub>Hex</sub>    | OUT               | I/O | I/O | I/O |
| F <sub>Hex</sub>    | TRI               | TRI | TRI | TRI |

NOTE 2 In previous versions of this standard, I/O code 6<sub>Hex</sub> was defined as IN I/O I/O I/O.

#### 5.6.5.8 Read\_Identification\_Code

The "Read\_Identification\_Code request" is a command request and shall be used by the master to read the identification code of a specific slave.

The Read\_Identification request shall have the following structure:

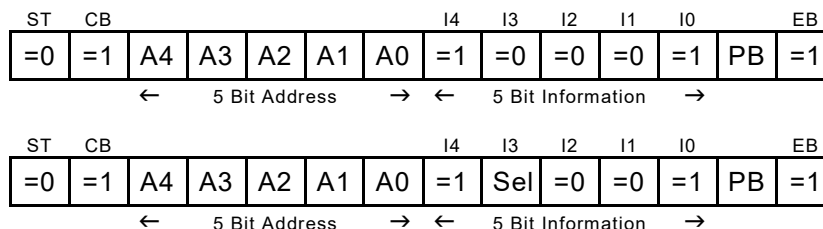


**Figure 26 – Structure of Read\_Identification\_Code request (top: standard addressing mode; bottom: extended addressing mode)**

The slave response shall contain the ID-Code and shall have the following structure:

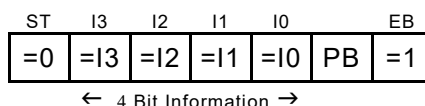


**Figure 27 – Structure of the slave response (Read\_Identification\_Code)**

If the Identification\_Code of a slave is "A<sub>Hex</sub>" the slave uses the extended addressing mode.

If the Identification\_Code of a slave is "B<sub>Hex</sub>" the slave transfers safe signals.

NOTE For further details, see Table 8 and Annex A.

### 5.6.5.9 Read\_Extended\_ID-Code\_1/2

The "Read\_Extended\_ID-Code\_1/2 Requests" are two command requests and shall be used by the master to read the content of the (optional) extended ID-Code register of a specific slave. These commands are optional.

The Read\_Extended\_ID-Code\_1/2 command request shall have the following structure:

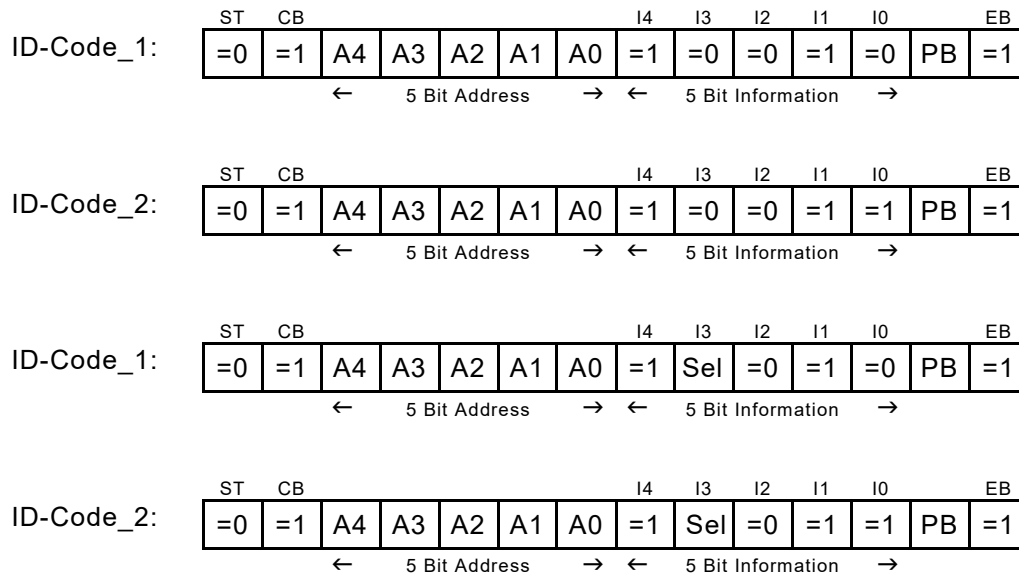


**Figure 28 – Structure of Read\_Extended\_ID-Code\_1/2 Request (top: standard addressing mode; bottom: extended addressing mode)**

The slave response shall have the following structure:

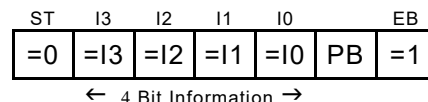


**Figure 29 – Structure of the slave response Read\_Extended\_ID-Code\_1/2**

**NOTE** If the slave is used in the Extended Address Mode I3 in the slave response to Read\_Extended\_ID-Code\_1 is used as SEL to show A/B address. In this mode the Extended ID-Code 1 (I2..I0) is limited to the range from 0 to 7.

### 5.6.5.10 Read\_Status

The "Read\_Status Request" is a command request and shall be used by the master to read the status of a specific slave.

The Read\_Status request shall have the following structure:

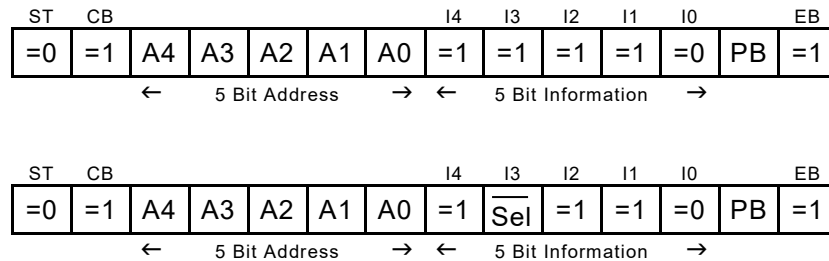


**Figure 30 – Structure of Read\_Status request (top: standard addressing mode; bottom: extended addressing mode)**

The slave response shall have the following structure:

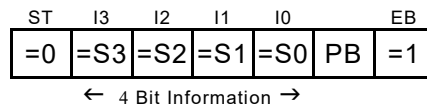


**Figure 31 – Structure of the slave response (Read\_Status)**

#### 5.6.5.11 R1

The "R1" is a command request. It is reserved and is optional.

This command will be coded in the information part of the master request as 1F<sub>Hex</sub>. The Reserve request shall have the following structure:

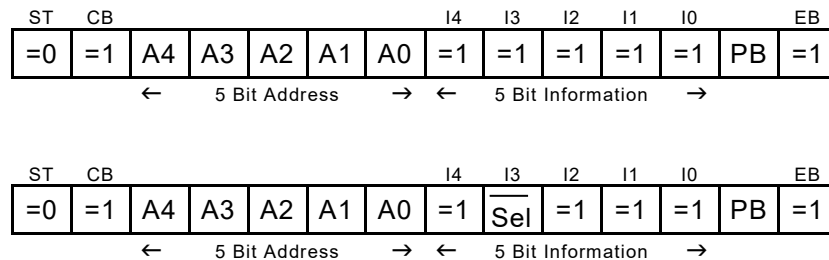


**Figure 32 – Structure of R1 request (top: standard addressing mode; bottom: extended addressing mode)**

The slave response may have the following structure:

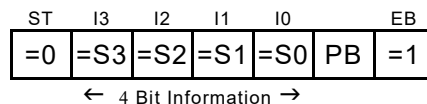


**Figure 33 – Structure of the slave response (R1)**

NOTE For compatibility reasons, the slave response may contain the content of the status register. This command has been a Read\_Reset\_Status in the first implementations of the system (up to version 2.0 of this standard). It is recommended not to use the command in new developments.

### 5.6.5.12 Broadcast (Reset)

The "Broadcast (Reset)" is a command request and is optional.

The Broadcast (Reset) request shall have the following structure:

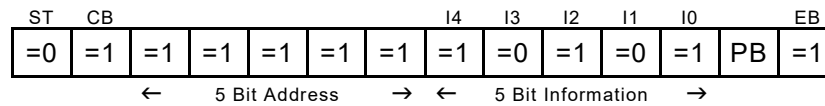


**Figure 34 – Structure of the Broadcast (Reset) request**

The slaves shall react with a Reset. There shall be no slave response to this request.

NOTE 1 In a network, this command may be used by the master to reset all slaves which realise the command. Thus it is used to perform an action similar to an emergency stop. As the Reset\_Slave request, the "Broadcast (Reset)" affects the slave's state machine. (see 8.4 for further details).

NOTE 2 For future expansion of the system the information part 15<sub>Hex</sub> is reserved for broadcast commands.

## 5.7 AS-i combined transactions

### 5.7.1 General

AS-i Single Transactions contain a maximum of 4 bits of information. If more than 4 bits of consistent information is to be transferred an additional set of rules has to be established to control the data transfer. There are several sets of rules available for different types of applications (e.g. single direction word transfer for analogue sensors or actuators, full duplex data exchange for intelligent slaves etc.). These are defined in the subsequent paragraphs.

To identify slaves that are capable to communicate via combined transactions the ID-codes (see 5.6.5.8) or extended ID-codes (see 5.6.5.9) are used. Masters that are capable to communicate via combined transactions are identified by their master profiles (see Annex B). Table 8 lists all presently defined combined transaction types.

**Table 8 – List of combined transaction types**

| Combined transaction type | Slave profile | Master profile | Remarks                                               |
|---------------------------|---------------|----------------|-------------------------------------------------------|
| Type 1                    | S-7.1         | Not supported  | <i>For new designs it is recommended to use S-7.3</i> |
| Type 1                    | S-7.2         | Not supported  | <i>For new designs it is recommended to use S-7.4</i> |
| Type 1                    | S-7.3         | M3             | 16 bit inputs or outputs                              |
| Type 1                    | S-7.4         | M3             | Complex field devices                                 |
| Type 2                    | S-7.5.5       | M4             | Combi field devices                                   |
| Type 2                    | S-7.A.5       | M4             | Combi field devices                                   |
| Type 2                    | S-B.A.5       | M4             | Serial communication field devices                    |
| Type 3                    | S-7.A.7       | M4             | 4I/4O in extended address mode                        |
| Type 3                    | S-7.A.A       | M4             | 8I/8O in extended address mode                        |
| Type 4                    | S-7.A.8       | M4             | 16 bit inputs in extended address mode                |
| Type 4                    | S-7.A.9       | M4             | Dual 16 bit inputs in extended address mode           |
| Type 5                    | S-6.0         | M4             | High speed 16 bit inputs and outputs                  |
| AS-i safety               | S-0.B         | Any            | AS-i safety input slaves                              |
| AS-i safety               | S-7.B         | Any            | AS-i safety input slaves with standard outputs        |

### 5.7.2 Combined transaction type 1

The combined transaction type 1 mechanism is handled according to the method given below. It uses the standard AS-i data transfer mechanisms to build a half duplex data transfer channel for byte transfer between the master and the slave with the profiles given in Table 8.

NOTE Combined transaction type 1 may be used for analogue sensors and actuators; replacement of 4 mA to 20 mA interfaces, for scanners and displays with 8 characters maximum. It may further be used for computer field devices with variable parameters; replacement for 4 mA to 20 mA interfaces with parameter exchange.

### 5.7.2.1 Definition of I/O data and parameter bits

The definition of the I/O data bits (Single transaction “Data\_Exchange”) is given in Figure 35.

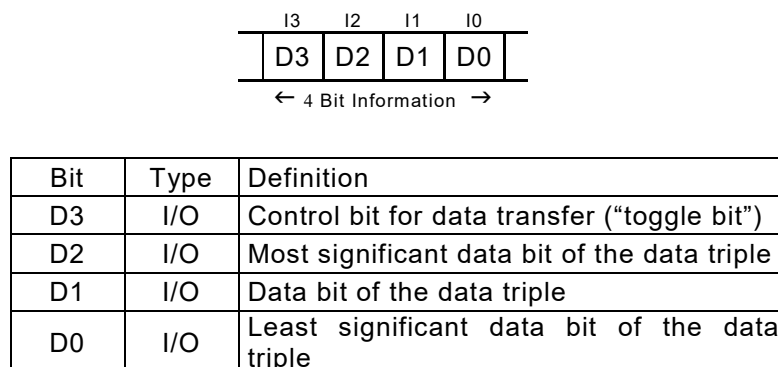


**Figure 35 – Definition of the I/O data bits in combined transaction type 1**

The definition of the parameter bits (Single transaction „Write\_Parameter“) is given in the following figure. This definition is valid for the slave profile S-7.4 only. For details see Annex A.

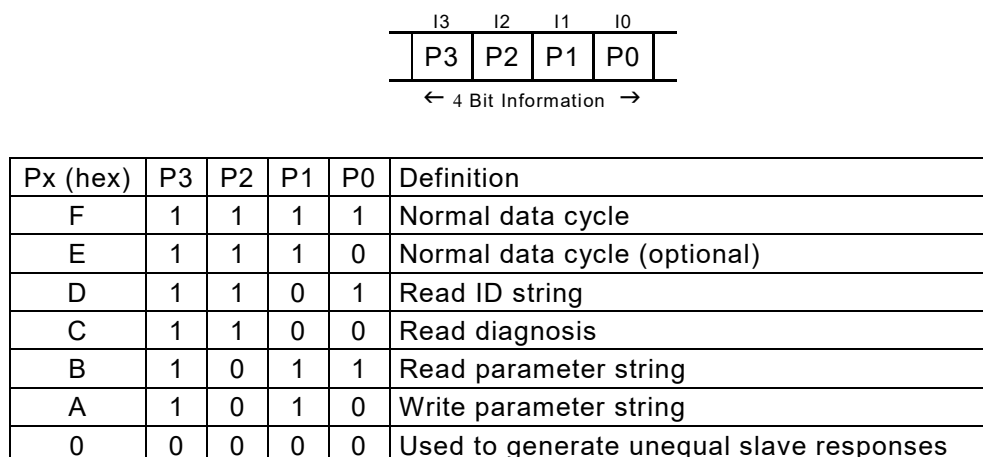


**Figure 36 – Definition of the parameter bits in combined transaction type 1**

When “Normal data cycle” is selected by the parameters, the data transfer direction is determined by the extended ID2 code as defined in 5.7.2.2. It cannot be changed during operation. The master acts as data source in case of an analogue output and as a data sink in case of an analogue input.

When “Read ID String”, “Read Diagnosis” or “Read parameter string” is selected by the parameters, the slave acts as data source and the master acts as data sink. When “Write parameter string” is selected by the parameters, the master acts as data source and the slave acts as data sink.

NOTE Due to this definition of data and parameter bits, combined transaction type 1 can only be used with standard addressing mode.

### 5.7.2.2 Definition of data transfer direction and number of channels

The data transfer direction and the number of data channels is defined by the extended ID2 code (Single transaction “Read\_ID2-Code”) stored in the slave (see Annex A for details).

NOTE For AS-i slaves that do not support the extended ID1/ID2 codes, the AS-i master should assume the default value extended ID2 = F<sub>Hex</sub>. This corresponds to an analogue input slave with 4 channels. It is allowed to implement less than 4 channels with extended ID2 code = F<sub>Hex</sub>. In this case, the slaves send data for the