

Environmental and endurance testing — Test methods for surface-mount boards of area array type packages FBGA, BGA, FLGA, LGA, SON and QFN

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British Standard

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National foreword

This British Standard is the official English language version of EN 62137:2004, including corrigendum February 2005. It is identical with IEC 62137:2004, including corrigendum January 2005.

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Summary of pages

This document comprises a front cover, an inside front cover, the EN title page, pages 2 to 26, an inside back cover and a back cover.

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English version

**Environmental and endurance testing -
Test methods for surface-mount boards of area array type packages
FBGA, BGA, FLGA, LGA, SON and QFN
(IEC 62137:2004)**

Essais d'environnement et d'endurance –
Méthodes d'essai pour les cartes
à montage en surface de boîtiers
de type matriciel FBGA, BGA, FLGA,
LGA, SON et QFN
(CEI 62137:2004)

Umwelt- und Dauerprüfung -
Prüfverfahren für in
Oberflächenmontagetechnik bestückte
Leiterplatten mit Area-Array-
Bauelementen der Bauformen
FBGA, BGA, FLGA, LGA, SON und QFN
(IEC 62137:2004)

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Foreword

The text of document 91/444/FDIS, future edition 1 of IEC 62137, prepared by IEC TC 91, Electronics assembly technology, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 62137 on 2004-07-01.

The following dates were fixed:

- latest date by which the EN has to be implemented
at national level by publication of an identical
national standard or by endorsement (dop) 2005-04-01
- latest date by which the national standards conflicting
with the EN have to be withdrawn (dow) 2007-07-01

Annex ZA has been added by CENELEC.

The contents of the corrigendum of February 2005 have been included in this copy.

Endorsement notice

The text of the International Standard IEC 62137:2004 was approved by CENELEC as a European Standard without any modification.

In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 60068-2-44	NOTE	Harmonized as EN 60068-2-44:1995 (not modified).
IEC 60749-1	NOTE	Harmonized as EN 60749-1:2003 (not modified).
IEC 60749-20	NOTE	Harmonized as EN 60749-20:2003 (not modified).
IEC 61189-3	NOTE	Harmonized as EN 61189-3:1997 (not modified).
IEC 61760-1	NOTE	Harmonized as EN 61760-1:1998 (not modified).
IEC 61190-1-1	NOTE	Harmonized as EN 61190-1-1:2002 (not modified).
IEC 61190-1-2	NOTE	Harmonized as EN 61190-1-2:2002 (not modified).
IEC 61190-1-3	NOTE	Harmonized as EN 61190-1-3:2002 (not modified).

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ENVIRONMENTAL AND ENDURANCE TESTING – TEST METHODS FOR SURFACE-MOUNT BOARDS OF AREA ARRAY TYPE PACKAGES FBGA, BGA, FLGA, LGA, SON AND QFN

1 Scope

This International Standard specifies the test method and guidelines for evaluating the quality and reliability of boards, solder lands, solder process and solder joints of reflow solder mounted area array type packages and peripheral terminal type packages.

This standard tests for durability against mechanical and thermal stress received during or after the mounting process of discrete semiconductor devices and of integrated circuits (hereinafter both referred to as semiconductor devices) used mainly for industrial and consumer use equipment.

The test method specified in this standard is an integrated one by including the evaluation method of mounting methods, mounting conditions, printed circuit boards, soldering materials, and so on. It does not specify the evaluation method of the individual semiconductor devices.

Mounting conditions, printed wiring boards, soldering materials, and so on significantly affect the result of the test specified in this standard. Therefore, the test specified in this standard shall not be regarded as the one to be used to guarantee the mounting reliability of the semiconductor devices.

The test method is not necessary if there is no stress (mechanical or others) from any of the tests covered in this standard.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-1:1988, *Environmental testing – Part 1: General and guidance*

IEC 60191-6-2:2001, *Mechanical standardization of semiconductor devices – Part 6-2: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for 1,50 mm, 1,27 mm and 1,00 mm pitch ball and column terminal packages*

IEC 60191-6-5:2001, *Mechanical standardization of semiconductor devices – Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch ball grid array (FBGA)*

JEITA¹ ETR-7001:1998, *Terms and definitions for surface mount technology*

3 Terms and definitions

For the purposes of this document, the terms and definitions for BGA, FBGA and so on, are referred to in IEC 60191-6-2 and IEC 60191-6-5.

¹ Japan Electronics and Information Technology Industries Association.

4 Abbreviations

FBGA fine-pitch ball grid array
BGA ball grid array
FLGA fine-pitch land grid array
LGA land grid array
SON small outline non-leaded package
QFN quad flat-pack non-leaded package

5 Solder joint quality test methods

5.1 Reflow solderability test for solder joint

5.1.1 Purpose

This test method specifies the reflow solderability test for the solder joint, as part of the specification in the standard. It is used to evaluate the solderability of reflow soldering of area-array type packages and peripheral terminal type packages (QFN and SON).

5.1.2 Test specimen

The test specimen shall satisfy the following conditions:

- a) test board design (see Clause A.4);
- b) standard mounting process (see Annex B);
- c) resistance to reflow soldering (see Clause A.1), solderability test for test board land (see Clause A.2) and peel test method for test board land (see Clause A.3).

5.1.3 Test apparatus

The test apparatus shall include the following:

- a) Oven
The oven shall maintain the temperature specified in 5.1.4.2.
- b) Moistening equipment
The humidifier shall maintain the temperature and humidity specified in 5.1.4.2. No reaction shall occur to the material of the oven at high temperatures. The water used for the test shall be purified water or deionized water, with pH 6,0 to pH 7,2 at 23 °C, and with a resistivity of 500 Ωm or higher.
- c) Infrared reflow/air reflow furnace
The infrared reflow/air reflow furnace shall meet the heating process conditions specified in 5.1.4.4.

5.1.4 Test procedure

5.1.4.1 Initial measurement

The initial measurement shall be carried out according to the items and conditions specified in the individual standard.

5.1.4.2 Moisture treatment

The moisture treatment is desirable for the test because a soldering defect may occur with moisture. "Defect of soldering" is defined in ETR-7001 as general failure of soldering.

a) Pre-treatment

Unless otherwise specified in the individual standard, the specimen subject to the moistening reflow pre-treatment in b) shall be baked in the oven at $(125 \pm 5) ^\circ\text{C}$ for 24 h or more.

b) Moistening process (1)

The specimen shall be moistened as specified in the individual standard. If there is no such specification mentioned in the individual standard, the specimen shall be subject to the moistening condition at $30 ^\circ\text{C}$, with a relative humidity of 70 % for 96 h.

c) Moistening process (2)

When the specimen is subjected to the reflow process twice, the specimen reflow soldered on the test board shall be moistened once again under the moistening condition as specified in the individual standard.

In this case, by taking into consideration the moistening reflow characteristic of the test board, it is desirable to set both the moisture soaking conditions and the moistening time for the repeat version of the test. In general, it is desirable to set the moistening condition to $30 ^\circ\text{C}$, with a relative humidity of 70 %, or to $30 ^\circ\text{C}$, with a relative humidity of 85 % up to 165 h maximum.

5.1.4.3 Test conditions

a) Reflow profile measurement

The infrared reflow/air reflow furnace shall meet the heating process conditions specified in Figure 3. The temperature of the specimen shall be measured at measurement Point A (the centre on the top of the package) and measurement point B (the soldered inner part of the terminal), shown in Figure 1.

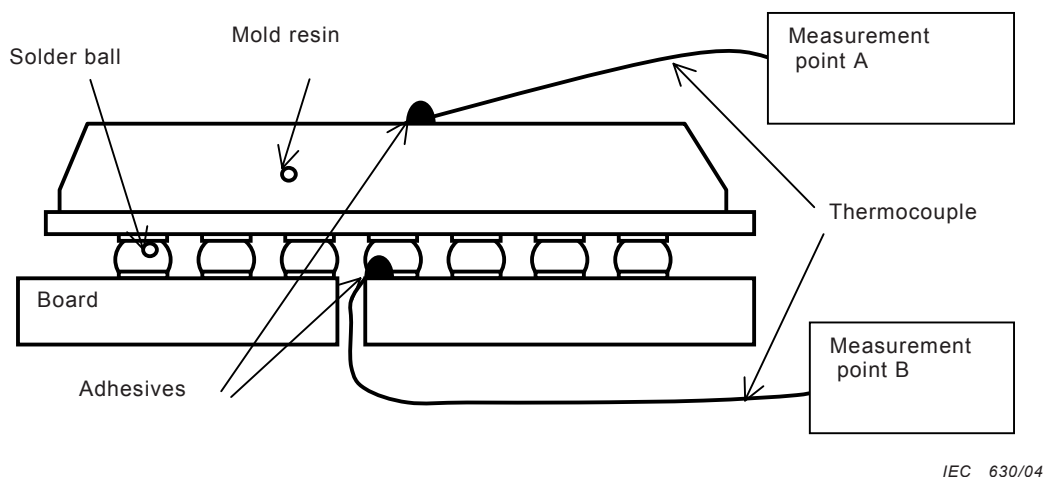


Figure 1 – Temperature measurement of the specimen using thermocouples

b) Test process.

The board to be tested shall carry out the evaluation under similar conditions to that of the actual usage of the board.

A proposal is shown in Figure 2.

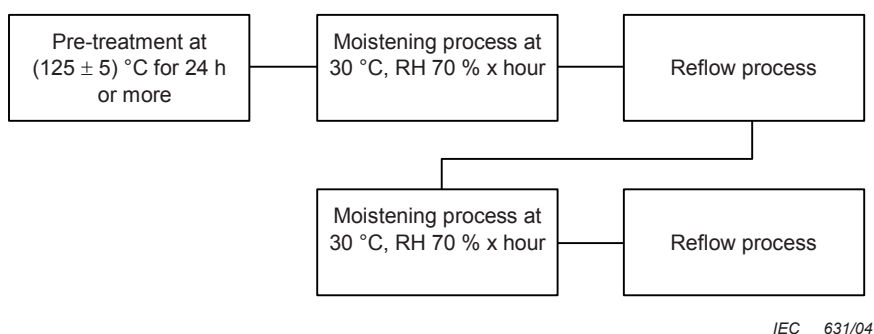


Figure 2 – Moistening/reflow process cycle proposed

5.1.4.4 Reflow heating

Mount the specimen on the mount reliability test board on which the solder paste has been printed as described in Annex B.

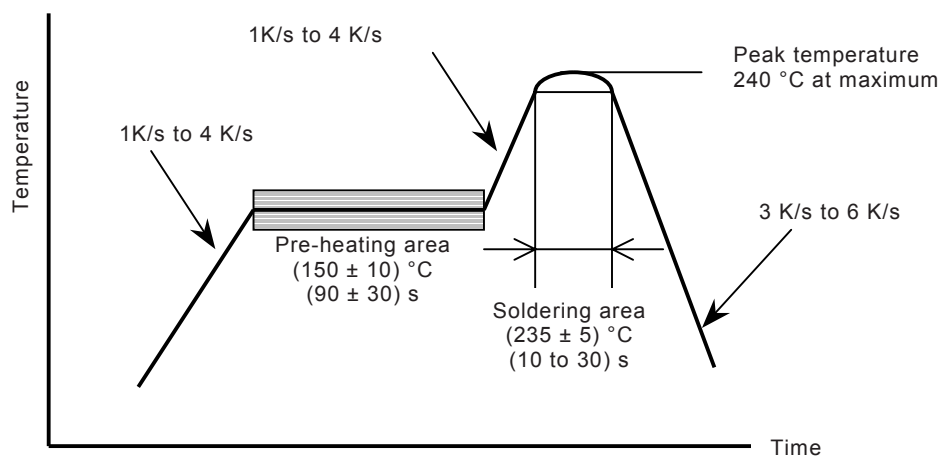


Figure 3 – Reflow profile

5.1.4.5 Post-treatment

After the test has been completed, if necessary, leave the specimen in the standard condition for the time specified in the individual standard:

- standard temperature range: 15 °C to 35 °C;
- standard relative humidity: 25 % to 75 %;
- standard atmospheric pressure: 86 kPa to 106 kPa.

Refer to IEC 60068-1.

5.1.4.6 Evaluation

Measure the electrical characteristic of the specimen according to the individual standard. Then, using soft X-ray inspection equipment, check the soldered condition. If necessary, observe the cross-sectional view after the buried process of resin.

5.2 Reserved for future use

(Vacant).