

Semiconductor die products —

Part 1: Requirements for procurement and use

The European Standard EN 62258-1:2005 has the status of a
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National foreword

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Foreword

The text of document 47/1820/FDIS, future edition 1 of IEC 62258-1, prepared by IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 62258-1 on 2005-10-01.

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- | | | |
|--|-------|------------|
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Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 62258-1:2005 was approved by CENELEC as a European Standard without any modification.

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INTRODUCTION

This International Standard is based on the work carried out in the ESPRIT 4th Framework project GOOD-DIE which resulted in the publication of the ES59008 series of European specifications. Organizations that helped prepare this standard include the ESPRIT GOOD-DIE project, The Die Products Consortium, JEITA, JEDEC and ZVEI.

SEMICONDUCTOR DIE PRODUCTS –

Part 1: Requirements for procurement and use

1 Scope

This part of IEC 62258 has been developed to facilitate the production, supply and use of semiconductor die products, including

- wafers,
- singulated bare die,
- die and wafers with attached connection structures,
- minimally or partially encapsulated die and wafers.

This standard defines the minimum requirements for the data which are needed to describe such die products and is intended as an aid in the design of and procurement of assemblies incorporating die products. It covers the requirements for data, including

- product identity,
- product data,
- die mechanical information,
- test, quality, assembly and reliability information,
- handling, shipping and storage information.

This standard covers the specific requirements for data needed to describe the geometrical properties of die, their physical properties and the means of connection necessary for their use in the development and manufacture of products. It also contains, in Annexes A and B, terminology and a list of common acronyms, respectively.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60191-4:1999, *Mechanical standardization of semiconductor devices – Part 4: Coding system and classification into forms of package outlines for semiconductor device packages*
Amendment 1 (2001)
Amendment 2 (2002)

IEC 61360-1:2002, *Standard data element types with associated classification scheme for electric components – Part 1: Definitions – Principles and methods*

IEC 62258-2, *Semiconductor die products – Part 2: Exchange data formats*¹

ISO 14644-1:1999, *Cleanrooms and associated controlled environments – Part 1: Classification of air cleanliness*

¹ To be published.

3 Terms and definitions

For the purposes of this document, the following terms apply.

NOTE 1 All terms defined here are in addition to relevant terms defined in IEC 60050: International Electrotechnical Vocabulary.

NOTE 2 Additional terms and acronyms are given for information in Annexes A and B.

3.1 Basic definitions

3.1.1

die (singular or plural)

separated piece(s) of semiconductor wafer that constitute(s) a discrete semiconductor or whole integrated circuit

3.1.2

wafer

slice or flat disc, either of semiconductor material or of such a material deposited on a substrate, in which devices or circuits are simultaneously processed and which may be subsequently separated into die

3.1.3

singulated die

individual and distinct die which have been separated from the wafer

3.1.4

bare die

unpackaged discrete semiconductor or integrated circuit with pads on the upper surface suitable for interconnection to the substrate or package

3.1.5

bare die with connection structures

unpackaged die that have had added bumps, lead frames or other terminations to interconnect for electrical attachment

NOTE Typically these can be die that have had solder or other metallic bumps added to the metallized pads on the die in the form of peripheral bumps or arrays (also known as flip-chip) or die that have had fine leads attached to the metallized pads on the die known as TAB.

3.1.6

minimally packaged die

MPD

die that have had some exterior packaging medium and interconnection structure added for protection and ease of handling

NOTE This definition includes such packaging technologies as chip scale packages (CSP) in which the area of the package is not significantly greater than the area of the bare die.

3.1.7

die device

bare die, with or without connection structures, or a minimally packaged die

3.2 General terminology

3.2.1

chip

common parlance for die

3.2.2

chip scale package

chip size package

CSP

generic term for packaging technologies that result in a packaged part that is only marginally larger than the internal die

3.2.3

discrete (semiconductor)

single two-, three- or four-terminal semiconductor device

NOTE Discrete semiconductors include such devices as individual diodes, transistors and thyristors.

3.2.4

hybrid (circuit)

module or encapsulated sub-assembly that comprises semiconductor die and printed or otherwise attached passive components

NOTE Also see multi-chip module and multi-chip package.

3.2.5

known good die

KGD

qualification of a semiconductor die which indicates that the die has been tested to a specified or determined level of quality or “goodness”

NOTE A commonly accepted definition of KGD is a die that has been tested and/or screened to quality levels that are of the same order as those applicable to the equivalent packaged parts.

3.2.6

package

total assembly which protects one or more electronic components from mechanical, environmental and electrical damage throughout its operational life and which provides means of interconnection

3.2.7

packaging

process of assembling one or more electronic components into a package

NOTE The use of “packaging” as a participle (e.g. “When packaging ICs into dual-in-line packages ...”) is deprecated.

3.2.8

packing

material which is used to protect electronic items from mechanical, environmental and electrical damage during transportation or storage and which is discarded prior to the incorporation of the item into its end application

3.2.9

multi-chip module

MCM

module that contains two or more die and/or minimally packaged die

NOTE Also see hybrid and multi-chip package.

3.2.10

multi-chip package

MCP

package that contains two or more die and/or minimally packaged die

NOTE Also see hybrid and multi-chip module.

3.2.11**system in a package****SiP**

multi-chip package (MCP) that performs a complete system function

3.2.12**multi-device sub-assembly****MDS**

sub-system which consists of multiple electronic devices including at least one integrated circuit

NOTE This is a generic term which includes, amongst others, hybrid, MCM, MCP and SiP.

3.2.13**pad**

conducting feature on a die device forming a terminal to which external electrical connections are made

NOTE For bare die without external connections, the pad acts as the terminal itself. For bumped die the terminal is in the form of additional conducting material placed on a pad, whilst for die with attached lead frame the terminal is in the form of a conductor connected to the pad and extending from the die.

3.3 Semiconductor manufacturing and interconnection terminology**3.3.1****mask**

- a) optical overlay used in photo-etching during the process of semiconductor fabrication
- b) general term to refer to the major individual patterning stages that are used within the fabrication process

3.3.2**layer**

loose topological term used in describing the process of semiconductor fabrication

NOTE A layer consists of a specific material and a semiconductor device consists of many layers.

3.3.3**passivation**

top or final processing and covering on a die, usually of semiconductor oxide or nitride, that protects and seals the active areas of the die from further external chemical or mechanical contamination

NOTE Bond pads require an opening in this passivation to allow electrical contact.

3.3.4**scribe line**

scribe lane

area surrounding the die that is set aside on the wafer for the purposes of scribing and sawing the die from the wafer

NOTE This feature may be covered by many other terms such as scribe street, saw lane, dicing lane, etc.

3.3.5**die separation**

dicing

sawing

means by which individual die are cut from the wafer

NOTE Die separation is commonly performed by using a fine circular saw.

3.3.6**wire bonding**

process of attaching interconnection wire or ribbon to a die

3.3.7

bond pads

metallized areas on the die that are used for temporary or permanent electrical connection (bonding)

3.3.8

bumps

raised metallized areas on the die that are used for temporary or permanent electrical connection

3.3.9

lead frame

supporting structure upon which a die is mounted and which also includes the connection structure to which the die is bonded

3.3.10

die attach

method and materials used to attach a die to a substrate

3.3.11

flip-chip

semiconductor die which is electrically and/or mechanically connected to an interconnection structure in such a way that the active area faces the interconnection structure

3.3.12

interposer

material placed between two surfaces giving electrical insulation, mechanical strength and/or controlled mechanical separation between the two surfaces

NOTE An interposer may be used as a means for redistributing electrical connections and/or allowing for different thermal expansions between adjacent surfaces.

3.3.13

redistribution

process of moving terminals on die to more convenient positions by additional connectivity layers or by the use of an interposer

4 General requirements

4.1 General

Suppliers of die devices shall furnish information which is necessary and sufficient for users of the devices at all stages of design, procurement, manufacture and test of products containing them. Details of the requirements are given below and in other parts of this standard. The form in which the information may be supplied is covered in IEC 62258-2.

Whilst it is expected that much of the information supplied in conformance with this standard will be in the public domain and available from sources such as manufacturers' data sheets, this specification does not place an obligation on a supplier to make information public. Any information that a supplier considers to be proprietary or commercially sensitive may be supplied under the terms of a non-disclosure agreement.

For further details of requirements, refer to Clauses 6, 7, 8, 9, 10 and 11.