

High-voltage switchgear and controlgear —

Part 101: Synthetic testing

ICS 29.130.10

National foreword

This British Standard is the UK implementation of EN 62271-101:2006+A1:2010. It is identical with IEC 62271-101:2006, incorporating amendment 1:2010. It supersedes BS EN 62271-101:2006, which will be withdrawn on 1 September 2013.

The start and finish of text introduced or altered by amendment is indicated in the text by tags. Tags indicating changes to IEC text carry the number of the IEC amendment. For example, text altered by IEC amendment 1 is indicated by **A1** **A1**.

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CENELEC

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Foreword

The text of document 17A/753/FDIS, future edition 1 of IEC 62271-101, prepared by SC 17A, High-voltage switchgear and controlgear, of IEC TC 17, Switchgear and controlgear, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 62271-101 on 2006-07-01.

This European Standard supersedes EN 60427:2000.

This standard shall be read in conjunction with EN 62271-100:2001. The numbering of the subclauses of Clause 6 is the same as in EN 62271-100. However, not all subclauses of EN 62271-100 are addressed; merely those where synthetic testing has introduced changes.

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HIGH-VOLTAGE SWITCHGEAR AND CONTROLGEAR –

Part 101: Synthetic testing

1 Scope

This part of IEC 62271 mainly applies to a.c. circuit-breakers within the scope of IEC 62271-100. It provides the general rules for testing a.c. circuit-breakers, for making and breaking capacities over the range of test duties described in 6.102 to 6.111 of IEC 62271-100, by synthetic methods.

NOTE Circuits for the test duties described in 6.111 have not yet been standardized. However, present methods are given in Annex G.

It has been proven that synthetic testing is an economical and technically correct way to test high-voltage a.c. circuit-breakers according to the requirements of IEC 62271-100 and that it is equivalent to direct testing.

The methods and techniques described are those in general use. The purpose of this standard is to establish criteria for synthetic testing and for the proper evaluation of results. Such criteria will establish the validity of the test method without imposing restraints on innovation of test circuitry.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

☐^{A1} IEC 62271-100:2008, *High-voltage switchgear and controlgear – Part 100: Alternating-current circuit-breakers*¹ ☐^{A1}

IEC 62271-100:2001, *High-voltage switchgear and controlgear – Part 100: High-voltage alternating current circuit-breakers*

IEC 62271-308:2002, *High-voltage switchgear and controlgear – Part 308: Guide for asymmetrical short-circuit test duty T100a*

3 Terms and definitions

For the purposes of this document, the terms and definitions of IEC 62271-100, as well as the following terms and definitions, apply.

3.1

direct test

test in which the applied voltage, the current and the transient and power-frequency recovery voltages are all obtained from a circuit having a single-power source, which may be a power system or special alternators as used in short-circuit testing stations or a combination of both

¹ Unless explicitly otherwise mentioned, all of the references to IEC 62271-100 make reference to IEC 62271-100:2001. A second amendment to IEC 62271-101, which will update all cross-references to the new IEC 62271-100:2008 is under consideration.

3.2

synthetic test

test in which all of the current, or a major portion of it, is obtained from one source (current circuit), and in which the applied voltage and/or the recovery voltages (transient and power frequency) are obtained wholly or in part from one or more separate sources (voltage circuits)

3.3

test circuit-breaker

circuit-breaker under test (see 6.102.2 of IEC 62271-100:2001)

3.4

auxiliary circuit-breaker(s)

circuit-breaker(s) forming part of a synthetic test circuit used to put the test circuit-breaker into the required relation with various circuits

3.5

current circuit

that part of the synthetic test circuit from which all or the major part of the power-frequency current is obtained

3.6

voltage circuit

that part of the synthetic test circuit from which all or the major part of the applied voltage and/or recovery voltage is obtained

3.7

prospective current (of a circuit and with respect to a circuit-breaker)

current that would flow in the circuit if each pole of the test and auxiliary circuit-breakers were replaced by a conductor of negligible impedance

[IEV 441-17-01, modified]

3.8

actual current

current through the test circuit-breaker (prospective current modified by the arc voltage of the test and auxiliary circuit-breakers)

3.9

distortion current

calculated current equal to the difference between the prospective current and the actual current

3.10

post-arc current

current which flows through the arc gap of a circuit-breaker when the current and arc voltage have fallen to zero and the transient recovery voltage has begun to rise

3.11

current-injection method

synthetic test method in which the voltage circuit is applied to the test circuit-breaker before power-frequency current zero

3.12

initial transient making current

ITMC

transient current which flows through the circuit-breaker at the moment of voltage breakdown prior to the initiation of current from the current circuit during making

3.13

injected current

current supplied by the voltage circuit of a current injection circuit when it is connected to the circuit-breaker under test

3.14

voltage-injection method

synthetic test method in which the voltage circuit is applied to the test circuit-breaker after power frequency current zero

3.15

reference system conditions

conditions of an electrical system having the parameters from which the rated and test values of IEC 62271-100 are derived

3.16

time delay of making device

t_m

time interval, during synthetic making test, between the instant of breakdown of the applied voltage and the initiation of current from the current circuit

3.17

minimum clearing time

sum of the minimum opening time, minimum relay time ($\frac{1}{2}$ cycle), and the minimum arcing time for the minor loop of the first-pole-to-clear, during test duty T100a only, as declared by the manufacturer. This definition should be used only for the determination of the test parameters for test duty T100a.

NOTE 1 The minimum clearing time obtained during the tests should not be lower than the value declared by the manufacturer. Prior to the tests, the minimum opening time should be measured at maximum trip coil voltage maximum pressure for operation and minimum pressure for interruption. If the minimum opening time measured prior to the tests is lower than the one declared by the manufacturer, this lower value should be used for the determination of the required test parameters.

NOTE 2 This definition assumes that the minimum clearing time obtained with the minimum pressure for interruption is similar to the one that would be obtained with the maximum pressure for interruption. Normally, the minimum clearing time is obtained with the maximum pressure for interruption. If such pressure condition is giving a minimum clearing time such that the minimum clearing time range applicable (as given in Tables 1a to 2d of IEC 62271-308:2002) for tests is different than the one obtained at minimum pressure for interruption, then it is permissible to verify the minimum clearing time by using the maximum pressure for interruption.

3.18

pre-strike

voltage breakdown between the contacts during a making operation which initiates current flow

4 Synthetic testing techniques and methods for short-circuit breaking tests

4.1 Basic principles and general requirements for synthetic breaking test methods

Any particular synthetic method chosen for testing shall adequately stress the test circuit-breaker. Generally, the adequacy is established when the test method meets the requirements set forth in the following subclauses.

A circuit-breaker has two basic positions: closed and open. In the closed position a circuit-breaker conducts full current with negligible voltage drop across its contacts. In the open position it conducts negligible current but with full voltage across the contacts. This defines the two main stresses, the current stress and the voltage stress, which are separated in time.

If closer attention is paid to the voltage and current stresses during the interrupting process (Figure 1), three main intervals can be recognized:

- High-current interval

The high-current interval is the time from contact separation to the start of the significant change in arc voltage. The high-current interval precedes the interaction and high-voltage intervals.

- Interaction interval

The interaction interval is the time from the start of the significant change in arc voltage prior to current zero to the time when the current including the post-arc current, if any, ceases to flow through the test circuit-breaker (see also Clause B.2).

- High-voltage interval

The high-voltage interval is the time from the moment when the current including the post-arc current, if any, ceases to flow through the test circuit-breaker to the end of the test.

4.1.1 High-current interval

During the high-current interval the test circuit-breaker shall be stressed by the test circuit in such a way that the starting conditions for the interaction interval, within tolerances to be specified, are the same as under reference system conditions.

In synthetic test circuits the ratio of the power-frequency voltage of the current circuit to the arc voltage is low in comparison with tests at reference system conditions due to:

- the voltage of the current circuit being a fraction of the system voltage;
- the fact that the arc voltages of the test circuit-breaker and of the auxiliary circuit-breaker are added.

As a result the duration of the current loop and the peak value of the current will be reduced. This distortion of the current is outlined in Annex A.

Considerations with respect to the arc energy released in the test circuit-breaker lead to a maximum permissible influence in terms of tolerances on two characteristic values of the shape of the current, i.e. current-peak value and current-loop duration (see Annex A).

The tolerance on the amplitude and the power frequency of the prospective breaking current is given in 6.103.2 and 6.104.3 of IEC 62271-100. Therefore, the following conditions concerning the actual current through the test circuit-breaker shall be met:

- for symmetrical testing the current amplitude and final loop duration shall not be less than 90 % of the required values based on rated current;
- for asymmetrical testing, the current amplitude and final loop duration shall be between 90 % and 110 % of the required values, based on rated current and time constant (see Tables I.1a to I.2d).

Adjustment measures:

The amplitude and duration of the last current loop may be adjusted by several means, such as

- increasing or decreasing of the r.m.s. value of the short-circuit test current,
- changing of the frequency of the test current,
- using pre-tripping or delayed tripping,
- changing the instant of current initiation (initial d.c. component).

For reference see 5.3 of IEC 62271-308.

4.1.2 Interaction interval

During the interaction interval, the short-circuit current stress changes into high-voltage stress and the circuit-breaker performance can significantly influence the current and voltages in the circuit. As the current decreases to zero, the arc voltage may rise to charge parallel capacitance and distort current passing through the arc. After the current zero the post-arc conductivity may result in additional damping of the transient recovery voltage and thus influence the voltage across the circuit-breaker and the energy supplied to the ionized contact gap. The interaction between the circuit and the circuit-breaker immediately before and after current zero (i.e. during the interaction interval) is of extreme importance to the interrupting process.

During the interaction interval, the current and voltage waveforms shall be the same for a synthetic test as under reference system conditions (see 3.15), taking into account the possible deviations of the current and voltage from the prospective values due to the interaction between the circuit-breaker and the circuit.

The interaction interval presents the critical time for the thermal failure mode of the circuit-breaker. Therefore, it is of extreme importance that the shape and magnitude of the prospective transient recovery voltage (TRV) corresponds to that associated with the prospective current of the relevant test duty.

The above implies strict requirements for the test circuit. The requirements are given for the current injection method in 4.2.1 and for the voltage injection method in 4.2.2.

NOTE Depending on the test circuit used, the interaction between circuit and test circuit-breaker may be disturbed by the behaviour of the auxiliary circuit-breaker during the critical interval around current zero.

The arc voltage of the auxiliary circuit-breaker should be less than or equal to the arc voltage of the test circuit-breaker.

If an auxiliary circuit-breaker with a higher arc voltage is used, a higher power-frequency voltage of the current circuit may be necessary.

4.1.3 High-voltage interval

During the high-voltage interval, the gap of the test circuit-breaker is stressed by the recovery voltage.

The prospective TRV shall comply with the requirements of 4.102, 4.105, 4.106 and 6.104.5 of IEC 62271-100.

Suitable methods for determining the prospective TRV in synthetic test circuits can be selected from Annex F of IEC 62271-100.

The impedance of the voltage circuit shall be low enough to give clear evidence of breakdown, if any.

NOTE 1 If the test circuit-breaker is fitted with parallel breaking resistors, a special procedure may be necessary (see Annex F).

NOTE 2 If the TRV is obtained from more than one source the overall waveshape should not show any appreciable discontinuity.

In principle, the power-frequency recovery voltage for the basic short-circuit test duties should preferably be a.c. and shall equate with the requirements of 6.104.7 of IEC 62271-100. In synthetic testing, the recovery voltage is supplied from a voltage circuit, either directly or in series with the current circuit. This gives an a.c. voltage, or a combined a.c. and d.c. voltage, or a d.c. voltage, which in most cases decays due to the limited energy of the voltage source. It may thus not be possible to maintain the recovery voltage for at least 0,3 s as specified in 6.104.7 of IEC 62271-100. Deviations from the specified recovery voltage are acceptable if the following conditions are met:

- The instantaneous value of the recovery voltage during a period equal to $1/8$ of a cycle of the rated frequency of the circuit-breaker shall be not less than the equivalent instantaneous value of the power-frequency recovery voltage specified in 6.104.7 of IEC 62271-100 which, for a test with symmetrical current, starts with a minimum peak value of $0,95 \times k_{pp} \times U_r \sqrt{2} / \sqrt{3}$

where

k_{pp} is the first pole-to-clear factor;

U_r is the rated voltage of the circuit-breaker.

- Whether an exponentially decaying d.c., an a.c. or a combined a.c. and d.c. recovery voltage is used, its instantaneous value (for d.c.) or its peak value (for a.c. or combined a.c. and d.c.) should in principle be kept as close as possible to $U_r \sqrt{2} / \sqrt{3}$ and in any case must not fall below $0,5 U_r \sqrt{2} / \sqrt{3}$ in less than 0,1 s (see Figure 2).
- If an exponentially decaying d.c. or a combined a.c. and d.c. recovery voltage imposes an inappropriate stress on the circuit-breaker compared to that due to the specified a.c. recovery voltage in reference system conditions, then a more appropriate circuit may be used taking into account 6.104.7 of IEC 62271-100 and also the limits stated above.

4.2 Synthetic test circuits and related specific requirements for breaking tests

4.2.1 Current injection methods

These methods can be described in terms of general principles as follows (see Annex B):

- the current from the voltage circuit is superimposed on the power-frequency current through the test circuit-breaker prior to the interaction interval;
- an auxiliary circuit-breaker interrupts the current from the current circuit prior to the interaction interval.

During the interaction interval, the test circuit-breaker is exposed to the voltage of the voltage circuit having an impedance which is representative of the reference system conditions. This explains the validity of current injection methods. Several current injection methods are known but only the conditions for parallel current injection are given below since this method is used by the majority of the test laboratories. The following conditions shall be met:

a) *TRV waveshape circuit*

- 1) The shape and magnitude of the prospective TRV shall comply with the specified values.
- 2) Ideally the equivalent surge impedance Z_h (see Figure 3) shall be equal to $(du/dt)/(di/dt)$ during the interaction interval. (du/dt) is the rate of rise of the specified transient recovery voltage and di/dt is the rate of decrease of the specified short-circuit current.
- 3) The combination of the stray and lumped capacitance C_{dh} in parallel with Z_h gives rise to the delay time $t_d = Z_h \times C_{dh}$.

b) *Inductance of the voltage circuit*

The value of the inductance of the voltage circuit shall be between 1,0 and 1,5 times the inductance derived from the equivalent power-frequency voltage divided by the prospective current.

c) *Frequency of the injected current and the injection timing*

The frequency of the injected current shall preferably be of the order of 500 Hz with a lower limit of 250 Hz and an upper limit of 1 000 Hz.

In order to prevent undue influence on the waveshape of the power-frequency current, the lower limit of the frequency of the injected current is 250 Hz.

The maximum frequency of the injected current is determined by the interval of significant change of arc voltage, the interval for which shall be smaller than the time for which the arc is fed only by the injected current. To achieve this, the period of the injected frequency should be at least four times the interval of significant change of arc voltage (see Annex B).

The initiation of the injected current shall be adjusted such that the time, during which the test circuit-breaker is fed only by the injected current, is not more than a quarter of the period of the injected current frequency with a maximum of 500 μ s.

NOTE Attention should be paid to the possible overstressing of the circuit-breaker if the time that the test circuit-breaker is fed by the injected current only is less than 200 μ s.

d) *Waveshape of the injected current*

The prospective rate of decrease (di/dt) of the injected current shall correspond to that of the prospective power-frequency current.

The injected current shall be practically free of superimposed oscillations for a time not less than 100 μ s before current zero.

4.2.2 Voltage injection method

Several voltage injection methods are known but only series voltage injection is described here in general terms as follows (see also Annex C):

- the voltage from the voltage circuit is applied to the test circuit-breaker after the interaction interval;
- a capacitor in parallel with the auxiliary circuit-breaker is used to apply the recovery voltage to the test circuit-breaker;
- during the high-current and interaction intervals, the test circuit-breaker is exposed to the current circuit only.

The voltage injection method shall not be used to check the thermal behaviour of the circuit-breaker.

For example in the case of short-line fault tests, in addition to the voltage injection circuit supplying the source side TRV, a current injection circuit which is connected to the line-side terminal of the test circuit-breaker shall be used to supply the line-side transient voltage.

When used for tests relating to the dielectric behaviour of the circuit-breaker, the following conditions shall be met:

- the auxiliary circuit-breaker should have an arc voltage less than or equal to that of the test circuit-breaker (see Note in 4.1.2);
- the voltage circuit shall be designed in such a manner as to allow detection of re-ignitions or re-strikes, should they occur.
Therefore, the capacitance across the auxiliary circuit-breaker shall be at least 20 times the capacitance in parallel with the test circuit-breaker. Care should be taken to avoid undue distortion of the current before power-frequency current zero;
- no pause shall be introduced by the combining of the current circuit and the voltage circuit.

4.2.3 Duplicate circuit method (transformer or Skeats circuit)

This method can be described in terms of general principles as follows (see also Annex D):

- the current and voltage are supplied from the same source;
- the a.c. recovery voltage is supplied from a step-up transformer, the primary of which is connected to the current circuit;
- the recovery voltage is applied to the test circuit-breaker through an impedance (normally a resistance).

The auxiliary circuit-breaker interrupts the current prior to the test circuit-breaker by a short time interval (usually about 10 μ s). During this short interval the value of di/dt of the current in the test circuit-breaker is decreased.

The Skeats circuit is therefore not valid for tests where attention is paid to the thermal failure mode of the test circuit-breaker. It is suitable for testing the dielectric behaviour of a circuit-breaker and can be used for making tests.

The Skeats circuit can easily be adapted to supply full voltage stresses in two (or more) operations e.g. at both closing and opening in a CO operation, at both openings in an O – t – CO operation or even at consecutive current zeros in an opening operation. See Annex D.

4.2.4 Other synthetic test methods

Other methods may proven to be correct and advantageous for testing of circuit-breakers with specific characteristics or for testing of a circuit-breaker for specific performance. Even though these methods are not covered by this standard, they can be used subject to understanding of their application and agreement between the manufacturer and the user.

Methods concerning metal enclosed, and dead tank circuit-breakers should take into account the recommendations of [\[A1\]](#) Annex O of IEC 62271-100:2008. [\[A1\]](#)

A method available for testing circuit-breakers having parallel breaking resistors is reported in Annex F.

4.3 Three-phase synthetic test methods

Three-phase synthetic test methods shall be applied for testing of circuit-breakers which can not be tested single pole as per 6.102.4.1 of IEC 62271-100. They can also be used as an alternative to single phase synthetic tests if relevant. Short-circuit test sequences T10, T30 and T60 may in any case be performed in single-phase test circuits.

To ensure that the appropriate stresses in the interrupting element and those between poles and, if relevant, to the enclosure are applied, the following general requirements shall be fulfilled:

- a) full three-phase current shall be supplied to the three-pole circuit-breaker under test;
- b) information about the required test circuits for test duties T100s and T100a is given in Table 1;
- c) the test parameters for each pole-to-clear are given in Tables 2a and 2b;
- d) all the above stresses preferably should be applied in the same test. If this is impossible, a multi-part testing procedure may be necessary;
- e) to avoid changing the connection of the high-voltage circuit to the circuit-breaker between the tests of each test sequence, the first-pole-to-clear is allowed to be kept in the same phase during the whole sequence, taking into account the requirements of 6.105.1 of IEC 62271-100.

Table 1 – Test circuits for test duties T100s and T100a

k_{pp}	T100s		T100a	
	First-pole-to-clear	Other poles	First-pole-to-clear	Other poles
1,5	Application of synthetic circuits of 4.2.1 or 4.2.2 at all operations	Application of synthetic circuits of 4.2.1, 4.2.2 or 4.2.3 at all operations	Application of synthetic circuits of 4.2.1 or 4.2.2 for at least two operations. The third operation can be tested with 4.2.3	Application of synthetic circuit 4.2.1 or 4.2.2 at least to the operation with major extended loop and longest arcing time
1,3	Application of synthetic circuits of 4.2.1 or 4.2.2 for at least two operations. The third operation can be tested with 4.2.3	Application of synthetic circuit 4.2.1 or 4.2.2 at least to the second-pole-to-clear at the operation with the longest arcing time. Application of synthetic circuits of 4.2.1 through 4.2.3 at all other operations	Application of synthetic circuits of 4.2.1 or 4.2.2 for at least two operations. The third operation can be tested with 4.2.3	Application of synthetic circuits of 4.2.1 or 4.2.2 at least to the second-pole-to-clear at the operation with major extended loop and longest arcing time. Application of synthetic circuits of 4.2.1 through 4.2.3 at all other operations
k_{pp} first-pole-to-clear factor. NOTE Voltage injection is only permitted if there are no ITRV requirements, or if these requirements are covered by SLF testing.				

Table 2 – Test duties T10, T30, T60 and T100s

Table 2a – First-pole-to-clear factor: 1,5 –
Test parameters during three-phase interruption

TRV peak in %				Recovery voltage peak p.u.	du/dt %	di/dt %	Phase angle °
		At instant of first-pole-to-clear	At instant of second and third-pole-to-clear				
Phases	A	100	-	1	100	100	-
	B	0	58	1	70	87	90
	C	0	58	1	70	87	90
Between phases	A – B	100	58	1,732			
	B – C	0	115	1,732			
	A – C	100	58	1,732			

TRV peak first pole-to-clear: $u_c = k_{af} \times k_{pp} \times U_r \times \sqrt{2}/\sqrt{3}$ (= 100 %).

1 p.u. = $U_r \times \sqrt{2}/\sqrt{3}$.

The first-pole-to-clear is in phase A.

Table 2b – First-pole-to-clear factor: 1,3 –
Test parameters during three-phase interruption

TRV peak in %				Recovery voltage peak p.u.	du/dt %	di/dt %	Phase angle °
		At instant of first-pole-to-clear	At instant of second and third-pole-to-clear				
Phases	A	100	- / -	1	100	100	-
	B	0	- / 77	1	70	57	120
	C	0	98 / -	1	95	89	77
Between phases	A – B	100	- / 91	1,732			
	B – C	0	98 / 98	1,732			
	A – C	100	89 / -	1,732			

TRV peak first pole-to-clear: $u_c = k_{af} \times k_{pp} \times U_r \times \sqrt{2}/\sqrt{3}$ (= 100 %)

1 p.u. = $U_r \times \sqrt{2}/\sqrt{3}$

The first-pole-to-clear is in phase A.

The second-pole-to-clear is in phase C.

5 Synthetic testing techniques and methods for short-circuit making tests

5.1 Basic principles and general requirements for synthetic making test methods

During a closing operation onto a short-circuit, the circuit-breaker contact gap is subjected to the applied voltage as per 6.104.1 of IEC 62271-100. After the moment of breakdown the circuit-breaker is subjected to the making current as per 6.104.2.1 of IEC 62271-100. In a synthetic test circuit the applied voltage is supplied by a separate voltage source and the short-circuit current is supplied by a current circuit at reduced voltage. This latter is connected to the circuit-breaker immediately after breakdown of the contact gap by means of a fast making device, e.g. a triggered spark gap.

Any particular synthetic method chosen for testing shall adequately stress the test circuit-breaker. Generally the adequacy is established when the test method meets the requirements set forth in the following subclauses.

Prior to making, a circuit-breaker withstands the rated phase-to-earth voltage applied across its terminals: during making, it carries the rated short-circuit current. If closer attention is paid to the voltage and current stresses during the making test (see Figure 4) three main intervals can be recognized:

- High-voltage interval
The high-voltage interval is the time from the commencement of the test, with the circuit-breaker in the open position, to the moment of breakdown across the contact gap;
- Pre-arcing interval
The pre-arcing interval is the time, during the closing stroke of the circuit-breaker, from the moment of breakdown across the contact gap to the touching of the contacts;
- Latching interval
The latching interval is the time, during the closing stroke of the circuit-breaker, from the touching of the contacts to the moment when the contacts reach the fully closed (latched) position.

5.1.1 High-voltage interval

During this interval the circuit-breaker shall be stressed by the test circuit in such a way that the starting conditions for the pre-arcing interval, within the tolerances to be specified, are the same as the following reference system conditions:

- The applied voltage shall comply with the requirement set forth in 6.104.1 of IEC 62271-100;
- The phase relationship between the applied voltage and the short-circuit current shall correspond to the rated power factor of the test circuit within the tolerances given in 6.103.1 of IEC 62271-100.

5.1.2 Pre-arcing interval

During pre-arcing the circuit-breaker is subjected to electrodynamic forces due to the current and to deteriorating effects due to arc-energy. The current is composed of three components:

- the initial transient making current, ITMC;
- the d.c. and a.c. components of the short-circuit current.

Two typical cases may occur depending on the moment of closing:

- breakdown occurs near the crest of the applied voltage establishing an almost symmetrical current. Pre-arc energy and ITMC are relatively high;
- breakdown occurs near zero of the applied voltage establishing an asymmetrical current. Pre-arc energy and ITMC are negligible, with the exception of the case of non-simultaneous closing in a multi-unit pole.

5.1.3 Latching interval and fully closed position

During these intervals the circuit-breaker has to close in presence of the electrodynamic forces due to the current and contact friction forces. Therefore during these intervals the making current shall comply with 4.103 of IEC 62271-100.

5.2 Synthetic test circuit and related specific requirements for making tests

5.2.1 General

The test circuit and specific requirements shall fulfil requirement a) of 6.104.2.1 of IEC 62271-100.

5.2.2 Test circuit

The test circuit is made up with two sources, namely the current and the voltage circuit. Typical circuits showing voltage and current waveshapes are given in Figure 5 for single-phase and Figure 6 for three-phase.

- the voltage circuit supplies
 - the applied voltage during the high-voltage interval,
 - the ITMC during the pre-arcing interval, by the discharge of the ITMC-circuit;
- the current circuit supplies the making current during the pre-arcing, and latching intervals.

5.2.3 Specific requirements

During a synthetic making test, the phase relationship between the applied test voltage and the short-circuit current depends on the following parameters:

- power factor ($\cos \varphi$) of the current circuit;
- phase displacement (β) between U_{cs} and U_h (if U_h is an a.c. voltage source);
- time delay of making device (t_m).

The condition of the correct making operation is fulfilled when:

$$\beta + t_m' + (90 - \varphi) \leq 27^\circ \text{ in the case that } U_h \text{ is an a.c. source and } t_m \text{ is as short as possible but in any case not longer than } 300 \mu\text{s}$$

where $t_m' = (t_m / T) \times 360^\circ$ (with $T = 20$ ms for 50 Hz and $T = 16,7$ ms for 60 Hz).

NOTE 1 The high-voltage circuit U_h may be an a.c. source, a d.c. source or a combination of both.

NOTE 2 β may be negative if the voltage U_h is obtained by a separate source.

The injected current supplied by the voltage circuit shall ensure pre-arcing until the breakdown of the fast make gap. Therefore, the time constant of the ITMC circuit shall be long enough to ensure current flow during the time delay of the making device.

6 Specific requirements for synthetic tests for making and breaking performance related to the requirements of 6.102 through 6.111 of IEC 62271-100

Subclauses 6.102 through 6.111 of IEC 62271-100 are also applicable for synthetic testing. However, in some cases special techniques are necessary. These cases are outlined in the following subclauses. The numbering of the subclauses corresponds to that of IEC 62271-100.

A1 Annex O of IEC 62271-100:2008 gives guidelines for the testing of metal-enclosed and dead tank circuit breakers.

6.102.4.2 Unit testing

For the application of the synthetic test methods to one or more units of a circuit breaker, the requirements of 6.102.4.2 of IEC 62271-100:2008 are applicable. In the case of metal-enclosed or dead tank circuit-breakers, Annex N gives details of some typical test circuits and Annex O of IEC 62271-100:2008 outlines appropriate testing guidelines. **A1**

6.102.4.3 Multi-part testing

For synthetic methods of testing circuit-breakers fitted with breaking resistors, see Annex F.

Opening operations of circuit-breakers with closing resistors require no special testing techniques since the closing resistor will not influence the test circuit.

The closing resistors can only be tested in a direct circuit that provides the correct current and voltage stresses from a single power source.

During the synthetic making tests it is necessary to remove the closing resistor in order to obtain the correct short-circuit current stresses and pre-arcing conditions in the main interrupter.

6.102.10 Demonstration of arcing times

The basic requirements to be met are given in 6.102.10 of IEC 62271-100.

In order to be able to perform synthetic tests on the same basis as direct tests, normally it will be necessary to apply special re-ignition methods to prolong the arcing of the test circuit-breaker through the necessary number of zeros of the power-frequency current. See Annex H for re-ignition methods to prolong arcing.

The "step-by-step" method described in Annex H is the method used on most synthetic tests. The method is considered to be a sufficiently close approximation of the direct testing procedure.

The arcing is prolonged by means of thermal re-ignitions. As this method makes it possible to force the test circuit-breaker to re-ignite in all conditions, special care shall be taken not to re-ignite the circuit-breaker at the instant of a current zero when the circuit-breaker can clear. For this purpose it is necessary to determine, for each terminal fault, short-line fault and out-of-phase test duty, the minimum arcing time of the circuit-breaker. At least two breaking tests, one clearance and one re-ignition, are necessary for this determination.

The clearance at the minimum arcing time is the first valid breaking operation. The other test is performed to demonstrate that a re-ignition at an early current zero would take place between the arcing contacts.

NOTE 1 The extra tests necessary to demonstrate correct behaviour at early current zeros will usually contribute insignificantly to contact wear, etc., due to the short arcing times. Therefore, no re-conditioning should be necessary because of these tests.

NOTE 2 The re-ignition(s) obtained when determining the minimum arcing time do(es) not indicate a failure of the circuit-breaker. However, it is important to establish that this re-ignition has taken place between the arcing contacts only. When using a current injection method, the interruption of the injected current a few loops after the re-ignition is often a useful means for the judgement. Thorough inspection of screens, arcing and main contacts, etc., should also be made to verify correct behaviour.

6.102.10.1 Three-phase tests

Depending on the test circuit used, the test procedures given here may not cover the conditions of the 3rd pole-to-clear for solidly earthed systems ($k_{pp} = 1,3$). For this case the same procedures may be applied, with the manufacturer's consent, by combining the TRV and di/dt parameters for the 2nd pole-to-clear and the arcing time corresponding to the 3rd pole-to-clear. Alternatively, an additional test may be performed with the TRV, di/dt and the maximum arcing time corresponding to the 3rd pole-to-clear.

For alternative testing procedures of multi-enclosure type circuit-breakers with operating mechanism characteristics that require three-phase current, see Annex K.

6.102.10.1.1 Test duties T10, T30, T60, T100s(b)

The test procedure is as follows:

For convenience of testing, the pole in phase A is kept as the first-pole-to-clear.

First the minimum arcing time and correct re-ignition behaviour are established. This is done by changing the setting of the tripping impulse in steps of 18° (possibly this has to be repeated several times). After having done so, the setting of the control of the tripping impulse has to be advanced by approximately 40°, starting from the shortest arcing time at which the circuit-breaker cleared. For the last test, the setting of the control of the tripping impulse has to be advanced by approximately 20°, starting from the shortest arcing time at which the circuit-breaker cleared.

- First valid breaking operation: $t_{arc\ min}$, minimum arcing time in phase A;
- Re-ignition test: $t_{arc\ reig} = t_{arc\ min} - 18^\circ$, re-ignition in phase A;
- Second valid breaking operation: $t_{max} = t_{arc\ min} + 40^\circ$, longest arcing time in phase A;
- Third valid breaking operation: $t_{med} = t_{arc\ min} + 20^\circ$, medium arcing time in phase A.

The first valid breaking operation and re-ignition test consist of single opening operations. The second and third valid breaking operations are carried out as part of the rated operating sequence. If the rated operating sequence is CO-15s-CO the third valid breaking operation is not required (see 6.102.10 of IEC 62271-100).

For comparison with the arcing time settings used in three-phase direct tests, see Figure 7.

6.102.10.1.2 Test duty T100a

The test procedure is as follows:

All tests consist of single opening operations.

In order to simplify the test procedure, the pole in phase A is kept as the first-pole-to-clear, but the pole in phase C will be subjected to increased electrical wear. In order to obtain similar electrical wear on the poles of phases B and C, the tests can be performed by exchanging the poles of phases B and C for the third valid breaking operation.

First the minimum arcing time (first valid breaking operation) and re-ignition behaviour are established with the major extended loop occurring in phase C. This is done by changing the setting of the tripping impulse in steps of 18° (possibly this has to be repeated several times).

The second valid breaking operation is carried out with the required asymmetry changed to phase A, hence both the initiation of short-circuit current and the setting of the tripping impulse shall be advanced by 60° with reference to the re-ignition test.

The third valid breaking operation is set with the required asymmetry in phase C. The initiation of the short-circuit current is delayed by 60° while the tripping impulse is advanced by 10°, with reference to the second valid breaking operation.

- First valid breaking operation: $t_{\text{arc min}}$
 - minimum arcing time in phase A,
 - required asymmetry conditions in phase C;
- Re-ignition test: $t_{\text{arc reig}} = t_{\text{arc min}} - 18^\circ$
 - re-ignition in phase A,
 - required asymmetry conditions in phase C;
- Second valid breaking operation: $t_{\text{arc max major}}$ in the first-pole-to-clear
 - both the initiation of the short-circuit current and the setting of the tripping impulse advanced by 60°, with reference to $t_{\text{arc reig}}$,
 - required asymmetry conditions in phase A;
- Third valid breaking operation: $t_{\text{arc max major extended}}$
 - maximum arcing time in phase A,
 - required asymmetry conditions in phase C;
 - initiation of the short-circuit current delayed by 60° and the setting of the tripping impulse advanced by 10°, with reference to $t_{\text{arc max major}}$.

The order of the tests given is for convenience only.

For comparison with the arcing time settings used in three-phase direct tests, see Figure 8.

The second and third valid breaking operations can be interchanged as follows:

- Second valid breaking operation: $t_{\text{arc max major extended}}$
 - maximum arcing time in phase A,
 - required asymmetry conditions in phase C,
 - the setting of the tripping impulse advanced by 70°, with reference to $t_{\text{arc reig}}$;
- Third valid breaking operation: $t_{\text{arc max major}}$ in the first-pole-to-clear:
 - initiation of short-circuit current advanced by 60° and the setting of the tripping impulse delayed by 10° with reference to $t_{\text{arc max major extended}}$;
 - required asymmetry conditions in phase A.

Since some circuit-breakers will not clear after a major loop, a test is still valid if the circuit-breaker interrupts at the subsequent minor loop.

NOTE For some types of circuit-breaker, it may appear that for the third valid test ($t_{\text{arc max major extended}}$), the minor loop of current at the previous current zero could already be cleared in phase B. This is not verified in the above described procedure, but can be checked by delaying both the initiation of short-circuit and the setting of the tripping impulse by 60°, with reference to $t_{\text{arc max major extended}}$. Hence, if clearance occurs at the previous minor loop, the third valid test may be repeated with a shorter arcing time depending on the arcing time at which the circuit-breaker will not clear this minor loop of current.

6.102.10.2 Single-phase tests in substitution for three-phase conditions

The procedures as described in 6.102.10.2 of IEC 62271-100 are applicable.

6.102.10.2.5 Splitting of test duties in test series, taking into account the associated TRV for each pole-to-clear

The procedures as described in 6.102.10.2.5 of IEC 62271-100 are applicable and the test procedure for synthetic testing is given in Annex L.

6.104.5.4 Test duty T30

For rated voltages up to and including 72,5 kV it may be difficult to meet the small values of t_3 . The shortest time which can be met should be used, but not less than the values specified in Table 13 of IEC 62271-100. The values used shall be stated in the test report.

6.104.5.5 Test duty T10

For rated voltages up to and including 72,5 kV it may be difficult to meet the small values of t_3 . The shortest time which can be met should be used, but not less than the values specified in Table 13 of IEC 62271-100. The values used shall be stated in the test report.

6.106 Basic short-circuit test duties

The basic requirements are given in 6.106 of IEC 62271-100. The synthetic test methods are given in Table 3.

Abbreviations used in 6.106 and Table 3 are given below.

Cd	Closing operation in a direct circuit at the voltage of the current source which can be less than the voltage specified in 6.104.1 of IEC 62271-100
Cs	Closing operation with specified parameters in a synthetic circuit
Cd _{asy}	Closing operation against the rated short-circuit making current according to 6.104.2. of IEC 62271-100 in a direct circuit at conditions described under Cd
Cs _{sym}	Closing operation against a symmetrical current equal to the rated short-circuit breaking current, carried out at the required applied voltage in a synthetic circuit
Od	Breaking operation at the voltage of the current source only and with the specified breaking current
Os	Breaking operation with specified parameters in a synthetic circuit
t	Time interval between operations (0,3 s or 3 min depending on the rated operating sequence)
t'	Time interval between operations (3 min)
t''	Time interval between operations (15 s)
SP	Single-phase test as defined in 6.108 of IEC 62271-100
DEF	Double earth fault test as defined in 6.108 of IEC 62271-100

NOTE 1 Due to the characteristics of synthetic testing it may be difficult to comply with the specified time intervals of the rated operating sequence. See 6.105.1 of IEC 62271-100.

NOTE 2 In order to comply with all test requirements, it may be necessary to make more operations than specified in the normal test duty. In such cases the circuit-breaker may be reconditioned and the test duty repeated.

6.106.1 Test duty T10

Several procedures may be used to perform the rated operating sequence synthetically with the specified parameters (see Table 3).

6.106.2 Test duty T30

Several procedures may be used to perform the rated operating sequence synthetically with the specified parameters (see Table 3).

6.106.3 Test duty T60

Several procedures may be used to perform the rated operating sequence synthetically with the specified parameters (see Table 3).

6.106.4 Test duty T100s

Several procedures may be used to perform the rated operating sequence synthetically with the specified parameters (see Table 3), as follows.

6.106.4.1 Time constant of the d.c. component of the test circuit equal to the specified value

One of the following methods shall be used when the time constant of the test circuit is equal to the specified value used for the rated short-circuit breaking current as defined by 4.101.2 of IEC 62271-100.

Method 1

The preferred procedure is to carry out the complete rated operating sequence as follows:

$$\begin{aligned} &Os - t - Cs \quad Os - t' - Cs \\ &Os \text{ or} \\ &CsOs - t'' - CsOs \end{aligned}$$

with one Cs meeting requirement a) and the other Cs meeting requirement b) of 6.104.2.1 of IEC 62271-100.

Method 2

The procedure is to carry out the complete rated operating sequence as follows:

$$\begin{aligned} &Os \text{ followed by} \\ &Od - t - Cs_{sym} \quad Os - t' - Cd_{asy} \quad Os \text{ or} \\ &Cs_{sym} \quad Od - t'' - Cd_{asy} \quad Os \end{aligned}$$

with Od having the same minimum arcing time condition as the previous Os and Cd_{asy} meeting requirement b) of 6.104.2.1 of IEC 62271-100.

The purpose of the first Os is

- to comply with the requirement to have the specified number of breaking operations at the specified values,
- to provide the necessary information to enable the control of the tripping impulse to be set for the relevant requirements during the subsequent operating sequence. This enables the minimum arcing time conditions to be established, as if direct tests were performed at specified values. These conditions have to be reproduced during the Od operation in the subsequent operating sequence.

The purpose of the Cs_{sym} is to meet requirement a) of 6.104.2.1 of IEC 62271-100; closing against a symmetrical current as a result of the pre-arcing commencing at the peak of the applied voltage.

Method 3

The procedure is to carry out the complete rated operating sequence as follows:

$$\begin{aligned} &Cs_{sym} \text{ and } Os \text{ followed by} \\ &Od - t - CdOs - t' - CdOs \text{ or} \\ &CdOd - t'' - CdOs \end{aligned}$$

with Od having the same minimum arcing time condition as the previous Os and one of the two Cd 's meeting requirement b) of 6.104.2.1 of IEC 62271-100.

The purpose of the first Os is

- to comply with the requirement to have the specified number of breaking operations at the specified values,
- to provide the necessary information to enable the control of the tripping impulse to be set for the relevant requirements during the subsequent operating sequence. This enables the minimum arcing time conditions to be established, as if direct tests were performed at specified values. These conditions have to be reproduced during the Od operation in the subsequent operating sequence.

The purpose of the Cs_{sym} is to meet requirement a) of 6.104.2.1 of IEC 62271-100; closing against a symmetrical current as a result of the pre-arcing commencing at the peak of the applied voltage.

6.106.4.2 Time constant of the d.c. component of the test circuit less than the specified value

One of the following methods shall be used when the time constant of the test circuit is less than the specified value used for the rated short-circuit breaking current according to 4.101.2 of IEC 62271-100.

Method 1

The procedure is to carry out the complete rated operating sequence as follows:

$$\begin{aligned} &Cd_{asy} \text{ and } Os \text{ followed by} \\ &Od - t - Cs_{sym}Os - t' - CdOs \text{ or} \\ &Cs_{sym}Od - t'' - CdOs \end{aligned}$$

with Od having the same minimum arcing time condition as the previous Os and Cd_{asy} meeting requirement b) of 6.104.2.1 of IEC 62271-100.

The purpose of the first Os is

- to comply with the requirement to have the specified number of breaking operations at the specified values,
- to provide the necessary information to enable the control of the tripping impulse to be set for the relevant requirements during the subsequent operating sequence. This enables the minimum arcing time conditions to be established, as if direct tests were performed at specified values. These conditions have to be reproduced during the Od operation in the subsequent operating sequence.

The purpose of the Cs_{sym} is to meet requirement a) of 6.104.2.1 of IEC 62271-100; closing against a symmetrical current as a result of the pre-arcing commencing at the peak of the applied voltage.

Method 2

The procedure is to carry out the complete rated operating sequence as:

Cd_{asy}, Cs_{sym} and Os followed by

$Od - t - CdOs - t' - CdOs$ or

$CdOd - t'' - CdOs$

with Od having the same minimum arcing time condition as the previous Os and Cd_{asy} meeting requirement b) of 6.104.2.1 of IEC 62271-100.

The purpose of the first Os is

- to comply with the requirement to have the specified number of breaking operations at the specified values,
- to provide the necessary information to enable the control of the tripping impulse to be set for the relevant requirements during the subsequent operating sequence. This enables the minimum arcing time conditions to be established, as if direct tests were performed at specified values. These conditions have to be reproduced during the Od operation in the subsequent operating sequence.

The purpose of the Cs_{sym} is to meet requirement a) of 6.104.2.1 of IEC 62271-100; closing against a symmetrical current as a result of the pre-arcing commencing at the peak of the applied voltage.

6.106.4.3 Time constant of the d.c. component of the test circuit greater than the specified value

One of the following methods shall be used when the time constant of the test circuit is greater than the specified value used for the rated short-circuit breaking current according to 4.101.2 of IEC 62271-100.

Method 1

The procedure is to carry out the complete rated operating sequence as follows:

Os followed by

$Od - t - Cs_{sym}Os - t' - Cd_{asy}Os$ or

$Cs_{sym}Od - t'' - Cd_{asy}Os$

with Od having the same minimum arcing time condition as the previous Os and Cd_{asy} , meeting requirement b) of 6.104.2.1 of IEC 62271-100.

The purpose of the first Os is

- to comply with the requirement to have the specified number of breaking operations at the specified values,
- to provide the necessary information to enable the control of the tripping impulse to be set for the relevant requirements during the subsequent operating sequence. This enables the minimum arcing time conditions to be established, as if direct tests were performed at specified values. These conditions have to be reproduced during the Od operation in the subsequent operating sequence.

The purpose of the Cs_{sym} is to meet requirement a) of 6.104.2.1 of IEC 62271-100, closing against a symmetrical current as a result of the pre-arcing commencing at the peak of the applied voltage.

Method 2

The procedure is to carry out the complete rated operating sequence as follows:

Cs_{sym} and Os followed by
 $Od - t - CdOs - t' - CdOs$ or
 $CdOd - t'' - CdOs$

with Od having the same minimum arcing time condition as the previous Os and one of the two Cd meeting requirement b) of 6.104.2.1 of IEC 62271-100.

The purpose of the first Os is

- to comply with the requirement to have the specified number of breaking operations at the specified values,
- to provide the necessary information to enable the control of the tripping impulse to be set for the relevant requirements during the subsequent operating sequence. This enables the minimum arcing time conditions to be established, as if direct tests were performed at specified values. These conditions have to be reproduced during the Od operation in the subsequent operating sequence.

The purpose of the Cs_{sym} is to meet requirement a) of 6.104.2.1 of IEC 62271-100, closing against a symmetrical current as a result of the pre-arcing commencing at the peak of the applied voltage.

6.106.5 Test duty T100a

Three breaking operations shall be made as specified in 6.106.5 of IEC 62271-100 (see Table 3).

During tests with asymmetrical current both di/dt and the TRV are modified due to the d.c. component. In synthetic tests these modifications have to be pre-arranged as follows:

- a) Depending on the required d.c. time constant, the following asymmetry criteria have to be fulfilled as given below and in IEC 62271-308:
- last current loop amplitude;
 - last current loop duration;
 - percentage of d.c. component at current zero (parameter controlling the di/dt and the following TRV parameters).

Several test parameters shall be simultaneously reproduced during T100a in order to obtain a valid interruption.

Values for the duration and amplitude of the last loop and the percentage of d.c. component at final current zero can be found in Tables I.1a to I.2d of Annex I.

The prospective percentage of d.c. component at current zero shall be calculated from the percentage d.c. component at contact separation during the test and from the d.c. time constant of the test circuit. The d.c. time constant of the test circuit shall be measured from the oscillogram of a prospective current calibration test in the region corresponding

to the instant of contact separation. The instant of initiation of the short-circuit during the actual tests and during the prospective current calibration test shall be within $\pm 10^\circ$.

For the prospective current calibration test, it is necessary to extend the duration of the current by at least an extra current loop in order to be able to measure accurately the prospective percentage of d.c. component at the predicted current zero.

NOTE 1 The percentage of d.c. component at current zero during actual tests can also be calculated by the following formula:

$$p_0 = p_{cs} \times \exp\left(-\frac{t_a}{\tau}\right)$$

where

p_0 is the percentage of d.c. component at current zero during the actual test;

p_{cs} is the percentage of d.c. component at contact separation measured during the actual test;

t_a is the arcing time;

τ is the d.c. time constant of the test circuit measured during the prospective current calibration test.

The applicable asymmetry criteria for each particular test method are described in 5.2. of IEC 62271-308.

b) Reduction of di/dt at current zero

The reduction of di/dt may be obtained for current injection methods by reducing the charging voltage of the voltage circuit.

The corresponding corrected values can be found in [\[A1\]](#) Tables 15 through 22 of IEC 62271-100:2008 [\[A1\]](#) for the first-pole-to-clear condition and in Tables I.3a and I.3b for the second pole-to-clear condition in the phase having the full asymmetrical current.

c) Correction of TRV

1) Simplified method

For TRVs with time t_2 or t_3 not exceeding 500 μs , a simplified method can be used.

The charging voltage of the synthetic circuit should be set to obtain the most onerous test parameters. For tests on the minor loop it is u_c , and for the major loop di/dt .

2) For TRVs with time t_2 exceeding 500 μs , other corrections and/or circuit modifications have to be used. For the required prospective TRV values see Tables I.4a through I.4d.

NOTE 2 Different test circuits for major and minor loops may be needed in order to realise the required values. A test with one single test circuit may over-stress the circuit-breaker and requires the consent of the manufacturer.

d) Correction of recovery voltage

When a test is made for clearance at the end of a major loop, the reduced recovery voltage will adequately cover the first quarter loop of the recovery voltage (of an equivalent direct test).

For clearance at the end of a minor loop of current, the reduced recovery voltage will not cover reference system conditions since in the system the power-frequency recovery voltage continues to rise after the onset of the TRV.

Together with the symmetrical test duties, the evidence is sufficient to prove the performance of the circuit-breaker.

6.108 Single-phase and double-earth fault tests

The basic test requirements are given in 6.108 of IEC 62271-100. The test method is shown in Table 3.

6.109 Short-line fault (SLF) tests

The basic test requirements are given in 6.109 of IEC 62271-100.

The test methods for SLF tests are shown in Table 3.

The final current loop before clearing shall have an amplitude equal to the test current times $\sqrt{2}$ with a tolerance of $\pm 10\%$ including the provisions of 4.1.1.

For short-line fault synthetic testing, the parameters of the short-line fault circuit shall be those given in 4.105 of IEC 62271-100 and the line circuit shall be in the current-carrying circuit during the whole interaction interval.

With current injection circuits, the short-line fault circuit may be connected in series with the voltage circuit and its inductance is added to L_h , as shown in Figure B.1.

The presence of the short-line fault circuit in the voltage circuit may cause oscillations to be superimposed on the injected current wave. These oscillations should be damped out (to satisfy d) of 4.2.1), so as not to affect the current during the interval of significant change of arc voltage or at least 100 μs before current zero.

A resistance may be connected in series with the TRV shaping circuit. In most cases this resistance, selected to control the initial rate of rise of recovery voltage, is sufficient to supply the necessary damping.

NOTE 1 If, for short-line fault tests, the line is connected to the same side of the test circuit-breaker as the voltage circuit impedance, special attention should be given to voltage distribution and measurement of prospective TRV.

If an extra capacitance is used to adjust the time delays as per 6.109.3 of IEC 62271-100, care should be taken as to where to apply this capacitance:

- when using a line side capacitance, it shall be connected across the line section of the test circuit to simulate the same conditions as in direct tests;
- when using a source side capacitance, it shall be connected across the source section of the voltage circuit.

NOTE 2 A capacitance across the circuit-breaker is normally considered as being part of the test object. In certain cases it may be necessary to apply additional capacitance across the circuit-breaker to adjust the time delay of the test circuit.

NOTE 3 A capacitance across the auxiliary circuit-breaker influences the time delay and is considered as being part of the delay capacitance of the test circuit.

6.110 Out-of-phase making and breaking tests

The basic requirements are given in 6.110 of IEC 62271-100.

The test methods for OP1 and OP2 are given in Table 3.

Table 3 – Synthetic test methods for test duties T10, T30, T60, T100s, T100a, SP, DEF, OP and SLF

Test duty	Synthetic test		Rated operating sequence	
	Subclause	Method	$O - t - CO - t' - CO$ $t = 0,3 \text{ s or } 3 \text{ min}$ $t' = 3 \text{ min}$	$CO - t'' - CO$ $t'' = 15 \text{ s}$
T10, T30 and T60	6.106.1 to 6.106.3	1	$Os - t - (Cd)Os - t' - (Cd)Os^a$	$(Cd)Os - t'' - (Cd)Os^a$
		2	Os $Od - t - (Cd)Os - t' - (Cd)Os^a$	Os $(Cd)Od - t'' - (Cd)Os^a$
T100s	6.106.4.1 time constant of the d.c. component of the test circuit equal to the specified value	1	$Os - t - CsOs - t' - CsOs$	$CsOs - t'' - CsOs$
		2	Os $Od - t - Cs_{sym}Os - t' - Cd_{asy}Os$	Os $Cs_{sym}Od - t'' - Cd_{asy}Os$
		3	Cs_{sym} Os $Od - t - CdOs - t' - CdOs^d$	Cs_{sym} Os $CdOd - t'' - CdOs^d$
	6.106.4.2 time constant of the d.c. component of the test circuit less than the specified value	1	Cd_{asy} Os $Od - t - Cs_{sym}Os - t' - CdOs^b$	Cd_{asy} Os $Cs_{sym}Od - t'' - CdOs^b$
		2	Cd_{asy} Cs_{sym} Os $Od - t - CdOs - t' - CdOs^b$	Cd_{asy} Cs_{sym} Os $CdOd - t'' - CdOs^b$
	6.106.4.3 time constant of the d.c. component of the test circuit greater than the specified value	1	Os $Od - t - Cs_{sym}Os - t' - Cd_{asy}Os^c$	Os $Cs_{sym}Od - t'' - Cd_{asy}Os^c$
		2	Cs_{sym} Os $Od - t - CdOs - t' - CdOs^{c, d}$	Cs_{sym} Os $CdOd - t'' - CdOs^{c, d}$
T100a	6.106.5		$Os - t' - Os - t' - Os$	
SP and DEF	6.108		Os	
SLF	6.109	1	$Os - t - (Cd)Os - t' - (Cd)Os^a$	
		2	Os $Od - t - (Cd)Os - t' - (Cd)Os^a$	
OP1	6.110		Os, Os, Os	
OP2	6.110	1	$Cs_{sym}Os, Os, Os$	
		2	Cs_{sym} $(Cd)Os, Os, Os^a$	

^a (Cd) is a closing operation as Cd, which may be carried out under no-load conditions.

^b Due to the smaller time constant of the d.c. component of the test circuit with respect to the specified value used for the rated short-circuit breaking current, the symmetrical value of the current during Cd_{asy} will need to be greater than the rated value. During the Cd for the same reason, the current peak, already demonstrated during Cd_{asy} will be smaller than the rated short-circuit making current.

^c Due to the larger time constant of the d.c. component of the test circuit with respect to the specified value used for the rated short-circuit, the current peak during the asymmetrical closing can be larger than the rated short-circuit making current. A peak current reduction circuit can be used or the closing operation may be controlled by use of point on wave control, to obtain the required rated short-circuit making current. The use of point-on-wave control is subject to the consent of the manufacturer.

^d One of the two Cd's shall be Cd_{asy} .

6.111 Capacitive-current switching tests

The basic requirements are given in 6.111 of IEC 62271-100. ^[A1] For metal-enclosed and dead tank circuit-breakers, typical test circuits are given in Annex N and additional guidelines are given in Annex O of IEC 62271-100:2008. ^[A1]

6.111.2 General

A test circuit with a 50 Hz current circuit may be used to prove the capacitive current switching capability for a rating of 60 Hz, provided that the recovery voltage fulfils the 60 Hz requirements (see note 4 of 6.111.2 of IEC 62271-100). The setting of the contact separation should be based on the frequency of the current source. However, the minimum arcing time is determined by changing the setting of the contact separation on opening by periods of approximately 6° based on the rated frequency of the circuit-breaker under test.

6.111.3 Characteristics of supply circuits

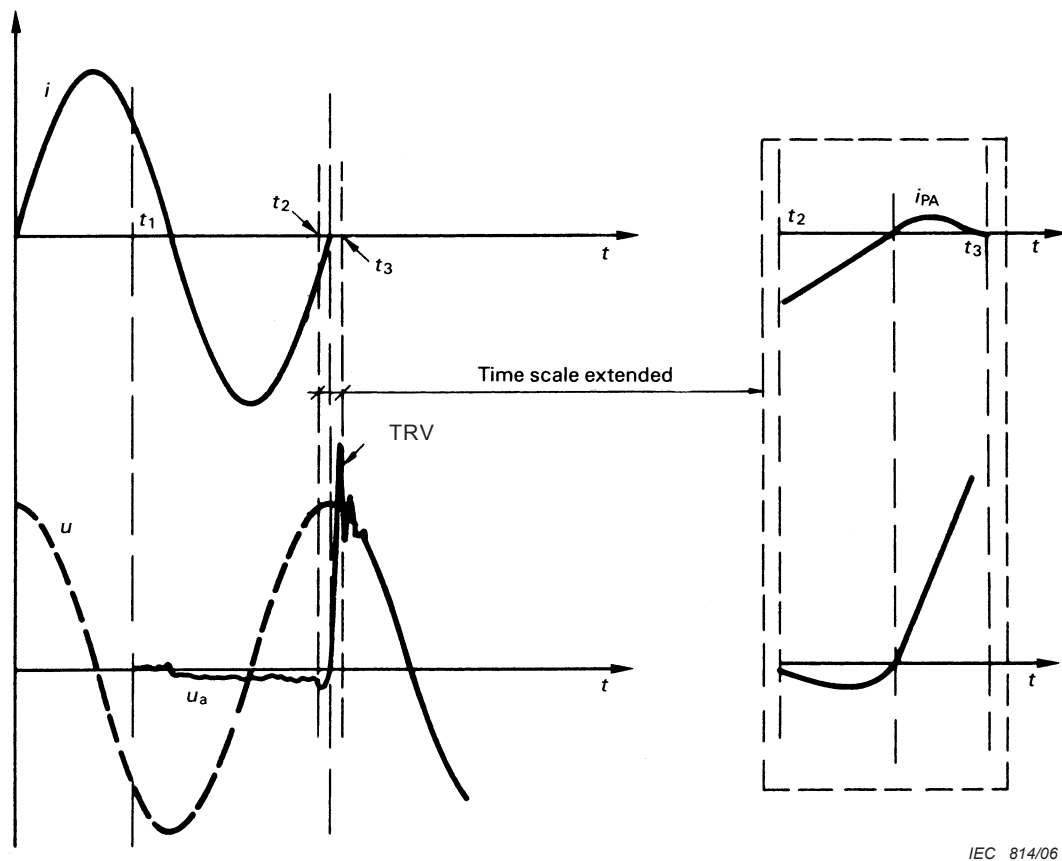
When the characteristics of the test circuit do not meet the requirements of 6.111.3 of IEC 62271-100, the prospective recovery voltage specified in 6.111.10 of IEC 62271-100 shall be applied.

NOTE The effects of current chopping, as described in Clause G.2, may modify the recovery voltage during the capacitive-current switching tests.

6.111.7 Test voltage

For single-phase synthetic capacitive current switching tests, the test voltage specified for direct tests in 6.111.7 of IEC 62271-100 shall be applied.

Examples of synthetic capacitive-current switching circuits are given in Annex G.

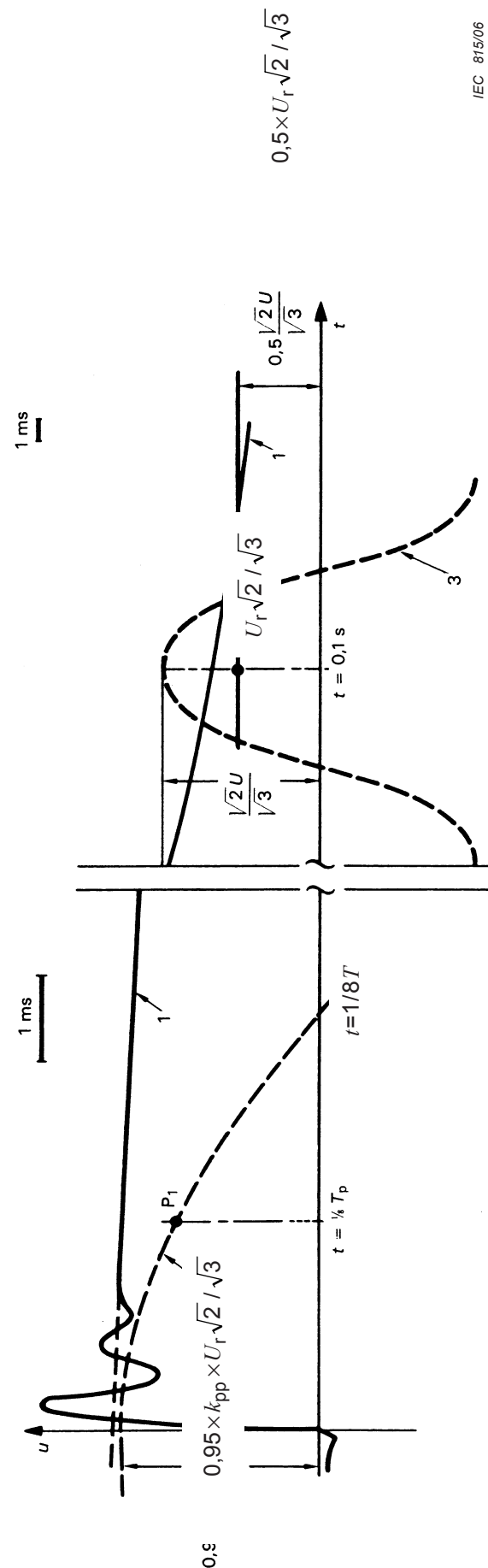


IEC 814/06

Key

i	breaking current	t_2	start of significant change in arc voltage
u	power-frequency voltage	t_3	instant of cessation of post-arc current
u_a	arc voltage	$t_2 - t_1$	high-current interval
TRV	transient recovery voltage	$t_3 - t_2$	interaction interval
i_{PA}	post-arc current	After t_3	high-voltage interval
t_1	instant of contact separation		

Figure 1 – Interrupting process – Basic time intervals

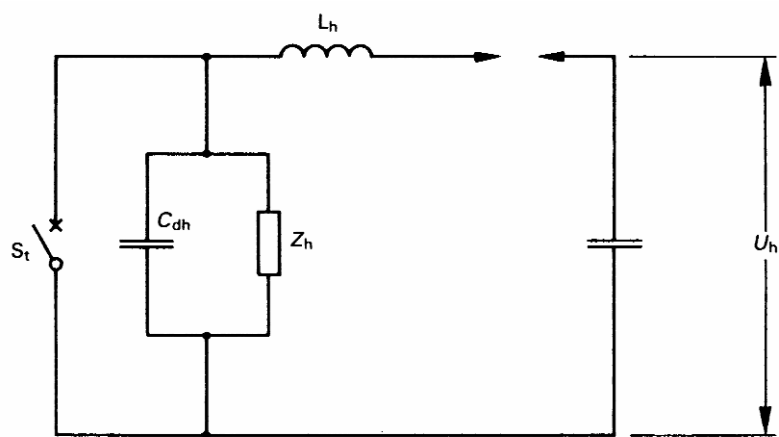


IEC 815/06

Key

- | | | | |
|---|--|----------------|--|
| 1 | recovery voltage with exponential decrement across the circuit-breaker during a synthetic test | P ₁ | point to which the recovery-voltage (1) shall not fall below the specified value (2) |
| 2 | power-frequency recovery voltage of the first extinguishing pole in the equivalent direct test, e.g. first-pole-to-clear factor $k_{pp} = 1,3$ | P ₂ | point below which the recovery-voltage (1) shall not fall during a synthetic test |
| 3 | power-frequency recovery voltage after interruption of currents in all three poles in the equivalent direct test | T | power frequency period |

Figure 2 – Example of recovery voltage



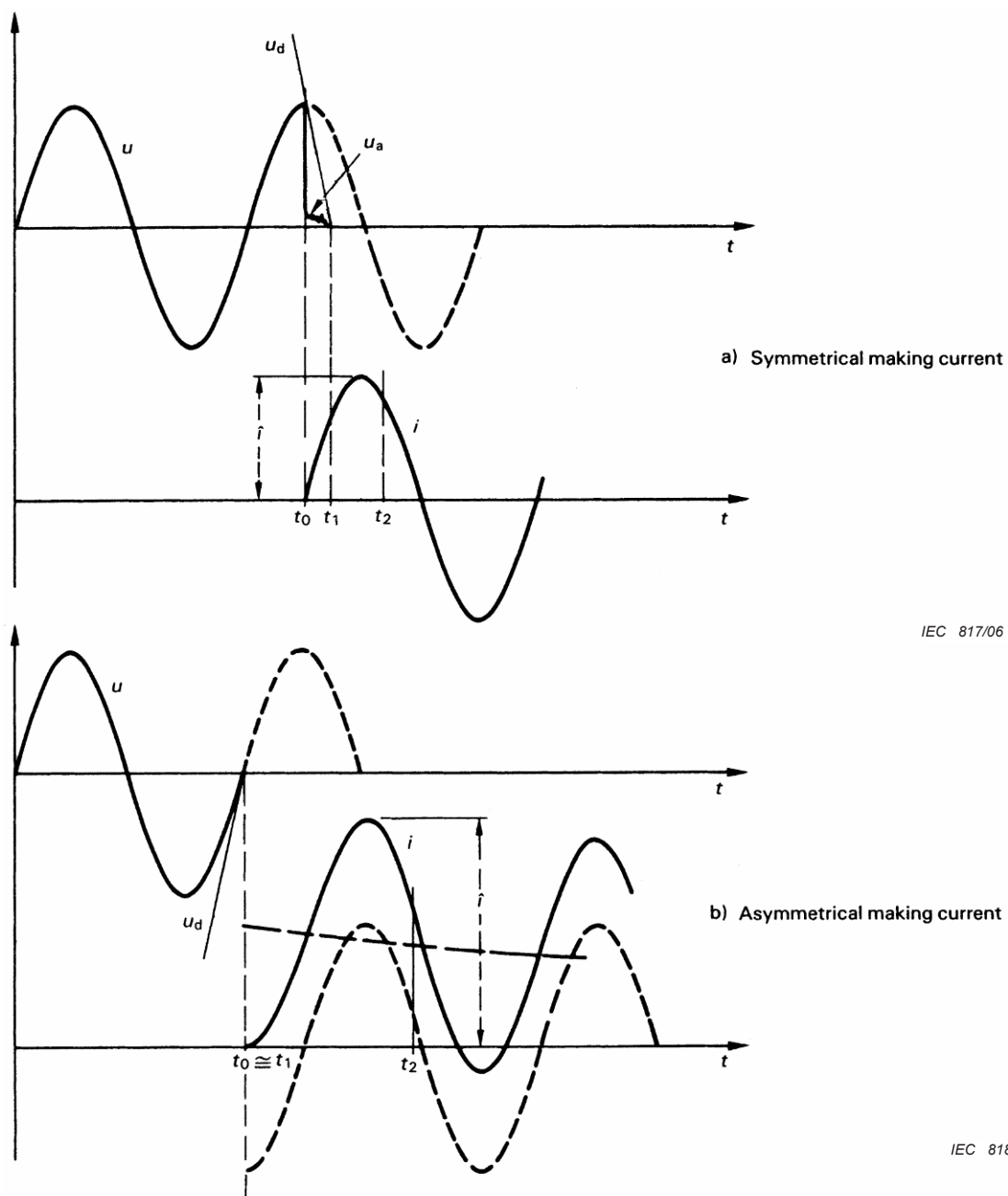
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IEC 816/06

Key

- U_h charging voltage of voltage circuit
- L_h inductance of voltage circuit
- Z_h equivalent surge impedance
- C_{dh} capacitance for time delay of voltage circuit
- S_t test circuit-breaker

**Figure 3 – Equivalent surge impedance of the voltage circuit
for the current injection method**



Key

i	current	u_a	arc voltage
$\hat{i}$	making current peak	t_0	instant of prestrike
u	power-frequency voltage	t_1	instant of contact touch
u_d	dielectric closing characteristic	t_2	instant of reaching fully closed position

Figure 4 – Making process – Basic time intervals

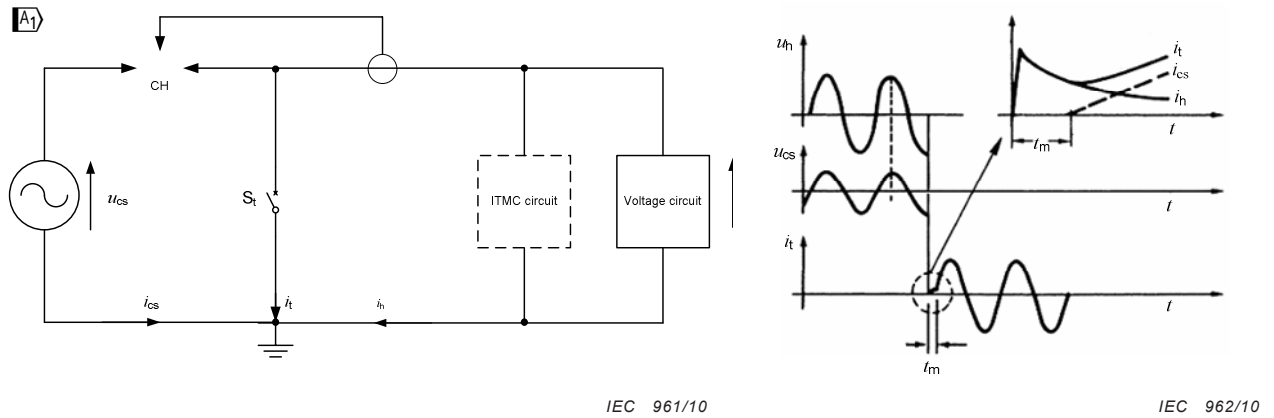


Figure 5a – Synthetic make circuit for terminal fault

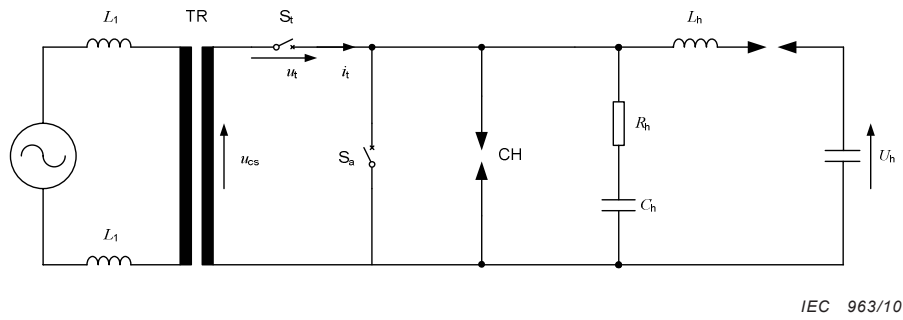


Figure 5b – Synthetic make circuit for out-of-phase (ac + dc method)

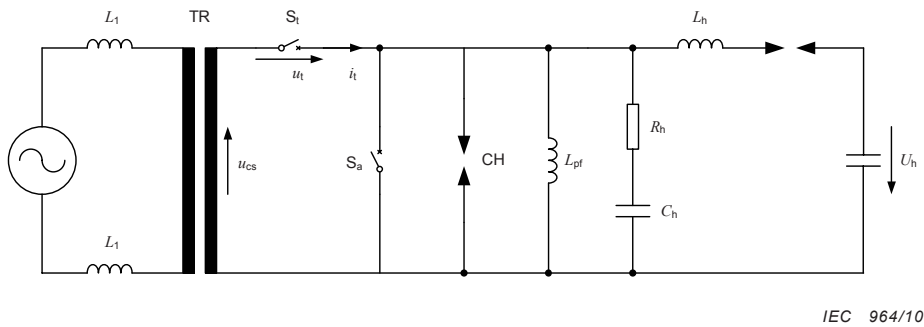
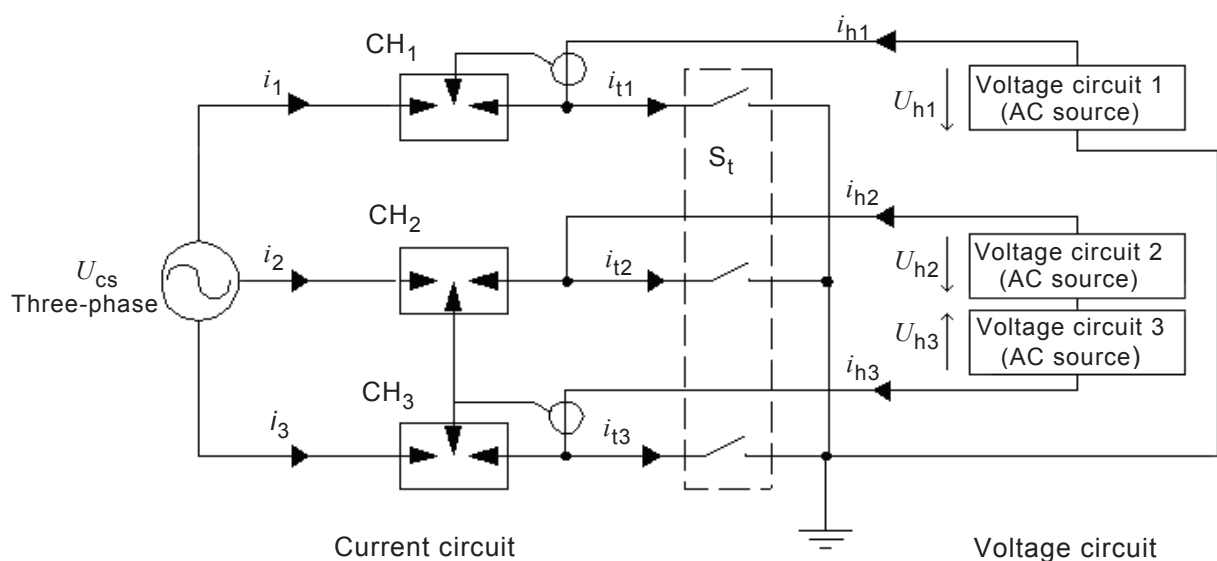


Figure 5c – Synthetic make circuit for out-of-phase (ac + ac method)

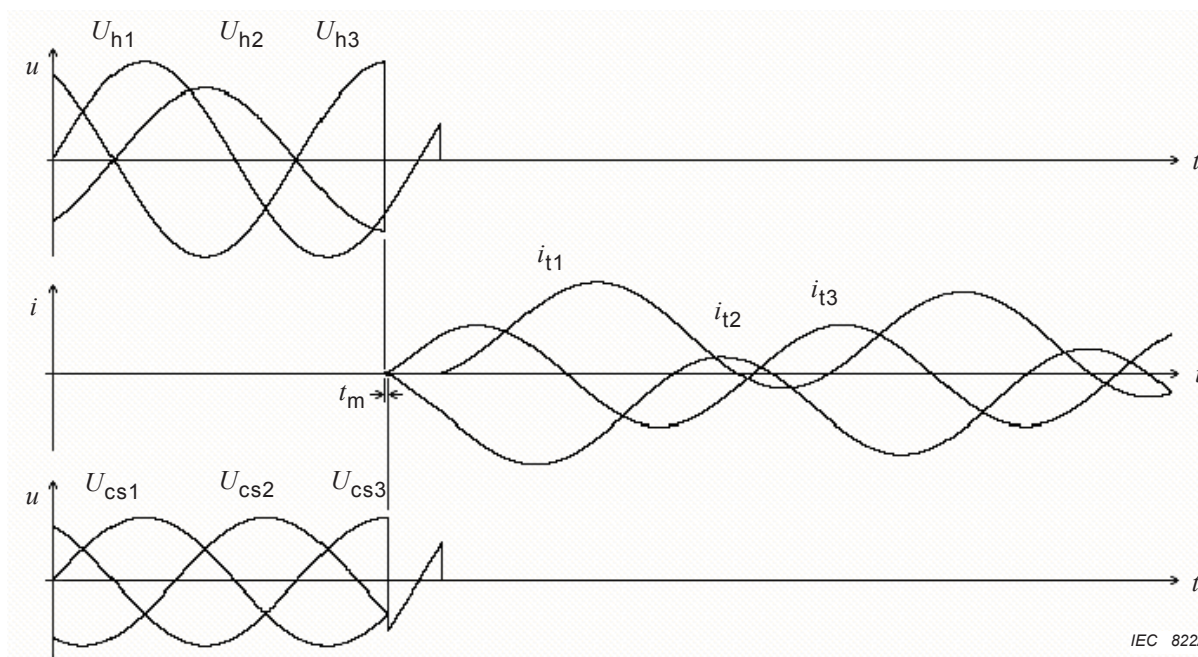
Key

S_a	auxiliary circuit-breaker	i_t	current through S_t
S_t	circuit-breaker under test	L_1	inductance of the current circuit
u_{cs}	voltage of the current circuit	L_h	inductance of the voltage circuit
i_{cs}	current of the current circuit	$R_h C_h$	components of the ITMC circuit
i_h	injected current	L_{pf}	parallel inductance of the voltage circuit
U_h	applied voltage	t_m	time delay of making device
CH	making device (triggered spark gap)		

Figure 5 – Typical synthetic make circuits for single-phase tests



IEC 821/06

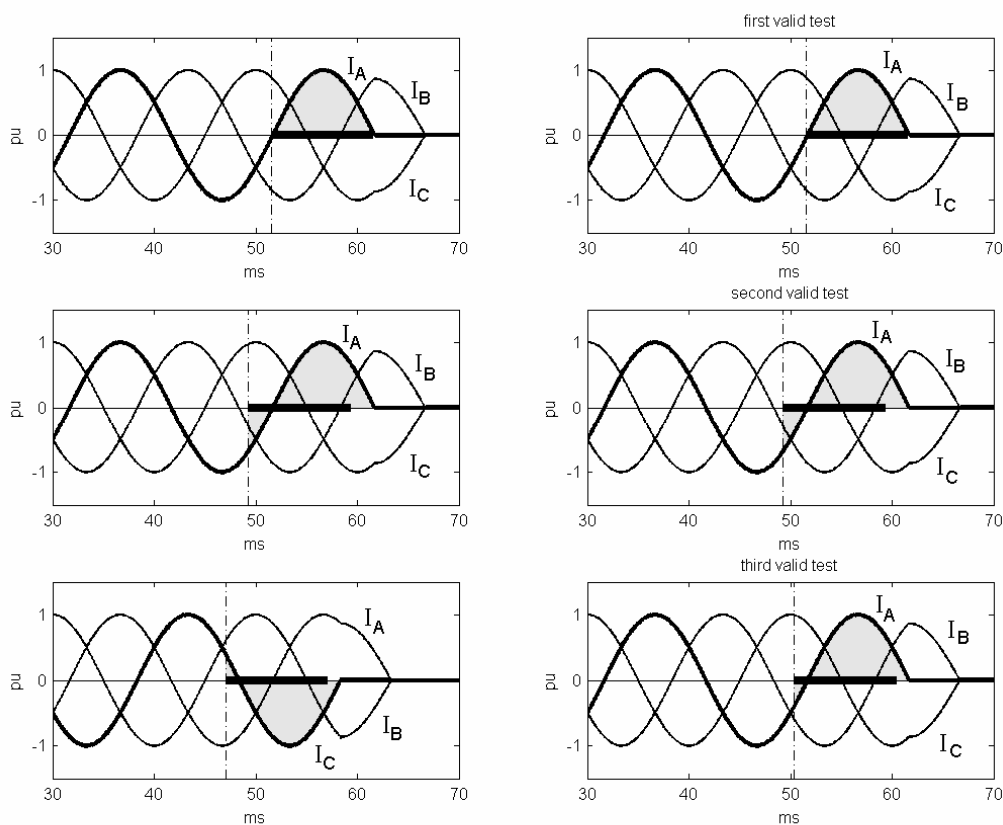


IEC 822/06

Key

$U_{cs1}, U_{cs2}, U_{cs3}$	voltage of current circuit	U_{h1}, U_{h2}, U_{h3}	applied voltage
i_1, i_2, i_3	current supplied by the current circuit	CH_1, CH_2, CH_3	making device
i_{t1}, i_{t2}, i_{t3}	current through the test object	S_t	test circuit-breaker
i_{h1}, i_{h2}, i_{h3}	initial transient making current (ITMC)	t_m	time delay of making device

Figure 6 – Typical synthetic make circuit for three-phase tests ($k_{pp} = 1,5$)

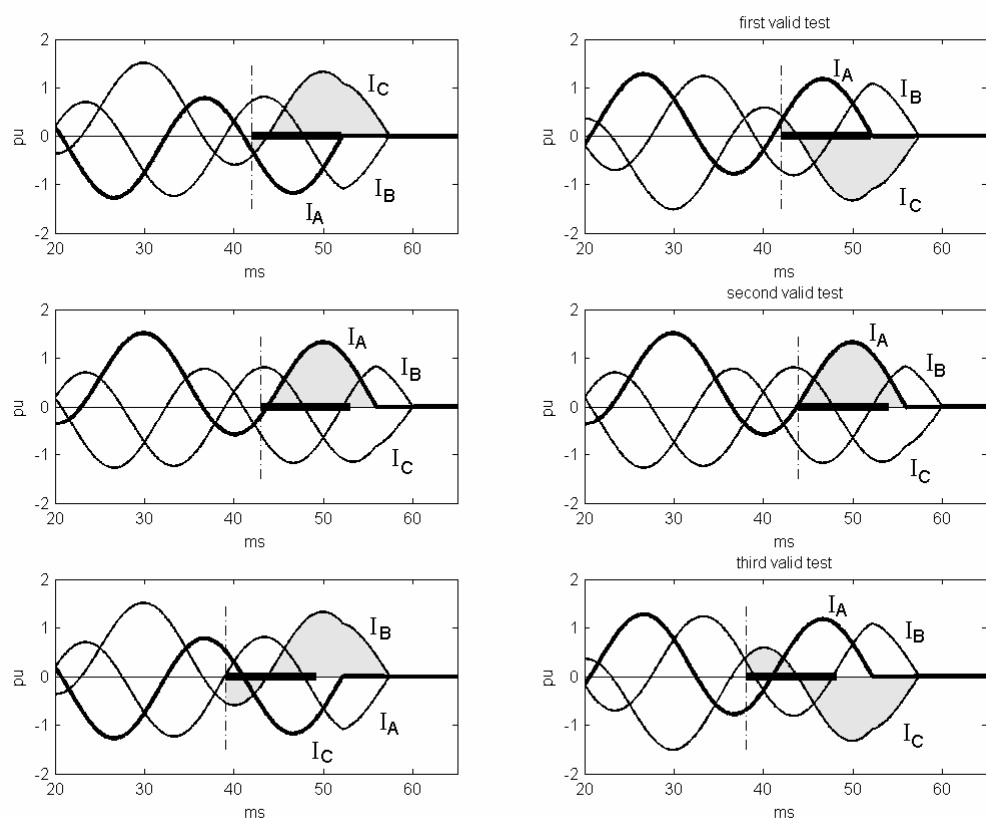


IEC 823/06

NOTE 1 I_A , I_B , I_C : currents in phases A, B and C, respectively.

NOTE 2 The solid horizontal bar is the minimum arcing time.

Figure 7 – Comparison of arcing time settings during three-phase direct tests (left) and three-phase synthetic (right) for T100s with $k_{pp} = 1,5$



IEC 824/06

NOTE 1 I_A , I_B , I_C : currents in phases A, B and C, respectively.

NOTE 2 The solid horizontal bar is the minimum arcing time.

Figure 8 – Comparison of arcing time settings during three-phase direct tests (left) and three-phase synthetic (right) for T100a with $k_{pp} = 1,5$

Annex A (informative)

Current distortion

Current distortion is a well known factor that should be considered during synthetic testing. Clauses A.1, A.2 and A.3 give a basic analysis using simplified methods. In practice digital calculations by computers may be more appropriate where various arc voltage waveshapes can be introduced.

A.1 Current distortion immediately prior to current zero

The interaction interval begins when the arc voltage starts to change significantly as the current approaches zero. The change of the arc voltage during this time influences the shape and the rate-of-change of the current immediately before current zero.

This deviation from the prospective current curve is caused by the distortion current, which mainly flows in the low time constant impedance, taking into account all parameters of the actual circuit.

The particular way in which the current approaches zero is responsible for the physical conditions of the medium between the arcing contacts of a circuit-breaker at current zero. The major interaction between circuit and circuit-breaker is caused by the arc voltage charging and discharging capacitances and influencing di/dt just before zero.

In a simplified circuit, as in Figure A.1 representing a short-circuit in service or a direct test, the voltage u supplies an arc current i with the appropriate arc voltage u_a . Parallel to the arc is a capacitor C .

If it is assumed that the arc voltage $u_a = 0$, then a prospective short-circuit current i_p (see Figure A.2) will flow through the arc, the magnitude and waveshape of this current being determined by the inductance L , the voltage u , the frequency of this voltage and the moment of current initiation.

If it is assumed that the supply voltage $u = 0$ and that an arc voltage exists, then the arc voltage will produce a current flow. This current i_d (see Figure A.3) is the distortion current, which will flow partly as i_{dL} through the inductance L , and partly as i_{dC} through the capacitance C . For this condition, the following equations apply:

$$u_a - L \times \frac{d}{dt}(i_{dL}) = 0$$

and

$$C \frac{d}{dt}(u_a) - i_{dC} = 0$$

From these, the following equation for i_d can be obtained:

$$i_d = i_{dL} + i_{dC} = \frac{1}{L} \int u_a dt + C \times \frac{d}{dt}(u_a)$$

If both of the voltages, u and u_a are present (see Figure A.4), then the resulting actual current is given by:

$$i = i_p - i_d$$

A.2 Current distortion during the high-current interval

During this interval, the arc voltage generates a distortion current i_d , in the circuit. i_d is superimposed on the total current.

By comparison with the prospective current, the resulting arc current exhibits distortion in four physical aspects: current amplitude, loop duration, arc-energy and di/dt .

To evaluate the influence of the arc voltage it is sufficient, in practice, to consider the current amplitude and the loop duration.

As a first approximation, two different arc voltage characteristics can be considered, namely:

- 1) a constant arc voltage $u_a = U_a$
- 2) a linearly rising arc voltage $u_a = S \times t$

Since the current through the capacitor C (see Figure A.1) will be small during this period of arcing, the simplified diagram of Figure A.5 is adequate.

A.2.1 Distortion during one loop of arcing related to a symmetrical current

The following equations are derived, where the resistance in Figure A.5 is neglected since the effect of this during the single loop is negligible. Some results are given in Figure A.8 and A.9.

Calculations are made based on the characteristics shown in Figure A.6 and A.7.

$\hat{u} = \omega L \times \hat{i}_p$	peak value of voltage of current circuit
$\hat{i}_p$	peak value of prospective current
$\hat{i}$	peak value of actual current (reduced by arc voltage)
t_m	instant of peak value $\hat{i}$

a) Ratio of current amplitudes

- for constant arc voltage:

$$\frac{\hat{i}}{\hat{i}_p} = \sin \omega \times t_m - \frac{U_a}{\hat{u}} \times \omega t_m$$

- for linearly rising arc voltage:

$$\frac{\hat{i}}{\hat{i}_p} = \sin \omega \times t_m - \frac{S \omega}{2 \hat{u}} t_m^2$$

b) Actual current loop duration T_1 (reduced by arc voltage)

- for constant arc voltage

$$\sin \omega T_1 = \frac{U_a \omega}{\hat{u}} T_1$$

– for linearly rising arc voltage:

$$\sin \omega T_1 = \frac{S\omega}{2\hat{u}} T_1^2$$

In Figure A.8 and A.9 relative reduction of current amplitude $\Delta i/\hat{i}_p$ and current loop duration $\Delta t/T_p$ are given as a function of ratio $U_a/\hat{u}$ for a constant arc voltage and of ratio $S \times T_a/2 \times \hat{u}$ for a linearly rising arc voltage, respectively, where:

$$\Delta i = \hat{i}_p - \hat{i},$$

$$\Delta t = T_p - T_1$$

T_p = prospective current loop duration

T_a = actual arcing time ($T_a = T_1$ for one loop of arcing, see Figures A.6 and A.7).

A.2.2 Distortion in general case

The distortion currents in the case of both symmetrical and asymmetrical currents including more than one loop of arcing are obtained by the following equations which are applicable for the case of constant and linearly rising arc voltages. These calculations are based on a circuit as in Figure A.5 where the L/R time constant of the supply impedance is introduced. The p.u. prospective current is given by:

$$i_p/\hat{i}_p = \sin(\omega t + \omega t_1 - \varphi) - \sin(\omega t_1 - \varphi) \times e^{-\frac{R}{L}t}$$

where

t time coordinate counting from the instant of current initiation;

t_1 time interval between the beginning of the positive voltage loop and current initiation;

$\varphi = \arctan \frac{\omega L}{R}$ for symmetrical current $\varphi = \omega t_1$.

The per unit distortion currents are

$i_d/\hat{i}_p = C$ for the first loop of arcing,

$i_d/\hat{i}_p = D - E$ for the second loop of arcing,

$i_d/\hat{i}_p = D - F + G$ for the third loop of arcing,

where C , D , E , F and G are defined as follows:

a) for constant arc voltage:

$$C = \frac{M}{\cos \varphi} \left[1 - e^{-\frac{R}{L}(t-t_{cs})} \right]$$

$$D = \frac{M}{\cos \varphi} \left[1 - e^{-\frac{R}{L}(t'_0-t_{cs})} \right] e^{-\frac{R}{L}(t'-t'_0)}$$

$$E = \frac{M}{\cos \varphi} \left[1 - e^{-\frac{R}{L}(t-t'_0)} \right]$$

$$F = \frac{M}{\cos \varphi} \left[1 - e^{-\frac{R}{L}(t''_0-t'_0)} \right] e^{-\frac{R}{L}(t-t''_0)}$$

$$G = \frac{M}{\cos \varphi} \left[1 - e^{-\frac{R}{L}(t-t_0'')} \right]$$

where

$M = \frac{U_a}{\hat{u}}$ = the ratio between the arc voltage and the peak value of the power-frequency voltage

$$\cos \varphi = \frac{R}{\sqrt{R^2 + (\omega L)^2}}$$

t_{cs} = instant of contact separation

t_0', t_0'' = instants at the end of each current loop

b) for linearly rising arc voltage:

$$C = \frac{M}{\cos \varphi} \left[(t - t_{cs}) - \frac{L}{R} (1 - e^{-\frac{R}{L}(t-t_{cs})}) \right]$$

$$D = \frac{M}{\cos \varphi} \left[(t_0' - t_{cs}) - \frac{L}{R} (1 - e^{-\frac{R}{L}(t_0' - t_{cs})}) \right] e^{-\frac{R}{L}(t-t_0')}$$

$$E = \frac{M}{\cos \varphi} \left[(t - t_0') - \frac{L}{R} (1 - e^{-\frac{R}{L}(t-t_0')}) + (t_0' - t_{cs}) \times (1 - e^{-\frac{R}{L}(t-t_0')}) \right]$$

$$F = \frac{M}{\cos \varphi} \left[(t_0'' - t_0') - \frac{L}{R} (1 - e^{-\frac{R}{L}(t_0'' - t_0')}) + (t_0' - t_{cs}) \times (1 - e^{-\frac{R}{L}(t_0'' - t_0')}) \right] e^{-\frac{R}{L}(t-t_0'')}$$

$$G = \frac{M}{\cos \varphi} \left[(t - t_0'') - \frac{L}{R} (1 - e^{-\frac{R}{L}(t-t_0'')}) + (t_0'' - t_{cs}) \times (1 - e^{-\frac{R}{L}(t-t_0'')}) \right]$$

where

$$M = \frac{S \times T_a}{2 \hat{u}}$$

Relative reductions of current amplitudes and loop durations related to the last arcing loop for some typical cases are given in Figures A.8 to A.11.

For symmetrical current, values are given for constant arc voltage as a function of ratio $U_a/\hat{u}$ in Figure A.8 and for linearly rising arc voltage as a function of the ratio $S \times T_a/2\hat{u}$ in Figure A.9. For asymmetrical current the corresponding results are given in Figures A.10 and A.11.

For arcing times, three typical values, i.e. for 1, 2 and 2,5 loops, are introduced. In the case of asymmetrical current contact parting positions have been selected starting about 1,5 cycles after current initiation.

The modifying of arc voltage is much dependent on not only arc voltage but also arcing time and current asymmetry, therefore an exact evaluation for each case is necessary.

NOTE In order to be able to compare the curves relevant to either type of arcing, suitable values have been chosen for the arc voltages: the value at the last current zero for linearly rising arc voltage is twice the value U_a for the constant arc voltage.