



BSI Standards Publication

High-voltage switchgear and controlgear

Part 101: Synthetic testing

National foreword

This British Standard is the UK implementation of EN 62271-101:2013, including amendment A1:2018 and corrigendum January 2018. It is identical to IEC 62271-101:2012, including amendment 1:2017 and corrigendum January 2018. It supersedes BS EN 62271-101:2013, which is withdrawn.

The text of IEC amendment 1:2017 has been provided in its entirety at the beginning of this document. BSI's policy of providing consolidated content remains unchanged; however, in the interest of expediency, in this instance BSI have chosen to collate the relevant content at the beginning of this document.

The UK participation in its preparation was entrusted to Technical Committee PEL/17/1, High-voltage switchgear and controlgear.

A list of organizations represented on this committee can be obtained on request to its secretary.

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Amendments/corrigenda issued since publication

Date	Text affected
30 April 2018	Implementation of IEC amendment 1:2017 and corrigendum January 2018 with CENELEC endorsement A1:2018

English version

**High-voltage switchgear and controlgear -
Part 101: Synthetic testing
(IEC 62271-101:2012)**

Appareillage à haute tension -
Partie 101: Essais synthétiques
(CEI 62271-101:2012)

Hochspannungs-Schaltgeräte und -
Schaltanlagen -
Teil 101: Synthetische Prüfung
(IEC 62271-101:2012)

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Management Centre: Avenue Marnix 17, B - 1000 Brussels

Foreword

The text of document 17A/1015/FDIS, future edition 2 of IEC 62271-101, prepared by SC 17A, "High-voltage switchgear and controlgear", of IEC TC 17, "Switchgear and controlgear" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 62271-101:2013.

The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2013-08-16
- latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2015-11-16

This document supersedes EN 62271-101:2006 + A1:2010.

EN 62271-101:2013 includes the following significant technical changes with respect to EN 62271-101:2006:

- addition of the new rated voltages of 1 100 kV and 1 200 kV;
- revision of Annex F regarding circuit-breakers with opening resistors;
- alignment with the EN 62271-100:2009 + A1: 2012.

This publication shall be read in conjunction with EN 62271-100:2009, to which it refers. The numbering of the subclauses of Clause 6 is the same as in EN 62271-100. However, not all subclauses of EN 62271-100 are addressed; merely those where synthetic testing has introduced changes.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC [and/or CEN] shall not be held responsible for identifying any or all such patent rights.

Endorsement notice

The text of the International Standard IEC 62271-101:2012 was approved by CENELEC as a European Standard without any modification.

English Version

High-voltage switchgear and controlgear - Part 101: Synthetic
testing
(IEC 62271-101:2012/A1:2017 + COR1:2018)

Appareillage à haute tension - Partie 101: Essais
synthétiques
(IEC 62271-101:2012/A1:2017 + COR1:2018)

Hochspannungs-Schaltgeräte und -Schaltanlagen - Teil
101: Synthetische Prüfung
(IEC 62271-101:2012/A1:2017 + COR1:2018)

This amendment A1 modifies the European Standard EN 62271-101:2013; it was approved by CENELEC on 2018-01-04. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this amendment the status of a national standard without any alteration.

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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
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European foreword

The text of document 17A/1149/FDIS, future edition 1 of IEC 62271-101:2012/A1 prepared by IEC/SC 17A: “High-voltage switchgear and controlgear”, of IEC/TC 17: “Switchgear and controlgear” was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 62271-101:2013/A1:2018.

The following dates are fixed:

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implemented at national level by
publication of an identical national
standard or by endorsement
- latest date by which the national (dow) 2021-01-04
standards conflicting with the
document have to be withdrawn

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Endorsement notice

The text of the International Standard IEC 62271-101:2012/A1:2017+ COR1:2018 was approved by CENELEC as a European Standard without any modification.

Annex ZA (normative)

Normative references to international publications with their corresponding European publications

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 Where an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu.

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 62271-100	2008	High-voltage switchgear and controlgear -	EN 62271-100	2009
+ A1	2012	Part 100: Alternating current circuit-breakers	+ A1	2012
+ A2	2017		+ A2	2017

INTERNATIONAL STANDARD

NORME INTERNATIONALE



AMENDMENT 1 AMENDEMENT 1

High-voltage switchgear and controlgear – Part 101: Synthetic testing

Appareillage à haute tension – Partie 101: Essais synthétiques

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FOREWORD

This amendment has been prepared by subcommittee 17A: Switching devices, of IEC technical committee 17: High-voltage switchgear and controlgear.

The text of this amendment is based on the following documents:

FDIS	Report on voting
17A/1149/FDIS	17A/1154/RVD

Full information on the voting for the approval of this amendment can be found in the report on voting indicated in the above table.

The committee has decided that the contents of this amendment and the base publication will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

The contents of the corrigendum of January 2018 have been included in this copy.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

INTRODUCTION to the Amendment

This amendment includes the following significant technical changes:

- the test procedure for test-duty T100a has been aligned with IEC 62271-100;
 - Annexes A through D have been transferred to IEC 62271-306;
 - Annex I has been revised and now includes Annex P of IEC 62271-100;
 - Annexes K, L and N have been revised.
-

2 Normative references

Replace the existing reference to IEC 62271-100:2008 by the following new reference:

IEC 62271-100:2008, *High-voltage switchgear and controlgear – Part 100: Alternating current circuit-breakers*

3.17 **minimum clearing time**

Replace the entire term, definition, note and source as follows:

3.17 (void)

Add, after the definition 3.18, a new term and definition as follows:

3.19 **intermediate asymmetry**

level of asymmetry in the other two phases having a reduced (intermediate) level of asymmetry when in a three-phase system the short-circuit current is initiated simultaneously in all phases and maximum asymmetry is obtained in one of the phases

4.1.2 High-current interval

Replace the entire subclause by the following:

The tolerance on the amplitude and the power frequency of the prospective breaking current is given in 6.103.2 and 6.104.3 of IEC 62271-100:2008. Therefore, the following conditions concerning the actual current through the test circuit-breaker shall be met:

- for symmetrical testing the current amplitude and final loop duration shall not be less than 90 % of the required values based on the current of the test-duty considered;
- for SLF test-duties and T100s and T100a when tested with ITRV, the product of the current amplitude and the duration of the final loop shall not be less than 95 % of the required values based on the current of the test-duty considered;
- for asymmetrical testing, both the current amplitude and final loop duration shall be between 90 % and 110 % of the required values, based on the current of the test-duty considered and time constant (see Tables L.12 to L.17).

In rare cases, where the applied voltage from the high current source is of the same magnitude as the required test voltage in a direct test circuit, a higher deviation of the last current loop is accepted provided that the prospective current loop with the auxiliary circuit-breaker arcing is within the specified tolerances.

4.1.4 High-voltage interval

Replace the first sentence of the first hyphen by the following:

The initial value of the power-frequency recovery voltage, excluding the transient oscillations, shall not be less than the equivalent initial value of the power-frequency recovery voltage specified in 6.104.7 of IEC 62271-100:2008 which, for a test with symmetrical current, starts with a minimum peak value of $0,95 \times k_{pp} \times U_r \sqrt{(2/3)}$.

4.2.1 Current injection methods

Replace, in the first sentence, "(see Annex B)" by "(see IEC 62271-306)".

Add, after the second indent, the following new sentences:

Current injection method is mandatory for:

- short-line fault test duties;

- T100s and T100a when tested with ITRV.

The time during which the arc is fed only by the injected current shall be treated as part of the length of the final current loop.

Replace the paragraph below the second hyphen by the following:

If any device with breaking capability interrupts the current through the test circuit-breaker at the same time as the test circuit-breaker, the method is not a valid current injection method.

Replace, in item c), "(see Annex B)" by "(see IEC 62271-306)".

4.2.2 Voltage injection method

Replace, in the first sentence, "(see also Annex C)" by "(see IEC 62271-306)".

Delete the sentence below the third hyphen of the first list.

4.2.3 Duplicate circuit method (transformer or Skeats circuit)

Replace, in the first sentence, "(see also Annex D)" by "(see IEC 62271-306)".

Delete the penultimate paragraph.

Replace, in the last paragraph, "See Annex D" by "See IEC 62271-306".

4.2.4 Other synthetic test methods

Remove the last two paragraphs.

Table 3 – Test parameters during three-phase interruption for test-duties T10, T30, T60 and T100s, $k_{pp} = 1,3$

Replace "98" by "97" (3 instances).

5.2.2 Test circuit

Replace the second sentence of the first paragraph by the following:

Examples of circuits showing voltage and current wave shapes are given in Figures 5 and 6 for single-phase and Figure 7 for three-phase.

6 Specific requirements for synthetic tests for making and breaking performance related to the requirements of 6.102 through 6.111 of IEC 62271-100:2008

Replace the existing title by the following new title:

6 Type tests

Add, before the existing text of this clause, the following new title:

6.1 General

Replace the second paragraph by the following new paragraphs and new table:

Requirements concerning testing of metal enclosed and dead tank circuit-breakers are given in Annex N.

General requirements for circuit-breakers with opening resistors are given in Annex R of IEC 62271-100:2008/AMD1:2012. A method available for testing circuit-breakers having opening resistors is reported in Annex F.

The abbreviations given in Table 6 are used to specify the operations to be performed.

Table 6 – Abbreviations used for operation during synthetic tests

Cd	Closing operation in a direct circuit at the voltage of the current source which can be less than the voltage specified in 6.104.1 of IEC 62271-100:2008
(Cd)	Closing operation as Cd, which may be carried out under no-load conditions
Cd _{asy}	Closing operation against the rated short-circuit making current according to 6.104.2 of IEC 62271-100:2008/AMD2:2017 in a direct circuit at conditions described under Cd
Cs _{sym}	Closing operation against a symmetrical current equal to the rated short-circuit breaking current, carried out at the required applied voltage in a synthetic circuit
Od	Breaking operation at the voltage of the current source only and with the specified breaking current
Os	Breaking operation with specified parameters in a synthetic circuit
<i>t</i>	Time interval between operations (0,3 s or 3 min depending on the rated operating sequence)
<i>t'</i>	Time interval between operations (3 min)
<i>t''</i>	Time interval between operations (15 s)
SP	Single-phase test as defined in 6.108 of IEC 62271-100:2008/AMD2:2017
DEF	Double-earth fault test as defined in 6.108 of IEC 62271-100:2008/AMD2:2017
NOTE Due to the characteristics of synthetic testing it may be difficult to comply with the specified time intervals of the rated operating sequence. See 6.105.1 of IEC 62271-100:2008/AMD1:2008.	

In order to comply with all test requirements, it may be necessary to make more operations than specified in the normal test-duty. In such cases the circuit-breaker may be reconditioned and the test duty repeated.

6.102.10 Demonstration of arcing times

Replace the subclause by the following:

6.102.10 Demonstration of arcing times

6.102.10.1 General

The basic requirements to be met are given in 6.102.10 of IEC 62271-100:2008/AMD2:2017.

In order to be able to perform synthetic tests on the same basis as direct tests, normally it will be necessary to apply special re-ignition methods to prolong the arcing of the test circuit-breaker through the necessary number of zeros of the power-frequency current. See Annex H for re-ignition methods to prolong arcing.

The "step-by-step" method described in Annex H is the method used on most synthetic tests. The method is considered to be a sufficiently close approximation of the direct testing procedure.

The arcing is prolonged by means of thermal re-ignitions. As this method makes it possible to force the test circuit-breaker to re-ignite in all conditions, special care shall be taken not to re-ignite the circuit-breaker at the instant of a current zero when the circuit-breaker can clear. For this purpose it is necessary to determine, for each terminal fault, short-line fault and out-

of-phase test duty, the minimum arcing time of the circuit-breaker. At least two breaking tests, one clearance and one re-ignition, are necessary for this determination.

The clearance at the minimum arcing time is the first valid breaking operation. The other test is performed to demonstrate that a re-ignition at an early current zero would take place between the arcing contacts. This re-ignition test shall not be the last in a test duty.

For Od operations, a tolerance of ± 2 ms on the arcing time applies.

The extra tests necessary to demonstrate correct behaviour at early current zeros will usually contribute insignificantly to contact wear, etc., due to the short arcing times. Therefore, no re-conditioning should be necessary because of these tests.

The re-ignition(s) obtained when determining the minimum arcing time do(es) not indicate a failure of the circuit-breaker. However, it is important to establish that this re-ignition has taken place between the arcing contacts only. When using a current injection method, the interruption of the injected current a few loops after the re-ignition is often a useful means for the judgement. Thorough inspection of screens, arcing and main contacts, etc., should also be made to verify correct behaviour.

NOTE When performing Od-COs, or COd-COs operations the first opening operation is performed in a direct test circuit. This first opening operation should represent the minimum arcing time found for single opening operations. In case the arcing time of this first opening operation is longer than required, the test is considered as more severe.

The minimum clearing time for test-duty T100a is validated by the minimum arcing time of an interruption after a major loop with intermediate asymmetry.

6.102.10.2 Three-phase tests

Depending on the test circuit used, the test procedures given here may not cover the conditions of the 3rd pole-to-clear for solidly earthed systems ($k_{pp} = 1,3$). For this case the same procedures may be applied, with the manufacturer's consent, by combining the TRV and di/dt parameters for the 2nd pole-to-clear and the arcing time corresponding to the 3rd pole-to-clear. Alternatively, an additional test may be performed with the TRV, di/dt and the maximum arcing time corresponding to the 3rd pole-to-clear.

For alternative testing procedures of multi-enclosure type circuit-breakers with operating mechanism characteristics that require three-phase current, see Annex K.

6.102.10.2.1 Test duties T10, T30, T60, T100s, T100s(b)

The test procedure is as follows:

For convenience of testing, the pole in phase A is kept as the first-pole-to-clear.

First the minimum arcing time and correct re-ignition behaviour are established. This is done by changing the setting of the tripping impulse in steps of 18° (possibly this has to be repeated several times). After having done so, the setting of the control of the tripping impulse has to be advanced by approximately 40° , starting from the shortest arcing time at which the circuit-breaker cleared. For the last test, the setting of the control of the tripping impulse has to be advanced by approximately 20° , starting from the shortest arcing time at which the circuit-breaker cleared:

- first valid breaking operation: $t_{arc \min}$, minimum arcing time in phase A;
- re-ignition test: $t_{arc \text{ reig}} = t_{arc \min} - 18^\circ$, re-ignition in phase A;
- second valid breaking operation: $t_{arc \max} = t_{arc \min} + 40^\circ$, longest arcing time in phase A;
- third valid breaking operation: $t_{arc \text{ med}} = t_{arc \min} + 20^\circ$, medium arcing time in phase A.

The first valid breaking operation and re-ignition test consist of single opening operations. The second and third valid breaking operations are carried out as part of the rated operating sequence. If the rated operating sequence is CO-15s-CO, the third valid breaking operation is not required (see 6.102.10 of IEC 62271-100:2008/AMD2:2017).

For comparison with the arcing time settings used in three-phase direct tests, see Figure 8.

6.102.10.2.2 Test duty T100a

The intention is to demonstrate in a series of breaking tests the requirement a) and b) as defined in clause 6.102.10.2.2 of IEC 62271-100:2008/AMD2:2017:

- condition a) where arc extinction occurs in the first-pole-to-clear at the end of a major loop in the first phase with the required asymmetry criteria and with the longest possible arcing time t_{arc1} ;
- condition b) where arc extinction occurs at the end of an extended major loop in the last-pole-to-clear or in the second-pole-to-clear with the required asymmetry criteria and with the longest possible arcing time, t_{arc2} and t_{arc3} as follows:
 - the longest possible arcing time t_{arc2} applies for the last-pole-to-clear for circuit-breakers rated for $k_{pp} = 1,5$;
 - the longest possible arcing time t_{arc3} applies for the second-pole-to-clear for circuit-breakers rated for $k_{pp} = 1,3$ or $1,2$.

The test procedure, for three-phase testing, is as follows:

In order to simplify the test procedure, the pole in phase A is kept as the first-pole-to-clear. As a consequence the pole in phase C will be subjected to increased electrical wear. In order to obtain similar electrical wear on the poles of phase B and C, the test can be performed by exchanging the poles of phases B and C for the second breaking operation.

First the minimum arcing time $t_{arc\ min}$ (Figures 9 and 10, first test) and re-ignition behaviour (Figures 9 and 10, second test) shall be demonstrated having intermediate asymmetry in phase A (Tables L.12 to L.17, columns 7, 8 and 9) and with the major extended loop occurring in phase C. This is done by changing the setting of the tripping impulse in steps of $d\alpha = 18^\circ$ (possibly this has to be repeated several times).

Before the next operation, initiation of short-circuit current shall be advanced by 60° where the required asymmetry changes to phase A (Figures 9 and 10 third test). Arc extinction shall occur in phase A, the first-pole-to-clear at the end of a major loop with the required asymmetry criteria and with the maximum arcing time demonstrating condition a) mentioned above.

The maximum arcing time t_{arc1} for the first pole-to-clear is achieved when the following condition is met:

$$t_{arc1} = t_{arc\ min} + \Delta t_{a1} - T \times d\alpha/360^\circ$$

In the next operation, the initiation of short-circuit current shall be delayed by 60° . As a result the required asymmetry changes to phase C. Arc extinction shall occur in phase C at the end of a major extended loop with the required asymmetry criteria and with the maximum arcing time demonstrating condition b) mentioned above:

- the maximum arcing time t_{arc2} for the last-pole-to-clear for circuit-breakers intended to be used in non-effectively earthed neutral systems (Figure 9 fourth test) is achieved when the following condition is met:

$$t_{arc2} = t_{arc\ min} + \Delta t_{a2} - T \times d\alpha/360^\circ$$

- the maximum arcing time $t_{\text{arc}3}$ for the second-pole-to-clear for circuit-breakers intended to be used in effectively earthed neutral systems (Figure 10 fourth test) is achieved when the following condition is met:

$$t_{\text{arc}3} = t_{\text{arc min}} + \Delta t_{\text{a}3} - T \times \alpha/360^\circ$$

where $\Delta t_{\text{a}1}$, $\Delta t_{\text{a}2}$, $\Delta t_{\text{a}3}$ are the relevant time parameters to be selected from Tables L.12 to L.17.

The order of the last two breaking operations can be interchanged.

Some circuit-breakers will not clear at the end of a major loop after the required arcing time. However, this test is valid if the circuit-breaker clears the subsequent minor loop, that becomes the last-pole-to-clear. The corresponding parameters for the last-pole-to-clear shall be applied.

For comparison with the arcing settings used in three-phase direct tests, see Figures 9 and 10.

6.102.10.3 Single-phase tests in substitution for three-phase conditions, out-of-phase and short-line fault tests

6.102.10.3.1 General

The procedures as described in 6.102.10.3 of IEC 62271-100:2008/AMD2:2017 are applicable with the following changes. These procedures are meant to demonstrate the first-pole-to-clear, the second-pole-to-clear and the third-pole-to-clear conditions, with current and voltage parameters applicable for the first-pole-to-clear.

6.102.10.3.3 Test-duty T100a

The test procedure is as follows.

The minimum arcing time $t_{\text{arc min}}$ and re-ignition behaviour shall be demonstrated with the major loop at intermediate asymmetry (Tables L.12 to L.17, columns 8 and 9). This is done by changing the setting of the tripping impulse in steps of 18° (possibly this has to be repeated several times).

After that, two breaking operations at required asymmetry shall be performed as described below. Tables L.12 to L.17, columns 3 and 4, give the required values of the peak short-circuit current and loop duration that shall be attained in the last loop prior to the interruption.

One breaking operation, corresponding to condition a) of 6.102.10.2.2 of IEC 62271-100:2008/AMD2:2017, shall demonstrate interruption at the end of the major loop with an arcing time equivalent to the maximum arcing time under three-phase conditions $t_{\text{arc}1}$ of the first-pole-to-clear.

The maximum arcing time $t_{\text{arc}1}$ for the first pole-to-clear is achieved when the following condition is met:

$$t_{\text{arc}1} = t_{\text{arc min}} + \Delta t_{\text{a}1} - T \times \alpha/360^\circ$$

Another breaking operation, corresponding to condition b) of 6.102.10.2.2 of IEC 62271-100:2008/AMD2:2017, shall demonstrate interruption at the end of the major loop with an arcing time equivalent to the maximum arcing time under three-phase conditions:

- the maximum arcing time $t_{\text{arc}2}$ for the last-pole-to-clear for circuit-breakers intended to be used in non-effectively earthed neutral systems ($k_{\text{pp}} = 1,5$) is achieved when the following condition is met:

$$t_{\text{arc}2} = t_{\text{arc min}} + \Delta t_{a2} - T \times d\alpha/360^\circ$$

- the maximum arcing time $t_{\text{arc}3}$ for the second-pole-to-clear for circuit-breakers intended to be used in effectively earthed neutral systems ($k_{\text{pp}} = 1,3$ or $k_{\text{pp}} = 1,2$) is achieved when the following condition is met:

$$t_{\text{arc}3} = t_{\text{arc min}} + \Delta t_{a3} - T \times d\alpha/360^\circ$$

where Δt_{a1} , Δt_{a2} , Δt_{a3} are the relevant time parameters to be selected from Tables L.12 to L.17.

The order of the last two breaking operations may be interchanged.

Since some circuit-breakers will not clear after a major loop, a test is still valid if the circuit-breaker interrupts at the subsequent minor loop.

6.102.10.3.5 Splitting of test-duties in test series, taking into account the associated TRV for each pole-to-clear

The procedures as described in 6.102.10.3.5 of IEC 62271-100:2008/AMD2:2017 are applicable and the test procedure for synthetic testing is given in Annex L.

6.102.10.3.101 Modified procedure in cases where the circuit-breaker did not interrupt during a test with a medium arcing time, during breaking tests with symmetrical current

If the circuit-breaker did not interrupt at the expected current zero during a breaking operation with symmetrical current with a medium arcing time then it is necessary to perform an additional breaking operation.

The breaking operation shall demonstrate interruption with the "ultimate maximum arcing time" $t_{\text{arc ult max}}$ which is:

$$t_{\text{arc ult max}} = t_{\text{arc med}} + T \times (150 / 360), \text{ if } k_{\text{pp}} = 1,5$$

$$t_{\text{arc ult max}} = t_{\text{arc med}} + T \times (180 / 360), \text{ if } k_{\text{pp}} = 1,3, 1,2 \text{ or } 1,0$$

where

$t_{\text{arc med}}$ is the medium arcing time at which the circuit-breaker did not interrupt;

$t_{\text{arc ult max}}$ is the ultimate maximum arcing time.

If the circuit-breaker does not interrupt during this additional breaking operation, it is permissible to carry out maintenance work on the circuit-breaker according to 6.102.9.5 of IEC 62271-100:2008/AMD2:2017 and repeat the test-duty where the breaking operation with the medium arcing time is replaced by the breaking operation with the ultimate maximum arcing time.

For test duties T10, T30, T60, L₉₀, L₇₅ and L₆₀, the $t_{\text{arc ult max}}$ is demonstrated with (Cd)Os.

For test duty T100s, the $t_{\text{arc ult max}}$ is demonstrated with CdOs.

For OP1 and OP2 test duties, the $t_{\text{arc ult max}}$ is demonstrated with Os.

6.106 Basic short-circuit test-duties

Delete the second paragraph and the list of abbreviations.

6.106.5 Test-duty T100a

Replace the second paragraph of item a) by the following:

Required values of the peak short-circuit current and loop duration shall be in accordance with the values in Tables L.12 to L.17.

Delete the fourth paragraph from item a) starting with "The required asymmetry level".

Replace the third paragraph of item b) by the following:

The corresponding corrected values can be found in Tables L.12 to L.17.

Replace the last sentence of 1) of item c) by the following:

See Annex I for more guidance.

Replace the last paragraph of 2) of item c) by the following:

Different test circuits for different asymmetry conditions may be needed in order to obtain the required values. A test with one single test circuit may over-stress the circuit-breaker and requires the consent of the manufacturer.

Add the following paragraph to item c):

- 3) u_c and RRRV for second-pole-to-clear and last-pole-to-clear are obtained from the respective values for symmetrical conditions reduced by the same factor as the corresponding di/dt .

Add, at the end of the list, the following new item e):

e) Intermediate asymmetry

The phase with the intermediate asymmetry as required for testing T100a according to 6.102.10.2.2 and 6.102.10.3.3 refers to the phase, in a three-phase system, having its current zero just prior to current zero of the phase with required asymmetry. This phase also starts with a major loop of current, at current initiation. As an example the red coloured phase in tests 1 and 2 of Figures 9 and 10 (synthetic test, right hand part of the figures) fulfils this intermediate asymmetry condition.

In this particular phase, the major loops are called intermediate major loops.

The parameters of the intermediate major loop can be obtained from Tables L.12 to L.17.

6.109 Short-line fault (SLF) tests

Replace the third paragraph by the following:

The final current loop before clearing shall have an amplitude equal to the test current times $\sqrt{2}$ with a tolerance of $\pm 10\%$ including the provisions of 4.1.2.

6.111.2 General

Delete the existing title and text.

6.111.3 Characteristics of supply circuits

Replace the second paragraph by the following:

The effects of current chopping, as described in G.7, may modify the recovery voltage during the capacitive current switching tests.

Add, after the second paragraph, the following new paragraph:

A test circuit with a 50 Hz current circuit may be used to prove the capacitive current switching capability for a rating of 60 Hz, provided that the recovery voltage fulfils the 60 Hz requirements (see 6.111.3 of IEC 62271-100:2008/AMD2:2017). The setting of the contact separation should be based on the frequency of the current source.

6.111.7 Test voltage

Replace the existing text by the following:

The prospective recovery voltage during synthetic capacitive current switching tests shall be calculated based on the test voltage of the corresponding single-phase direct test, as defined in 6.111.7 of IEC 62271-100:2008/AMD2:2017, and comply with the requirements of 6.111.10 of IEC 62271-100:2008/AMD2:2017.

Due to limitations of some synthetic test circuits the following additional requirements apply to the recovery voltage:

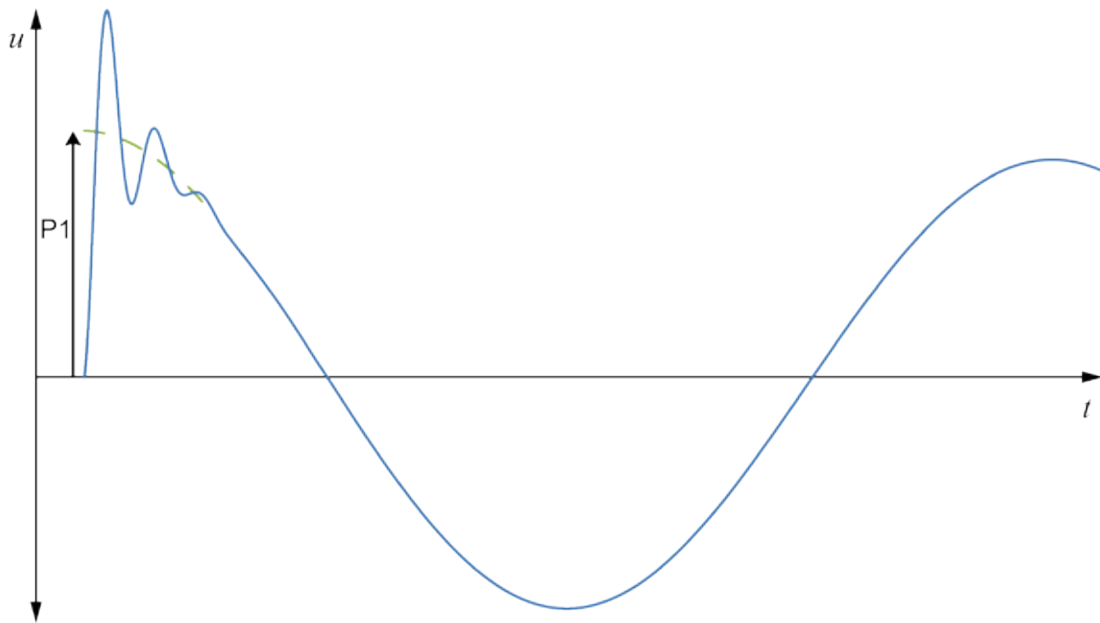
- The peak value of the a.c. component of the recovery voltage should be kept as close as possible to $k_C \times U_r \sqrt{2/\sqrt{3}}$;
- The d.c. component of the recovery voltage shall not decay more than 10 % within an interval of 0,3 s after final arc extinction, except for test duty LC1 and/or CC1;
- The recovery voltage shall not fall below $1,5 \times k_C \times U_r \sqrt{2/\sqrt{3}}$ within an interval of 0,1 s after final arc extinction.

Graphical representation is shown in Figure 8.

Examples of synthetic capacitive current switching circuits are given in Annex G.

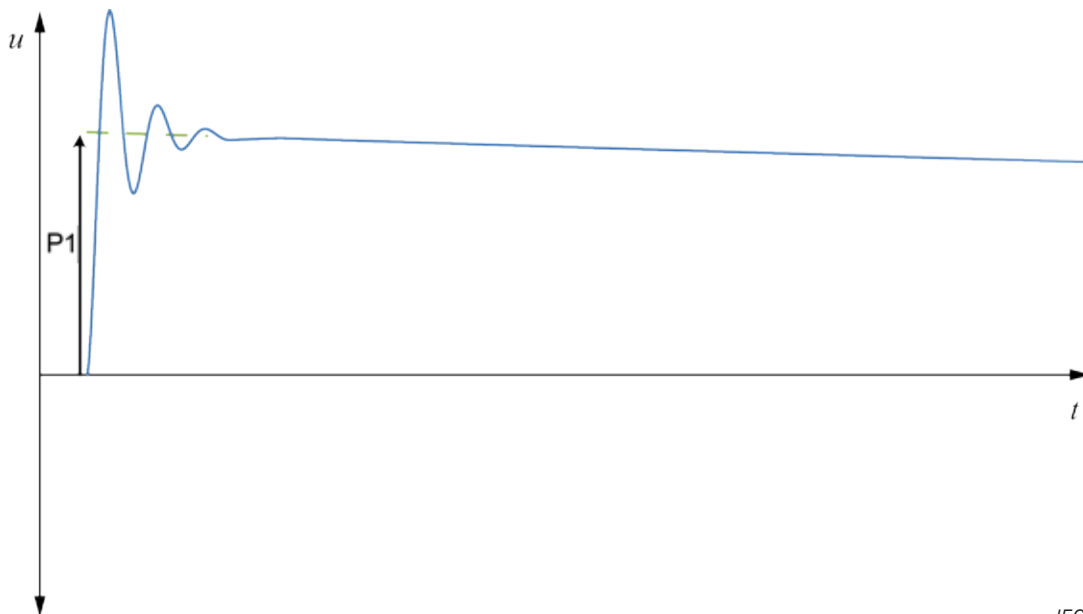
Figure 2 – Examples of evaluation of recovery voltage

Replace Figure 2 by the following:



IEC

a) Example of a power-frequency recovery voltage



IEC

b) Example of a d.c. steady-state recovery voltage

P1 Point of initial value of (power frequency or d.c. steady-state) recovery voltage,

$$\geq 0,95 \times k_{pp} \times U_r \times \sqrt{\frac{2}{3}}$$

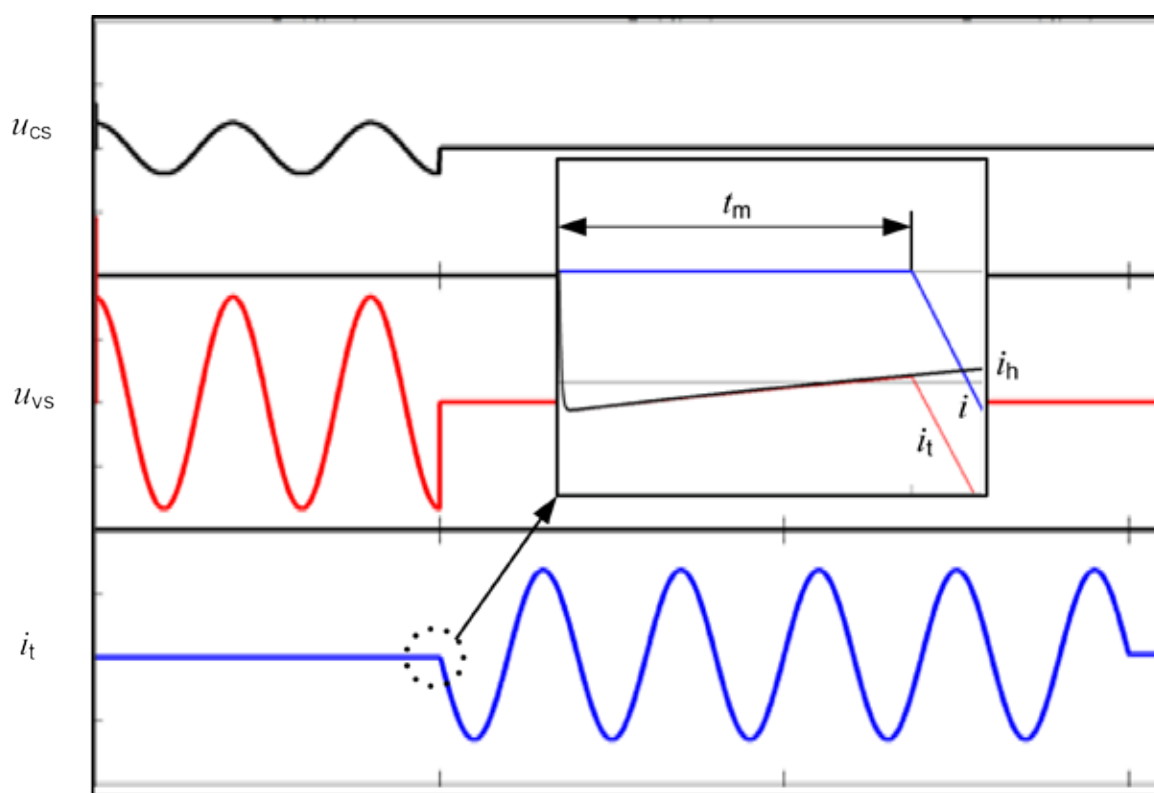
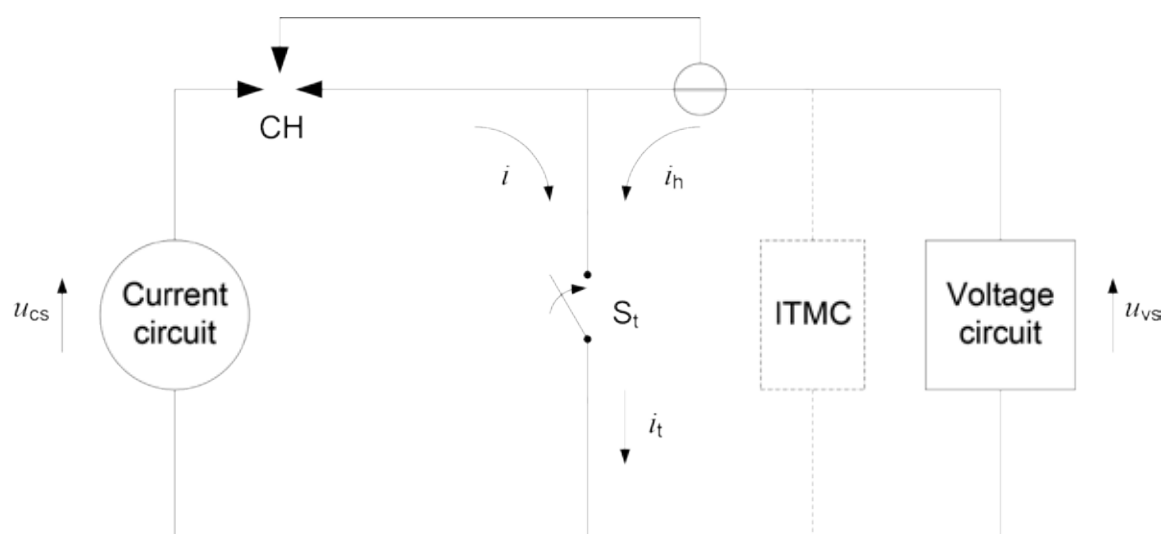
Blue line Tested recovery voltage

Green dotted line Tested power frequency or d.c. steady-state recovery voltage

Figure 2 – Examples of evaluation of initial recovery voltage

Figure 5 – Typical synthetic making circuit for single-phase tests

Replace Figure 5 by the following:



IEC

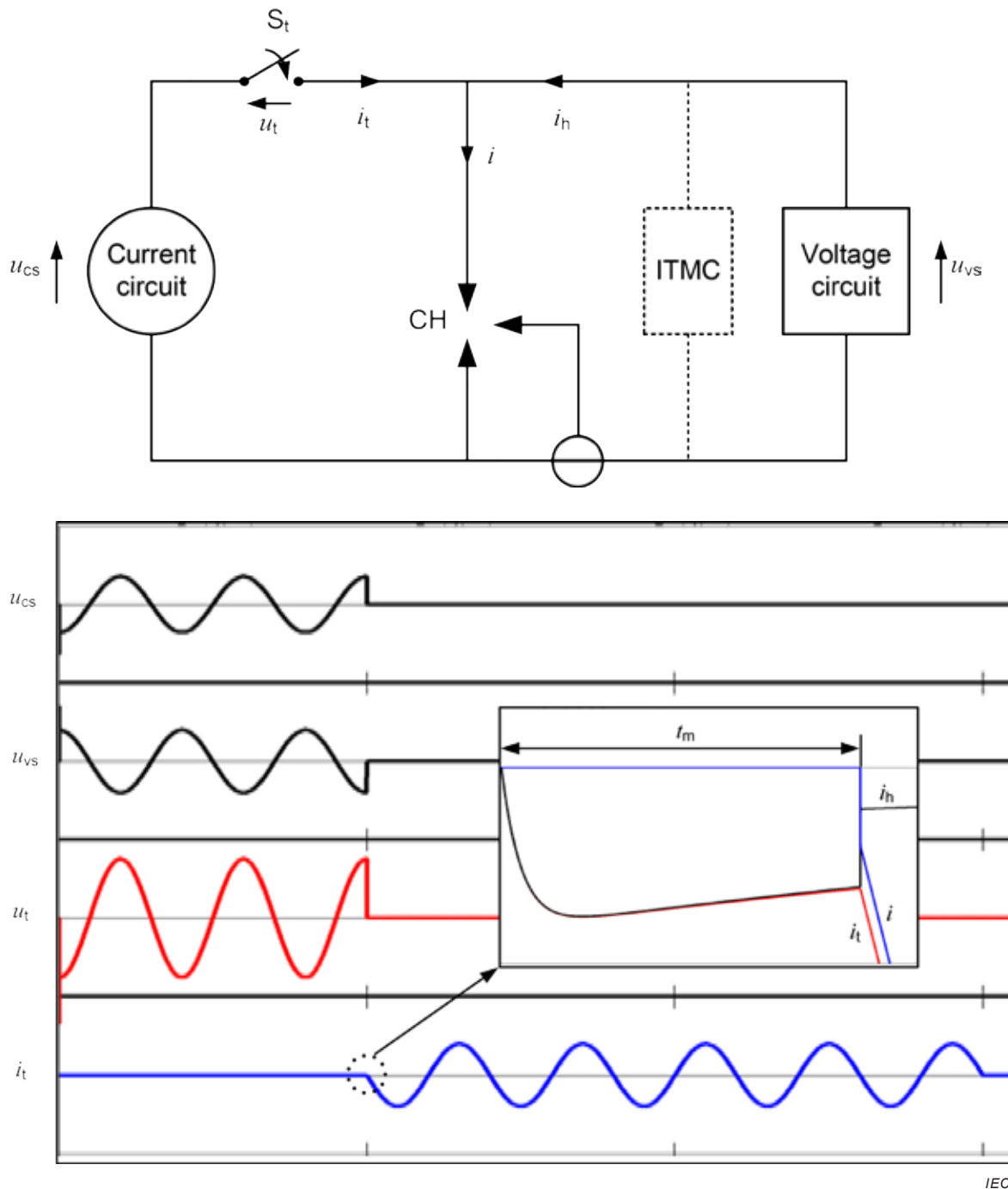
Key

u_{cs}	voltage of current circuit	u_{vs}	voltage of voltage circuit
CH	making device (triggered spark gap)	i_h	initial transient making current (ITMC)
i	power-frequency current supplied by current circuit	i_t	current in the test circuit-breaker
S_t	test circuit-breaker	t_m	time delay of making device

Figure 5 – Example of synthetic making circuit for single-phase tests

Figure 6 – Typical synthetic making circuit for out-of-phase

Replace Figure 6 by the following:



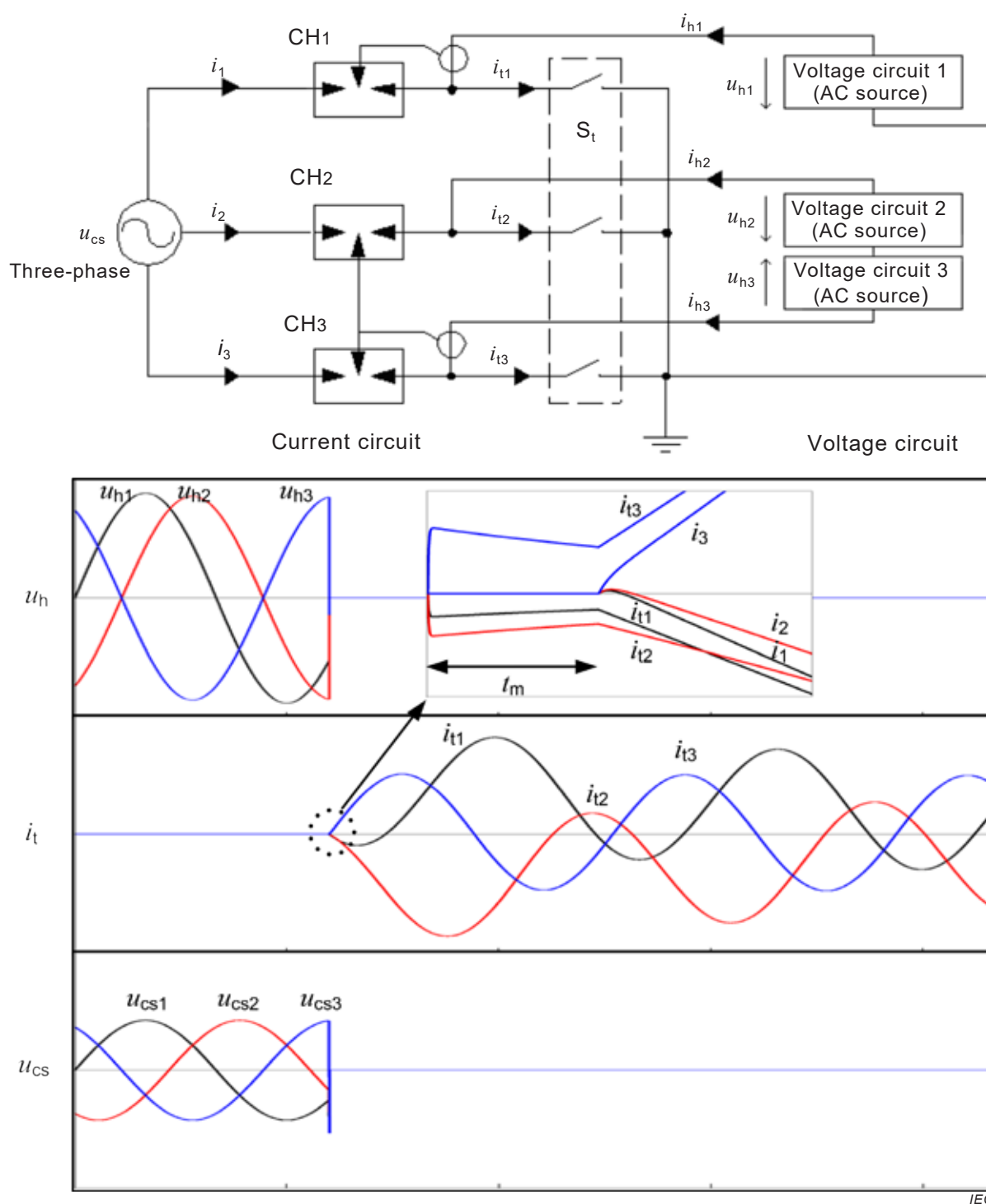
Key

u_{cs}	voltage of current circuit	u_{vs}	voltage of voltage circuit
CH	making device (triggered spark gap)	i_h	initial transient making current (ITMC)
i	power-frequency current supplied by current circuit	i_t	current in the test circuit-breaker
S_t	test circuit-breaker	u_t	test voltage across test circuit-breaker
t_m	time delay of making device		

Figure 6 – Example of synthetic making circuit for out-of-phase

Figure 7 – Typical synthetic make circuit for three-phase tests ($k_{pp} = 1,5$)

Replace Figure 7 by the following:



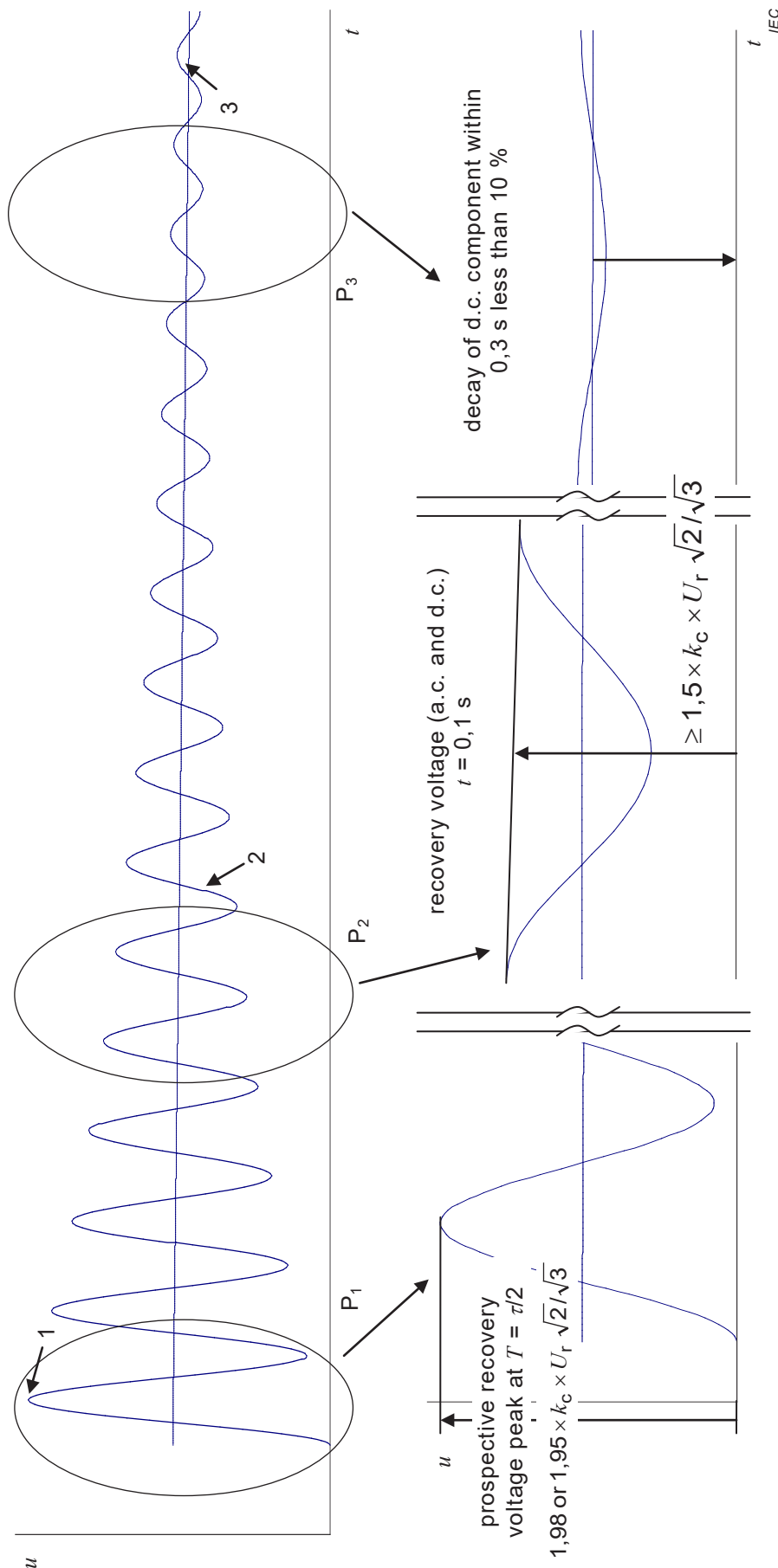
Key

$u_{cs1}, u_{cs2}, u_{cs3}$	voltage of current circuit	u_{h1}, u_{h2}, u_{h3}	applied voltage
i_1, i_2, i_3	current supplied by the current circuit	CH ₁ , CH ₂ , CH ₃	making device (triggered spark gap)
i_{t1}, i_{t2}, i_{t3}	current through the test object	S_t	test circuit-breaker
i_{h1}, i_{h2}, i_{h3}	initial transient making current (ITMC)	t_m	time delay of making device

Figure 7 – Example of synthetic making circuit for three-phase tests (k_{pp}

Figure 8 – Comparison of arcing time settings during three-phase direct tests (left) and three-phase synthetic (right) for T100s with $k_{pp} = 1,5$

Replace Figure 8 by the following:

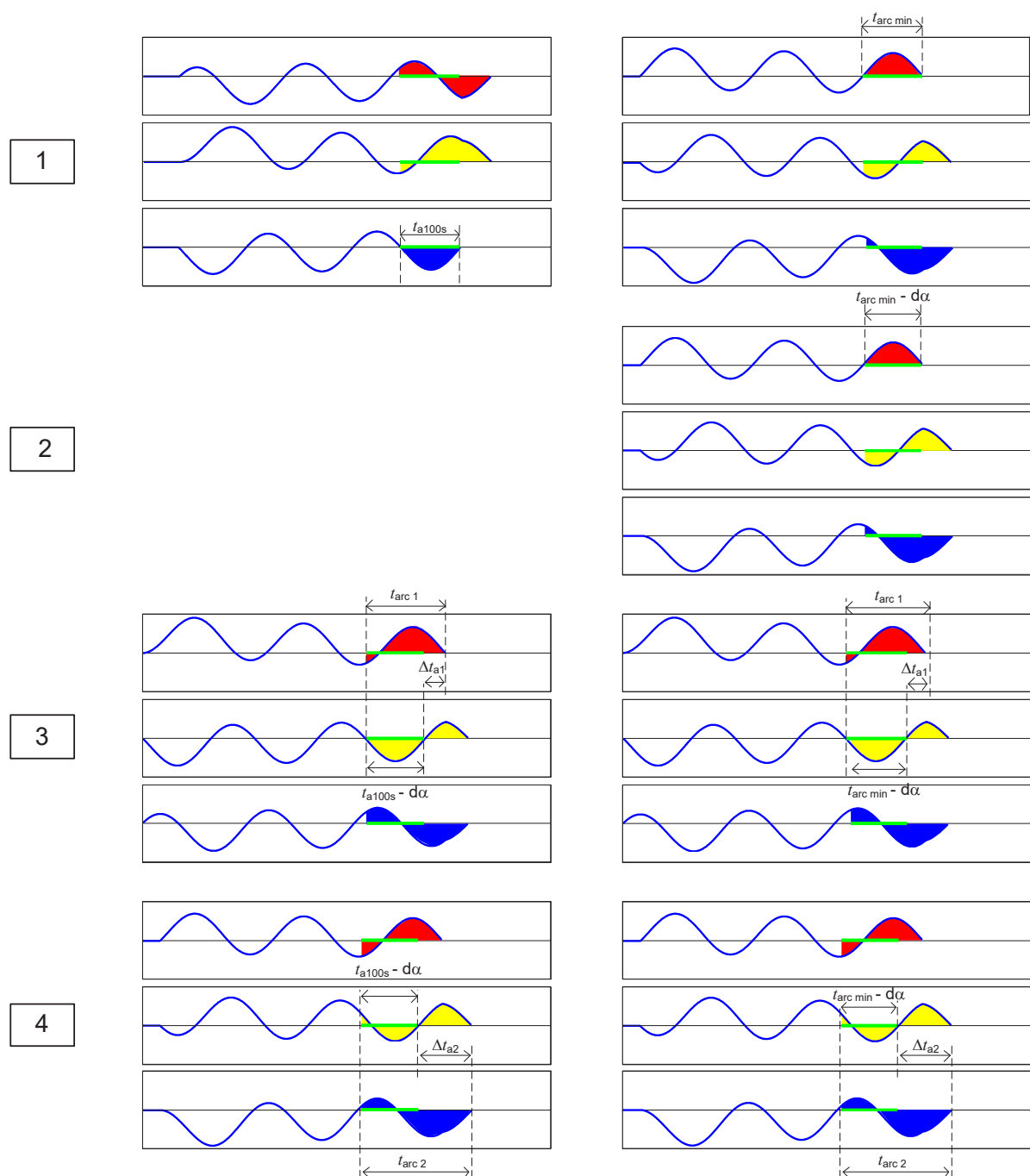


recovery voltage with exponential decrement in the a.c. and d.c. components across the circuit-breaker during a synthetic capacitive current switching test	P_1	point on which the peak of recovery voltage (1) occurs
a.c. component of the recovery voltage	P_2	point where the recovery voltage (1) shall not be below $1,5 \times k_c \times U_r \sqrt{2/\sqrt{3}}$
d.c. component of the recovery voltage cycle of power frequency	P_3	point where the d.c. recovery voltage (3) shall not be below $0,9 \times k_c \times U_r \sqrt{2/\sqrt{3}}$

Figure 8 – Evaluation of recovery voltage during synthetic capacitive current switching testing

Figure 9 – Comparison of arcing time settings during three-phase direct tests (left) and three-phase synthetic (right) for T100a with $k_{pp} = 1,5$

Replace Figure 9 by the following:



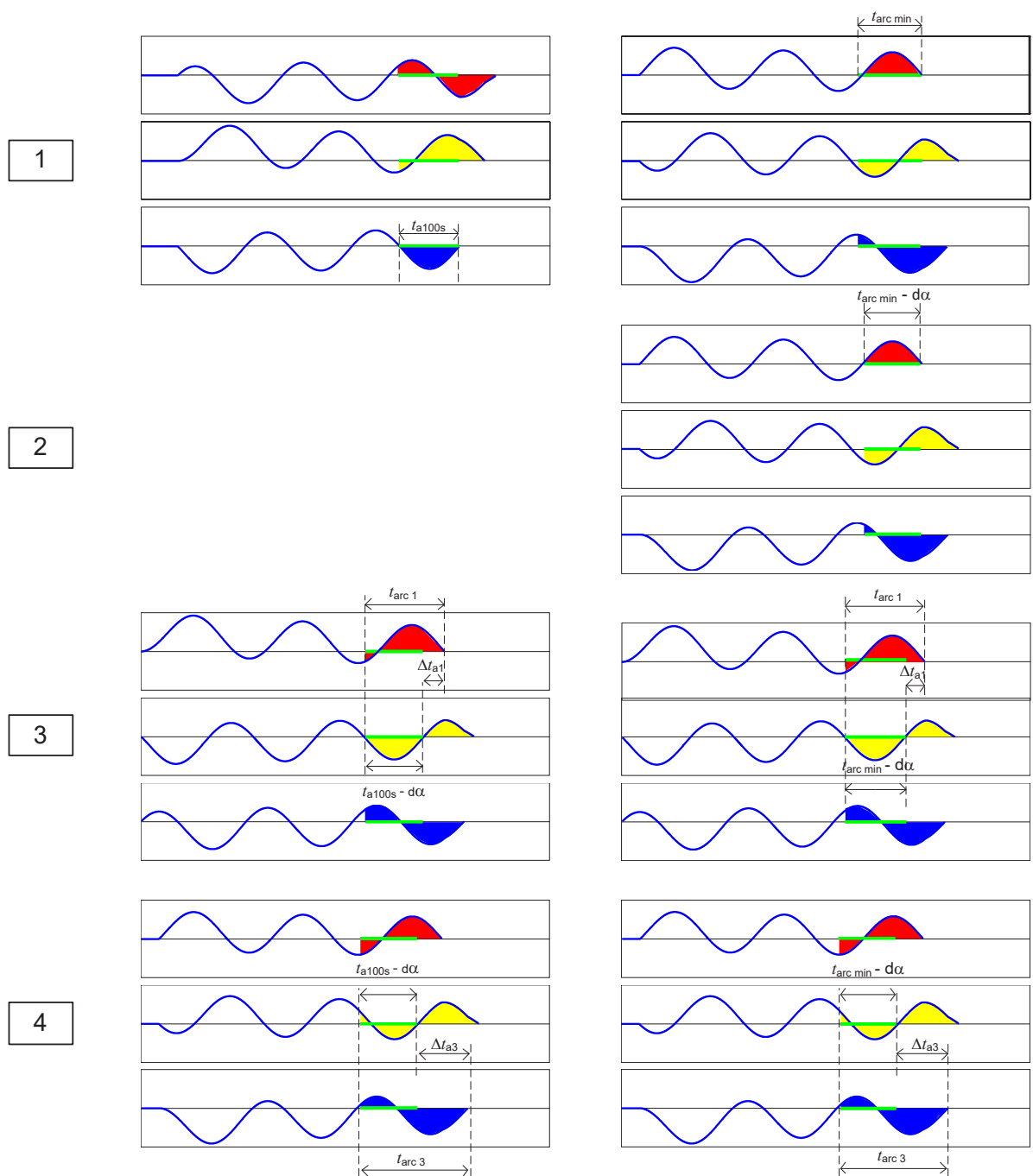
IEC

Key

- 1 First test, $t_{arc\ min}$
- 2 Second test, $t_{arc\ min} - d\alpha$, resulting in re-ignition
- 3 Condition a) first-pole-to-clear after major loop
- 4 Condition b) last-pole-to-clear after major extended loop

Figure 9 – Comparison of arcing time settings during three-phase direct tests (left) and three-phase synthetic tests (right) for T100a with $k_{pp} = 1,5$

Add, after the new Figure 9 added by this amendment, the following new Figure 10:



IEC

Key

- 1 First test, $t_{arc \min}$
- 2 Second test, $t_{arc \min} - d\alpha$, resulting in re-ignition
- 3 Condition a) first-pole-to-clear after major loop
- 4 Condition b) second-pole-to-clear after major extended loop

Figure 10 – Comparison of arcing time settings during three-phase direct tests (left) and three-phase synthetic tests (right) for T100a with $k_{pp} = 1,3$

E.1 General

Replace "Annex C of IEC 62271-100:2008" by "IEC 62271-306".

E.3 Test conditions

Replace item a) by the following:

- a) Circuit parameters of the circuits.

E.4.2 Voltages

Add, after item b), the following item:

- c) Voltage to enclosure for the test circuit-breaker when applicable.

E.4.3 Currents

Delete the paragraph below item b).

Annex G (informative) Synthetic methods for capacitive-current switching

Replace the entire text of this annex, including figures, by the following:

G.1 General

Synthetic capacitive current switching tests are generally performed using single-phase test circuits. There are principally two types of circuits:

- a) Combined current and voltage circuits

The test circuit consists of a current circuit and a voltage circuit. Both circuits have a capacitive nature, although an inductive or resistive current circuit can be used as an alternative, provided that the phase angle between the two sources is changed accordingly.

The two sources can be power frequency fed transformers or charged capacitors, or a combination of both. The application of this type of circuit implies the use of an auxiliary circuit-breaker to isolate the test circuit-breaker from the current circuit.

The time between separation of voltage circuit and current circuit by the auxiliary circuit-breaker (current zero in the current circuit) and the current zero in the voltage circuit should not be longer than 500 μ s.

- b) LC oscillating circuits

The test circuit consists of an LC oscillating circuit that provides both the current and voltage from a single source. The application of this type of circuit does not require the use of an auxiliary circuit-breaker.

For applicability of the mentioned methods in case of metal-enclosed or dead tank circuit-breakers, see Annex N of this document and Annex O of IEC 62271-100:2008/AMD2:2017.

NOTE Phenomena occurring after a restrike or a re-ignition event are not representative of service conditions as the test circuit does not adequately reproduce the post-event voltage conditions.

Many test circuits are possible with different features. Some examples are given in Figures G.1 to G.7.

An impedance may be added for protection of the test circuit and/or control of the inrush current, provided that the prospective recovery voltage is in accordance with 6.111.10 of IEC 62271-100:2008/AMD2:2017.

G.2 Recovery voltage

In principle, the recovery voltage consists of an a.c. voltage applied to one terminal of the test circuit-breaker, while a slowly decaying d.c. voltage stresses the other terminal. In some test circuits both voltages are superimposed at one terminal of the test circuit-breaker, the other terminal being earthed. This condition is more severe with respect to both the insulation to earth and across contacts. The combined current and voltage circuits of Figures G.4 and G.5 can be used to apply the correct voltage stresses to each terminal of the circuit-breaker. For synthetic method the decay of the AC voltage should be kept within limits given in 6.111.7 and Figure 8.

G.3 Combined current and voltage circuits

When tests are performed using the circuits described in item a) of G.1, the connection of the current and voltage circuits to the auxiliary and test circuit-breakers can be in parallel mode, subtracting the voltages on the auxiliary circuit-breaker, or in series mode, and adding the voltages on the test circuit-breaker.

Depending on whether the voltage circuit is connected permanently or switched in before or after power-frequency current zero, a distinction can be made between power-frequency current superposition, current injection and voltage injection circuits.

G.4 Making tests

An example of a test circuit is given in Figure G.7.

The voltage circuit supplies the test voltage during closing of the contacts until dielectric breakdown occurs causing the initial transient making current to flow.

G.5 Current chopping

Current chopping phenomena, caused by interaction between a circuit-breaker and its circuit (in service or during laboratory tests), generally leads to a reduction of the load side voltage and thus also of the dielectric stress applied to the circuit-breaker.

In service or during laboratory tests in direct test circuits, chopping of small capacitive currents may take place. In synthetic test circuits the probability of these events occurring is increased for the following reasons:

- generally speaking the characteristic parameters of the main and stray components of some synthetic test circuits are different and may influence the chopping behaviour of the circuit-breaker;
- the effect of additional (auxiliary) circuit-breakers in series with the test circuit-breaker in combined current and voltage circuits;
- the increased ratio of arc voltage to power-frequency voltage.

Therefore, when performing synthetic tests using test circuits described in item a) of G.1, it may be difficult to determine whether or not current chopping is a significant feature of the test circuit-breaker. To reduce current chopping, the following measures can be taken:

- modify the capacitances seen from the circuit-breaker terminals;

- use an auxiliary circuit-breaker with a short minimum arc duration and low arc voltage in combined current and voltage circuits.

Some synthetic test circuits are less-sensitive to current chopping, and therefore, may provide a recovery voltage for long arcing times where it would be reduced in a direct circuit.

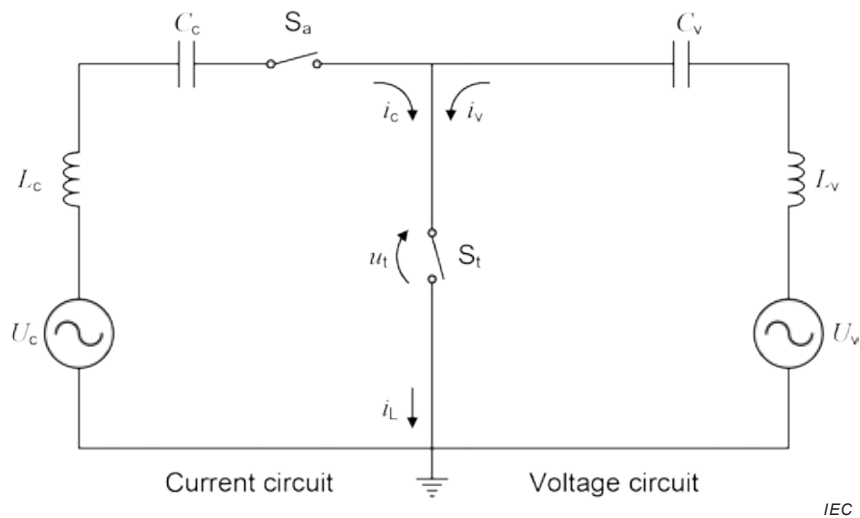
G.6 Examples test circuits

Figures G.1 to G.7 show some examples of synthetic test circuits for capacitive current switching. The following list of symbol explanations relates to these figures, as appropriate, and are listed here for the sake of brevity and to avoid repetition.

The equations presented for the given circuits are meant for guidance only. They do not take into account losses or other phenomena in the test circuits.

C_c	= capacitance of the current circuit
C_{hB}, C_B	= capacitances of the voltage circuit B
C_v	= capacitance of the voltage circuit
C_h, L_{pf}	= power frequency oscillation circuit
f_{inrush}	= frequency of the inrush current
f_L	= frequency of the current i_L
f_r	= rated power frequency
f_{RV}	= frequency of the recovery voltage
G	= gap
i_c	= current of the current circuit
$i_{max\ peak}$	= maximum peak of the inrush current
i_L	= load current (current through test circuit-breaker S_t)
i_v	= current of the voltage circuit
L_c	= inductance of the current circuit
L_v	= inductance of the voltage circuit
m	= ratio of current i_L to current i_v
n	= ratio of voltage u_t to voltage U_c
R_v	= resistance of the voltage circuit
R_B	= resistance of circuit B
R_p	= earthing resistor
S_a	= auxiliary circuit-breaker
S_{a1}, S_{a2}, S_{a3}	= auxiliary circuit-breakers
S_t	= test circuit-breaker
$\hat{t}$	= time to the peak of injected current
U_c	= voltage of the current circuit
U_h	= charging voltage of C_h
U_{hB}	= charging voltage of C_{hB}
U_v	= voltage of the voltage circuit
u_A, u_B	= voltage to earth at points A and B, respectively
u_t	= voltage across the test circuit-breaker S_t

U_t = test voltage according to IEC 62271-100
 ω = pulsation of the test circuit, $\omega = 2 \times \pi \times f_r$



$$U_c = u_t/n$$

$$i_c = i_L(1 - 1/m)$$

$$\omega L_c \ll 1/\omega C_c$$

$$C_c = n(1 - 1/m)C_L$$

C_L = equivalent load capacitance

$$U_v = u_t$$

$$i_v = i_L/m$$

$$\omega L_v \ll 1/\omega C_v$$

$$C_v = C_L/m$$

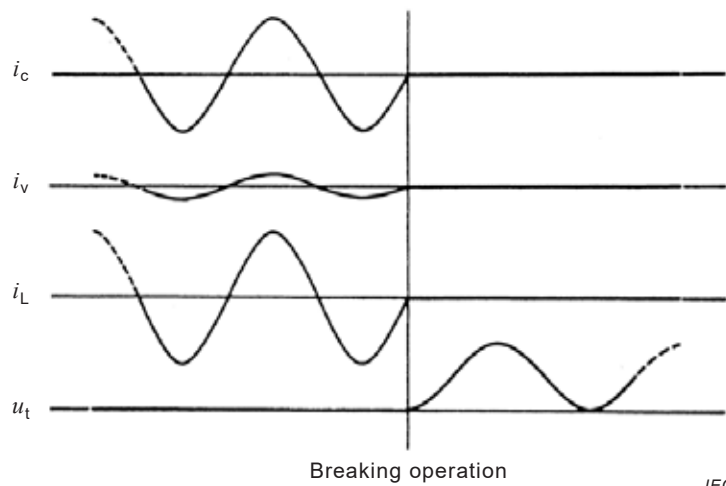
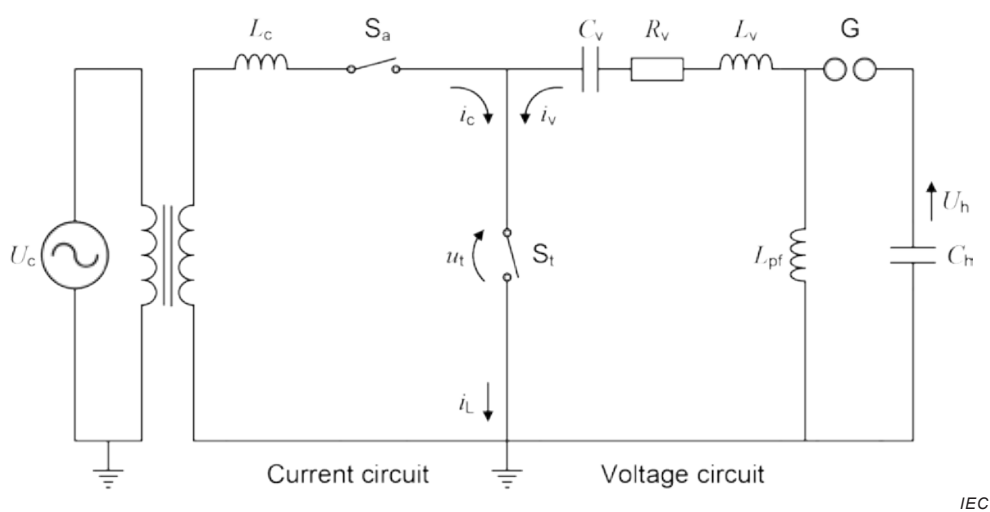


Figure G.1 – Power frequency circuits in parallel



$$U_h = \frac{(C_v + C_h)}{C_h} U_t \sqrt{2}$$

$$i_v = \frac{U_h}{\omega_0 L_v} e^{-\alpha t} \sin \omega_0 t, \text{ with } \alpha = \frac{R_v}{2L_v}$$

$$i_L = i_c + i_v$$

$$\text{and } \omega_0 = \sqrt{\frac{1}{L_v} \left(\frac{1}{C_h} + \frac{1}{C_v} \right) - \left(\frac{R_v}{2L_v} \right)^2}$$

$$\omega L_c = \frac{1}{n \times \omega \times C_L}$$

$$L_v = \frac{U_h}{i_L \times \omega \times \sqrt{2}}$$

$$f_{RV} = \frac{1}{2\pi \sqrt{C_h \times L_{pf}}}$$

C_L = equivalent load capacitance

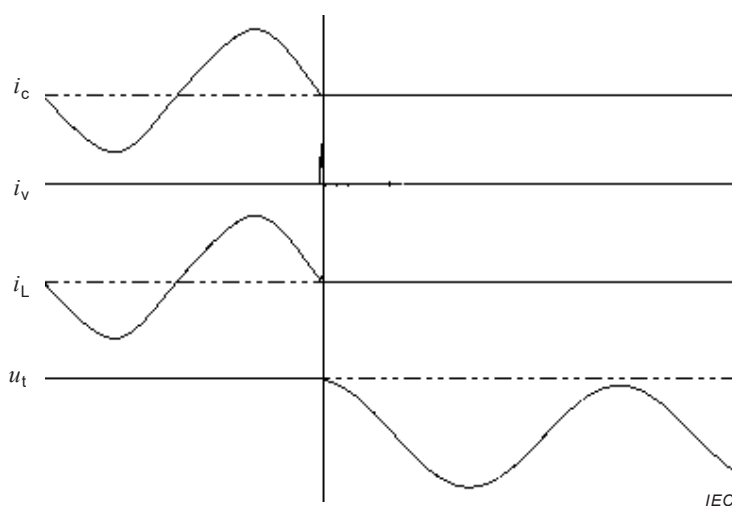
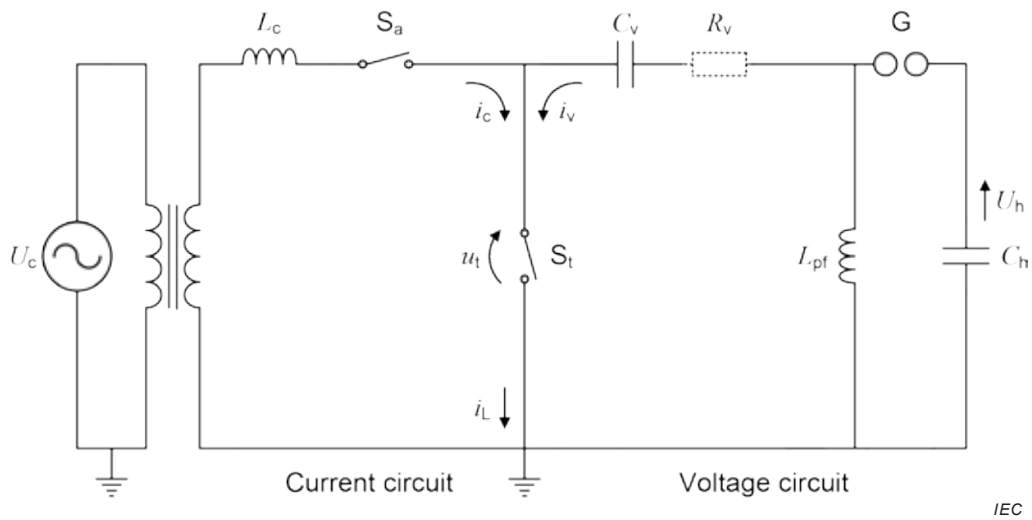


Figure G.2 – Current injection circuit



$$i_c = i_L - i_v$$

$$i_c = \frac{U_c}{\omega_r L_c}, \text{ with } \omega_r = 2\pi f_r$$

$$i_v = 2\pi f_L \times C_v \times U_h$$

$$U_h = U_t \sqrt{2}$$

$$f_L = \frac{1}{2\pi \sqrt{(C_h + C_v) \times L_{pf}}}$$

$$f_{RV} = \frac{1}{2\pi \sqrt{C_h \times L_{pf}}}$$

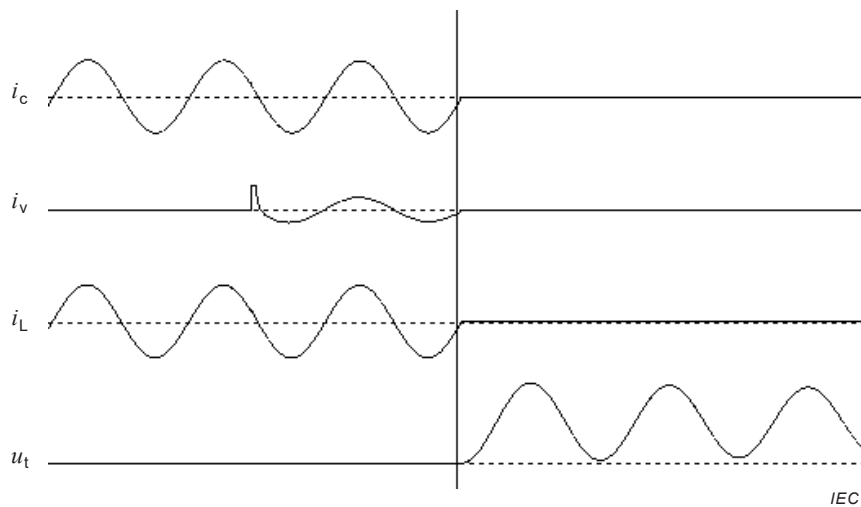
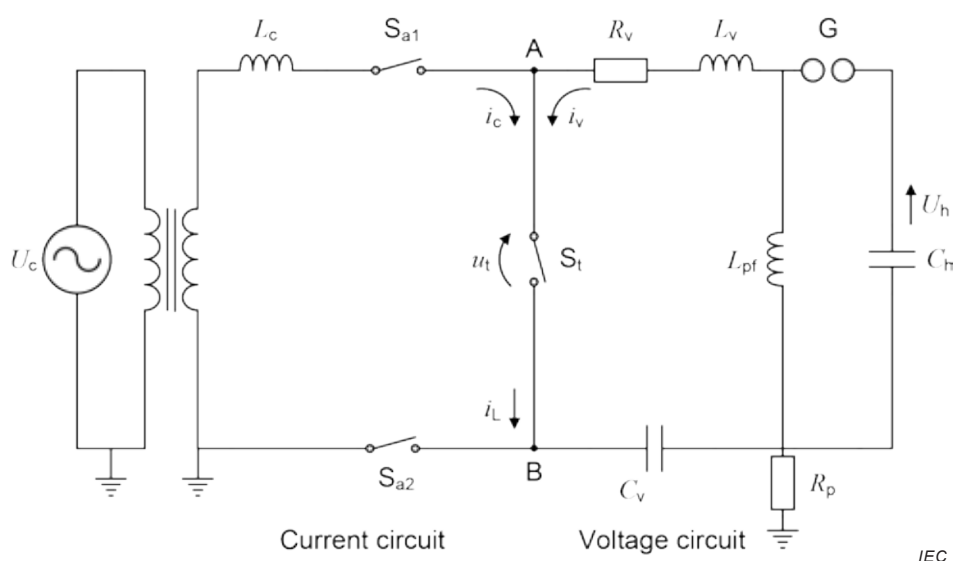


Figure G.3 – Power frequency current injection circuit



$$U_c = \frac{U_t}{n}$$

$$U_h = \frac{(C_v + C_h)}{C_h} U_t \sqrt{2}$$

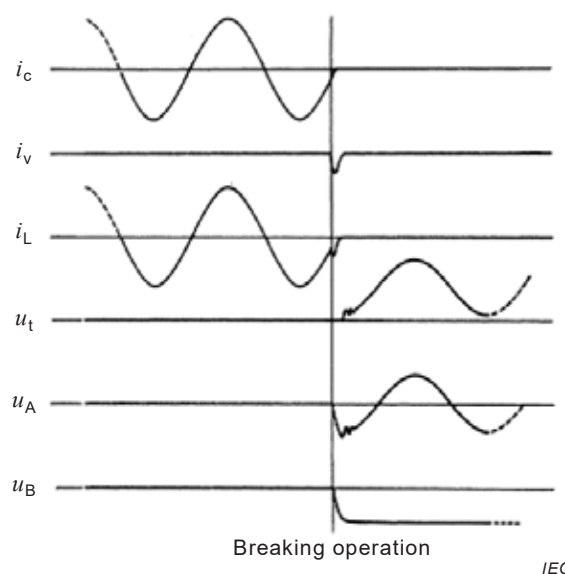
$$i_v = \frac{U_h}{\omega_0 L_v} e^{-\alpha t} \sin \omega_0 t, \text{ with } \alpha = \frac{R_v}{2L_v}$$

$$i_L = i_c + i_v$$

$$\text{and } \omega_0 = \sqrt{\frac{1}{L_v} \left(\frac{1}{C_h} + \frac{1}{C_v} \right) - \left(\frac{R_v}{2L_v} \right)^2}$$

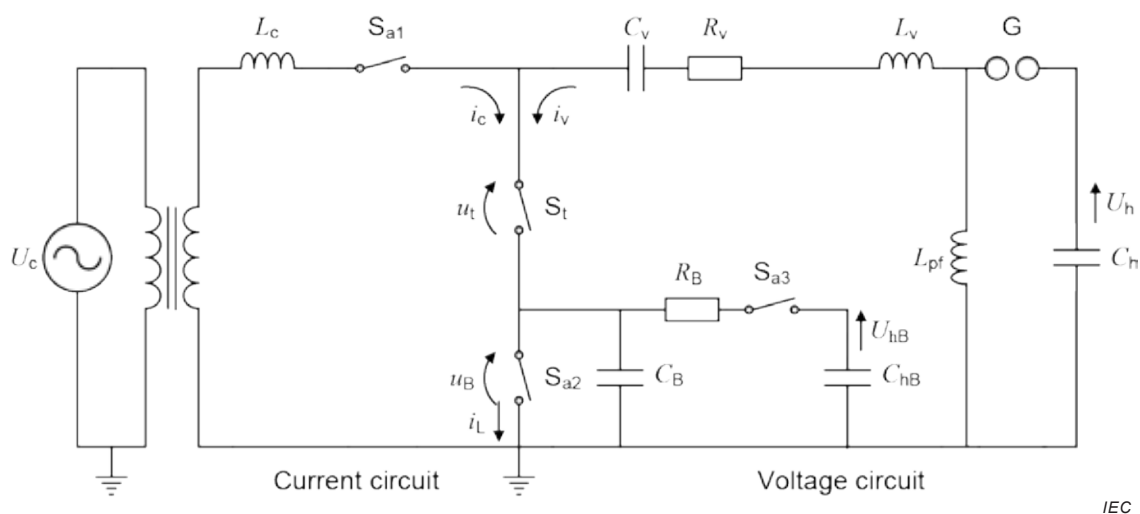
$$\omega L_c = \frac{1}{n \times \omega \times C_L}$$

$$L_v = \frac{U_h}{i_L \times \omega \times \sqrt{2}}$$



NOTE The circuit can also be used with the power frequency current injection method.

Figure G.4 – Current injection circuit, recovery voltage applied to both terminals of the circuit-breaker



IEC

$$U_c = \frac{U_t}{n}$$

$$i_L = i_c + i_v$$

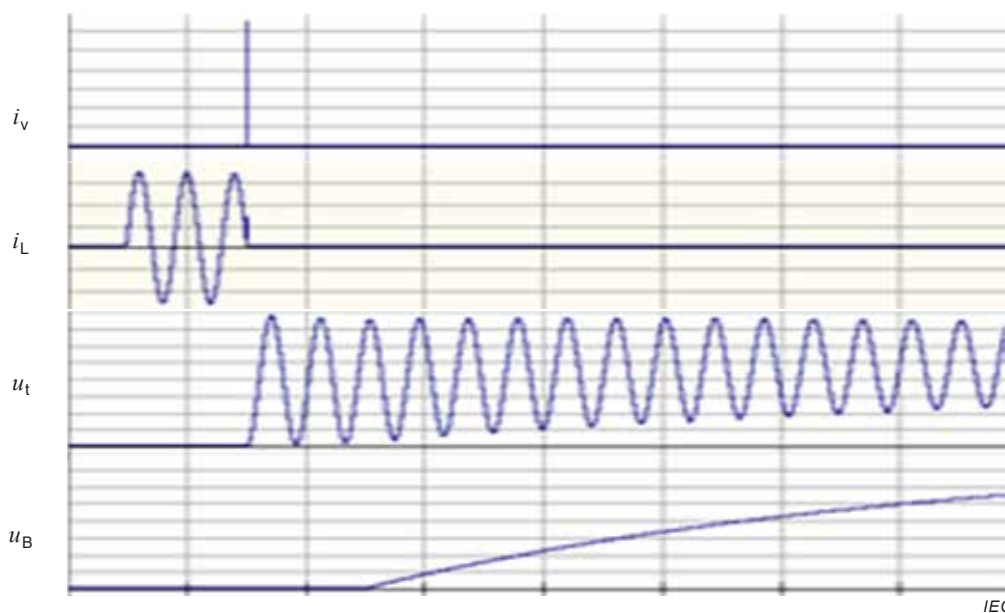
$$\omega L_c = \frac{1}{n \times \omega \times C_L}$$

$$U_h = \frac{(C_v + C_h)}{C_h} U_t \sqrt{2}$$

$$i_v = \frac{U_h}{\omega_0 L_v} e^{-\alpha t} \sin \omega_0 t, \text{ with } \alpha = \frac{R_v}{2L_v}$$

$$\text{and } \omega_0 = \sqrt{\frac{1}{L_v} \left(\frac{1}{C_h} + \frac{1}{C_v} \right) - \left(\frac{R_v}{2L_v} \right)^2}$$

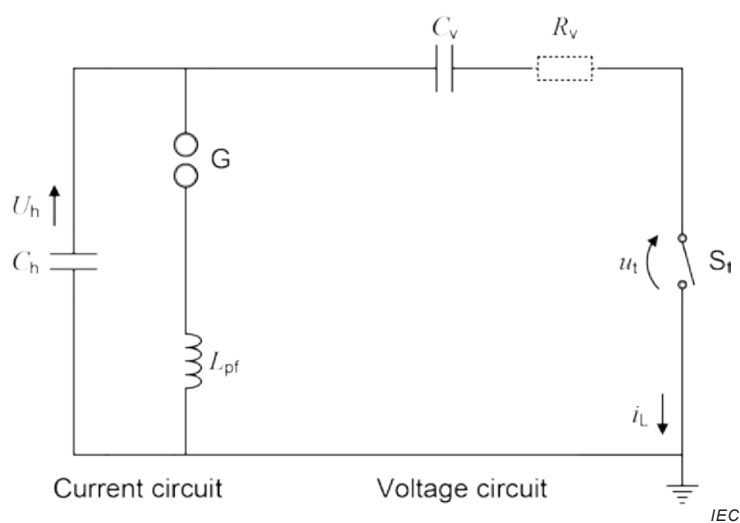
$$L_v = \frac{U_h}{i_L \times \omega \times \sqrt{2}}$$



IEC

NOTE The circuit can also be used with the power frequency current injection method.

Figure G.5 – Current injection circuit with decay compensation



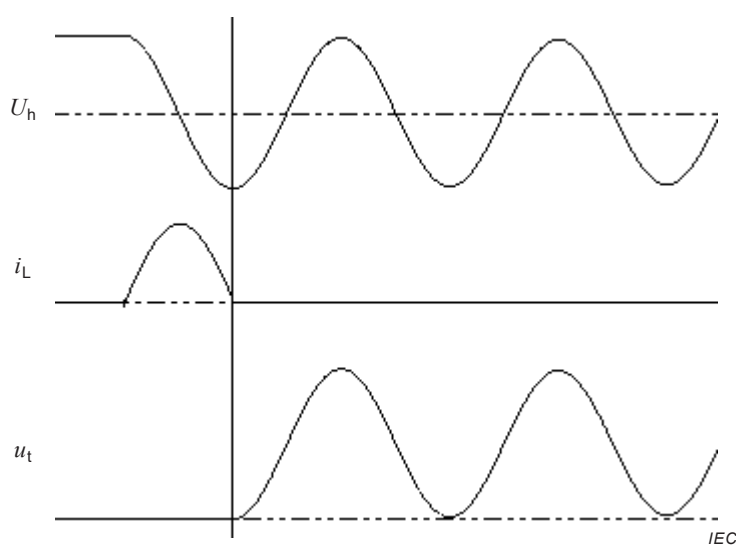
$$U_h = U_t \sqrt{2}$$

$$i_L = 2\pi f_L \times C_v \times U_h$$

$$f_{RV} = \frac{1}{2\pi \sqrt{C_h \times L_{pf}}}$$

$$f_L = \frac{1}{2\pi \sqrt{(C_h + C_v) \times L_{pf}}}$$

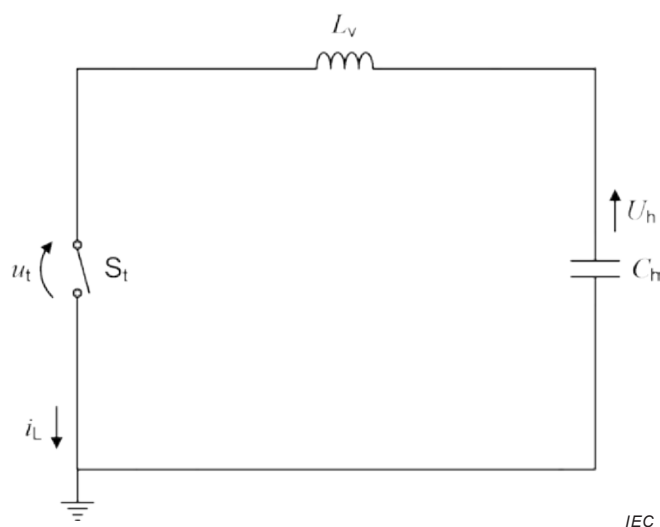
C_v = equivalent load capacitance



C_h and C_v are pre-charged at the voltage U_h .

NOTE The load side capacitance C_v can also be inserted between the test circuit-breaker and earth. Care should be taken to the correct voltage distribution in case of metal enclosed circuit-breakers.

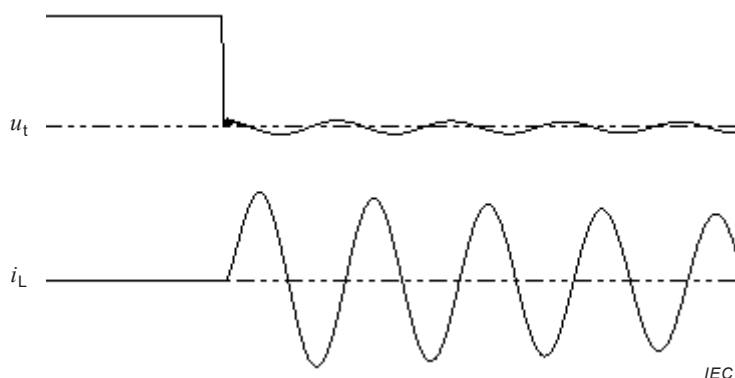
Figure G.6 – LC oscillating circuit



$$U_h = U_t \times \sqrt{2}$$

$$i_{\text{max peak}} = U_h \times C_h \times 2\pi f_{\text{inrush}}$$

$$f_{\text{inrush}} = \frac{1}{2\pi\sqrt{C_h \times L_v}}$$



NOTE This circuit does not reproduce possible interactions for back-to-back inrush making current test when the circuit-breaker can clear during the pre-arc interval.

Figure G.7 – Inrush making current test circuit

Annex H (informative) Re-ignition methods to prolong arcing

Replace the title of Annex H by the following:

Step-by-step method to prolong arcing

H.1 “Step-by-step” method

Delete the existing title.

Delete the last two sentences of the first paragraph.

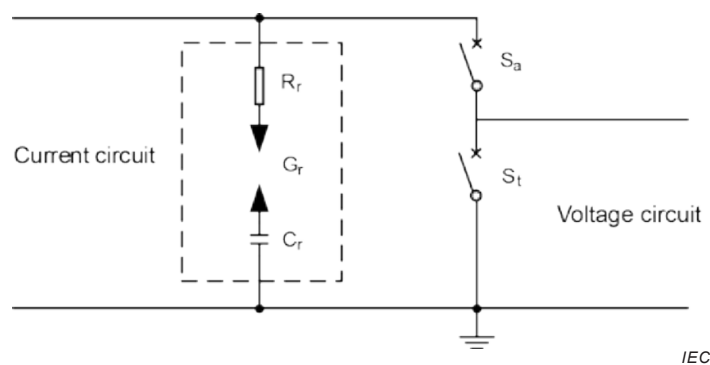
Replace, in item a), "Figure H.1" by "Figure H.1 and Figure H.2".

H.2 Method using a duplicate circuit

Delete H.2.

Figure H.1 – Typical re-ignition circuit diagram for prolonging arc-duration

Replace Figure H.1 by the following:



Key

S_t test circuit-breaker
 S_a auxiliary circuit-breaker
 R_r resistor for re-ignition circuit

C_r capacitor for re-ignition circuit
 G_r spark gap for closing re-ignition circuit

Figure H.1 – Example of a re-ignition circuit diagram for prolonging arc-duration

Figure H.2 – Combined Skeats and current injection circuits

Replace Figure H.2 by the following:

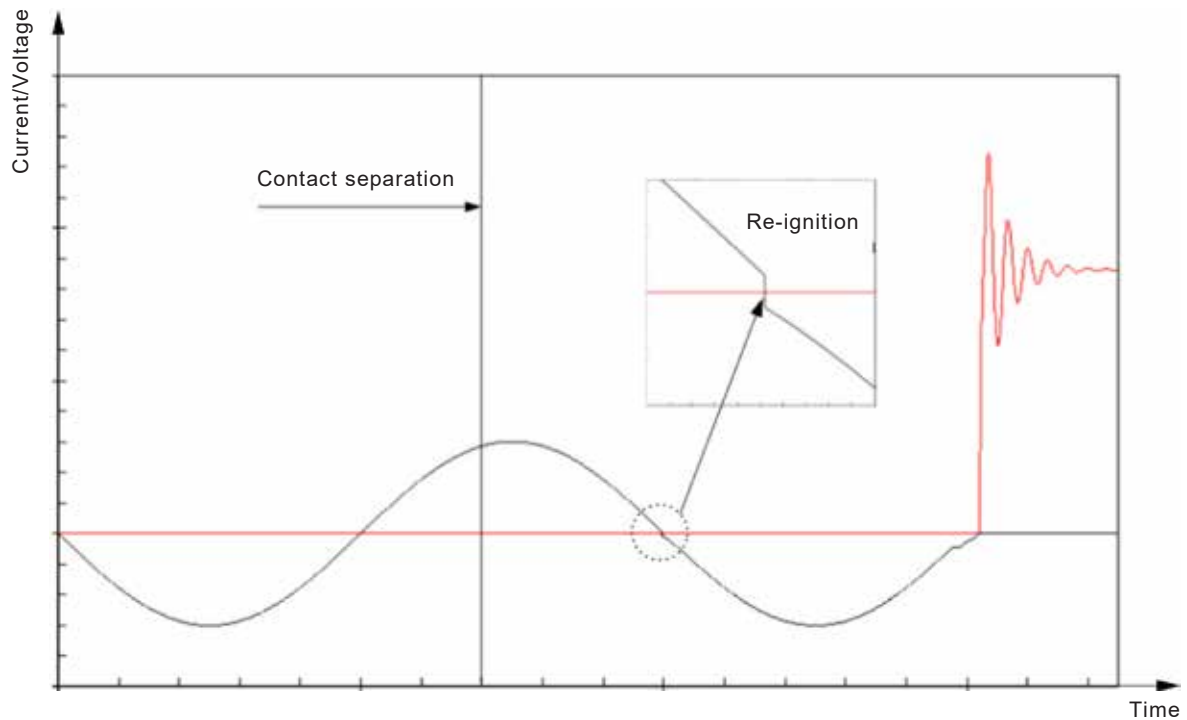


Figure H.2 – Example of waveforms obtained during a symmetrical test using the circuit in Figure H.1

Figure H.3 – Typical waveforms obtained during an asymmetrical test using the circuit in Figure H.2

Delete the existing title and figure.

Annex I (normative) Reduction in di/dt and TRV for test duty T100a

Replace the entire annex by the following:

Annex I (normative)

Correction of di/dt and TRV for test duty T100a

I.1 General

During asymmetrical fault condition, the resultant di/dt and TRV are modified by the d.c. component of the fault current.

There are two options:

- 1) Test circuit set to obtain the rated TRV associated with T100s

In that case, it is impossible to meet simultaneously all parameters (di/dt , u_1 and u_c) since these parameters are not varying linearly with the d.c. component at current zero. The charging voltage of the synthetic circuit shall be set to obtain the most onerous test parameter. For tests on the major loop, the most onerous test parameter is always di/dt while the most onerous parameter for tests on the subsequent minor loop is u_c . In case of voltage injection test method, the most onerous test parameter for tests on major loop becomes u_1 .

- 2) Use two different test circuits; one circuit set to obtain the modified TRV associated with tests on the minor loop and a second circuit set to obtain the modified TRV associated with tests on the major loop.

In that case all required parameters (di/dt , u_1 and u_c) can be met simultaneously.

The choice of the option is left to the manufacturer since option 1) may overstress the circuit-breaker (for example for tests on major loop, the required correction on di/dt will produce a higher u_c than required).

I.2 Reduction in di/dt

For the last current loop parameters, refer to Tables I.7 and I.8 and Tables L.12 through L.17.

I.3 Corrected TRV for the first-pole-to-clear with required asymmetry

Tables I.1 through I.6 cover the corrected TRV values for $k_{pp} = 1,5$, 1,3 and 1,2 for $f_r = 50$ Hz and $f_r = 60$ Hz.

Table I.1 – Corrected TRV values for the first-pole-to-clear for $k_{pp} = 1,3$ and $f_r = 50$ Hz

Minimum clearing time ms		10,0 < t ≤ 27,0		27,0 < t ≤ 47,5		47,5 < t ≤ 68,0		68,0 < t ≤ 87,9			
	U _r kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV		
τ=45 ms major loop	100	74	136	78	144	79	147	a	a		
	123	90	166	96	177	97	181				
	145	106	195	113	208	115	213				
	170	125	228	132	243	134	249				
	245	179	325	190	348	194	357				
	300	219	394	232	423	237	436				
	362	264	471	280	508	286	524				
	420	306	541	324	586	331	606				
	550	399	693	424	757	433	787				
800	576	965	613	1 074	628	1 126					
τ = 45 ms subsequent minor loop	100	72	135	76	143	78	146	a	a		
	123	88	167	94	176	96	180				
	145	104	197	110	208	113	212				
	170	122	232	129	244	132	249				
	245	176	338	187	354	191	360				
	300	216	417	229	435	234	442				
	362	261	507	276	528	283	535				
	420	304	593	321	615	328	623				
	550	399	789	421	814	430	821				
800	584	1 184	615	1 207	627	1 209					

Minimum clearing time ms		10,0 < t ≤ 27,0		27,0 < t ≤ 47,5		47,5 < t ≤ 67,5		67,5 < t ≤ 88,0			
	U _r kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV		
τ = 60 ms major loop	100	69	127	75	138	77	143	79	146		
	123	85	155	92	169	95	176	97	179		
	145	100	182	108	199	112	207	114	211		
	170	117	212	127	232	131	242	134	247		
	245	168	301	182	331	189	347	192	355		
	300	205	364	223	403	231	422	235	433		
	362	247	434	269	482	279	506	284	520		
	420	286	497	311	554	323	584	329	601		
τ = 60 ms subsequent minor loop	100	68	128	73	138	76	143	78	146		
	123	83	159	90	171	94	177	96	180		
	145	98	188	107	202	111	209	113	212		
	170	115	221	125	237	130	245	132	249		
	245	167	323	181	345	187	355	191	360		
	300	205	399	221	425	229	437	234	442		
	362	248	487	267	517	277	530	282	536		
	420	288	570	311	603	322	618	328	623		

Minimum clearing time ms		10,0 < t ≤ 27,0		27,0 < t ≤ 47,5		47,5 < t ≤ 67,5		67,5 < t ≤ 87,5		87,5 < t ≤ 108	
	U _r kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV
τ = 75 ms major loop	550	349	580	388	669	409	722	421	754	428	775
	800	501	785	560	928	592	1 015	610	1 070	621	1 106
τ = 75 ms subsequent minor loop	550	360	737	394	786	413	808	423	819	429	823
	800	529	1 126	577	1 184	603	1 207	618	1 215	626	1 216

^a Test duty T100a is not applicable, asymmetry level lower than 20 % for both current loops.

^a Test duty T100a is not applicable, asymmetry level lower than 20 % for both current loops.

Table I.2 – Corrected TRV values for the first-pole-to-clear for $k_{pp} = 1,3$ and $f_r = 60$ Hz

Minimum clearing time ms		8,5 < t ≤ 22,5		22,5 < t ≤ 39,5		39,5 < t ≤ 56,5		56,5 < t ≤ 73,0					
	U_r kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV				
$\tau = 45$ ms major loop	100	71	130	76	140	78	145	a	a				
	123	87	159	93	172	96	178						
	145	102	186	110	202	113	209						
	170	120	217	129	236	133	244						
	245	172	307	185	336	191	350						
	300	210	371	226	408	234	426						
	362	253	441	273	488	282	511						
	420	293	505	316	561	326	589						
	550	381	640	412	720	426	761						
800	548	873	595	1 006	617	1 079							
$\tau = 45$ ms subsequent minor loop	100	69	132	75	141	77	145	a	a				
	123	85	163	92	173	95	178						
	145	101	192	108	205	112	211						
	170	118	227	127	241	131	247						
	245	171	331	183	351	189	359						
	300	210	410	225	432	232	441						
	362	254	501	272	525	280	535						
	420	295	587	315	614	325	624						
	550	388	787	414	816	426	825						
800	570	1 196	607	1 223	623	1 225							
Minimum clearing time ms		8,5 < t ≤ 22,5		22,5 < t ≤ 39,5		39,5 < t ≤ 56,5		56,5 < t ≤ 73,0		73,0 < t ≤ 90,0			
	U_r kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV		
$\tau = 60$ ms major loop	100	66	120	72	133	76	140	78	144	a	a		
	123	81	146	89	162	93	171	95	176				
	145	95	171	104	191	110	201	112	207				
	170	111	199	122	222	128	235	132	242				
	245	159	281	176	316	185	335	189	346				
	300	194	338	215	382	226	407	232	422				
	362	234	400	259	455	272	487	279	505				
	420	270	456	299	522	315	560	324	582				
$\tau = 60$ ms subsequent minor loop	100	65	124	71	135	75	141	77	144	a	a		
	123	80	153	88	167	92	174	94	178				
	145	94	181	104	197	108	206	111	210				
	170	111	214	121	232	127	242	131	247				
	245	160	314	175	339	184	352	188	358				
	300	197	390	215	419	225	434	231	441				
	362	238	478	260	511	272	527	279	535				
	420	277	562	303	599	316	616	324	624				
Minimum clearing time ms		8,5 < t ≤ 22,5		22,5 < t ≤ 39,5		39,5 < t ≤ 56,0		56,0 < t ≤ 73,0		73,0 < t ≤ 90,0		90,0 < t ≤ 106,5	
	U_r kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV
$\tau = 75$ ms major loop	550 800	327 467	517 676	369 531	615 832	395 569	677 935	410 593	718 1 004	420 608	746 1 052	426 618	765 1 087
$\tau = 75$ ms subsequent minor loop	550 800	345 509	730 1 134	382 561	782 1 195	403 591	808 1 221	416 609	821 1 231	424 620	827 1 233	429 627	830 1 230
a Test duty T100a is not applicable, asymmetry level lower than 20 % for both current loops.													

Table I.3 – Corrected TRV values for the first-pole-to-clear for $k_{pp} = 1,5$ and $f_r = 50$ Hz

Minimum clearing time ms		10,0 < t ≤ 27,0		27,0 < t ≤ 47,5		47,5 < t ≤ 68,0		68,0 < t ≤ 87,9	
	U_r kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV
τ =45 ms major loop	72,5	b	114	b	121	b	123	a	a
	100	85	156	90	166	91	169		
	123	104	191	110	203	112	208		
	145	123	224	130	239	132	245		
	170	144	262	152	280	155	286		
τ =45 ms subsequent minor loop	72,5	b	113	b	119	b	122	a	a
	100	83	156	88	165	90	169		
	123	102	193	108	203	111	208		
	145	120	228	127	240	130	245		
	170	141	269	149	282	153	288		

Minimum clearing time ms		10,0 < t ≤ 27,0		27,0 < t ≤ 47,5		47,5 < t ≤ 67,5		67,5 < t ≤ 88,0	
	U_r kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV
τ =60 ms major loop	72,5	b	106	b	116	b	120	b	122
	100	79	146	86	159	89	165	91	168
	123	98	178	106	195	110	203	112	207
	145	115	209	125	229	129	238	132	243
	170	135	243	146	267	152	279	154	285
τ =60 ms subsequent minor loop	72,5	b	107	b	116	b	120	b	122
	100	78	149	85	160	88	166	90	168
	123	96	184	104	197	108	204	110	207
	145	114	217	123	233	128	241	130	245
	170	133	256	144	275	150	283	153	287

^a Test duty T100a is not applicable, asymmetry level lower than 20 % for both current loops.

^b u_1 is not defined for a two parameter TRV.

Table I.4 – Corrected TRV values for the first-pole-to-clear for $k_{pp} = 1,5$ and $f_r = 60$ Hz

Minimum clearing time ms		8,5 < t ≤ 22,5		22,5 < t ≤ 39,5		39,5 < t ≤ 56,5		56,5 < t ≤ 73,0		73,0 < t ≤ 90,0	
	U _r kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV
τ=45 ms major loop	72,5	b	109	b	117	b	121	b	123	a	a
	100	81	149	88	161	90	167	91	169		
	123	100	182	108	198	111	205	112	208		
	145	118	213	127	232	131	241	132	245		
	170	138	249	148	271	153	281	155	286		
τ=45 ms subsequent minor loop	72,5	b	110	b	117	b	121	b	123	a	a
	100	80	152	86	162	89	167	90	169		
	123	99	188	106	201	109	206	111	209		
	145	116	223	125	237	129	243	131	246		
	170	137	263	147	279	151	286	154	289		

Minimum clearing time ms		8,5 < t ≤ 22,5		22,5 < t ≤ 39,5		39,5 < t ≤ 56,5		56,5 < t ≤ 73,0		73,0 < t ≤ 90,0	
	U _r kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV	u ₁ kV	u _c kV
τ=60 ms major loop	72,5	b	100	b	111	b	117	b	120	b	122
	100	76	137	83	153	87	161	89	165	91	168
	123	93	168	102	187	107	197	110	203	111	206
	145	109	196	120	219	126	231	130	238	131	243
	170	128	228	141	255	148	270	152	279	154	284
τ=60 ms subsequent minor loop	72,5	b	103	b	113	b	118	b	120	b	122
	100	75	143	82	156	86	163	89	167	90	169
	123	92	177	101	193	106	201	109	206	111	208
	145	109	210	120	228	125	238	128	243	130	246
	170	128	249	140	269	147	280	151	285	153	288

^a Test duty T100a is not applicable, asymmetry level lower than 20 % for both current loops.

^b u₁ is not defined for a two parameter TRV.

Table I.5 – Corrected TRV values for the first-pole-to-clear for $k_{pp} = 1,2$ and $f_r = 50$ Hz

Minimum clearing time ms		$10,0 < t \leq 27,0$		$27,0 < t \leq 47,0$		$47,0 < t \leq 67,5$		$67,5 < t \leq 87,5$		$87,5 < t \leq 108$	
	U_r kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV
$\tau = 120$ ms major loop	1 100	530	871	615	1 070	671	1 206	709	1 304	736	1 375
	1 200	574	924	667	1 145	729	1 297	772	1 406	801	1 487
$\tau = 120$ ms subsequent minor loop	1 100	597	1 374	669	1 491	715	1 559	746	1 599	766	1 623
	1 200	655	1 524	733	1 648	783	1 719	815	1 760	837	1 784

Table I.6 – Corrected TRV values for the first-pole-to-clear for $k_{pp} = 1,2$ and $f_r = 60$ Hz

Minimum clearing time ms		$8,5 < t \leq 22,5$		$22,5 < t \leq 39,0$		$39,0 < t \leq 56,0$		$56,0 < t \leq 73,0$		$73,0 < t \leq 89,5$		$89,5 < t \leq 106,5$	
	U_r kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV	u_1 kV	u_c kV
$\tau = 120$ ms major loop	1 100 1 200	483 522	727 760	569 617	931 987	629 683	1 077 1 150	672 730	1 187 1 272	704 765	1 271 1 367	728 792	1 336 1 440
$\tau = 120$ ms subsequent minor loop	1 100 1 200	571 628	1 373 1 531	645 707	1 490 1 653	693 760	1 561 1 727	727 796	1 605 1 772	751 822	1 632 1 799	768 840	1 649 1 815

Table I.7 – Percentage of d.c. component and di/dr at current zero for first-pole-to-clear for $f_r = 50$ Hz

τ	Minimum clearing time	Major loop		Subsequent minor loop			
		d.c. component	di/dr	d.c. component	di/dr	I_{peak}	loop duration
ms	ms	%	%	%	%	p.u.	ms
45	$10,0 < t \leq 27,0$	44,6	92,7	37,9	89,9	0,59	7,5
	$27,0 < t \leq 47,5$	28,9	97,8	24,1	95,3	0,74	8,5
	$47,5 < t \leq 68,0$	18,7 ^a	99,6	15,3 ^a	97,7	0,83	9,0
60	$10,0 < t \leq 27,0$	54,2	86,9	48,6	84,8	0,49	6,5
	$27,0 < t \leq 47,5$	39,2	94,1	34,5	92,0	0,63	7,5
	$47,5 < t \leq 67,5$	28,3	97,4	24,6	95,6	0,74	8,5
	$67,5 < t \leq 88,0$	20,3	99,0	17,6 ^a	97,5	0,81	9,0
75	$10,0 < t \leq 27,0$	61,0	81,8	56,4	80,2	0,41	6,0
	$27,0 < t \leq 47,5$	47,1	90,2	42,9	88,5	0,55	7,0
	$47,5 < t \leq 67,5$	36,3	94,7	32,7	93,1	0,66	8,0
	$67,5 < t \leq 87,5$	27,9	97,2	25,0	95,8	0,74	8,5
	$87,5 < t \leq 108,0$	21,4	98,6	19,1 ^a	97,3	0,80	8,5
120	$10,0 < t \leq 27,0$	73,1	70,2	70,2	69,4	0,28	5,0
	$27,0 < t \leq 47,0$	62,1	80,0	59,2	79,0	0,39	6,0
	$47,0 < t \leq 67,5$	52,8	86,4	50,0	85,3	0,49	6,5
	$67,5 < t \leq 87,5$	44,8	90,6	42,2	89,5	0,57	7,0
	$87,5 < t \leq 108,0$	38,0	93,5	35,6	92,4	0,63	7,5

^a Percentage of d.c. component lower than 20 %. Test to be performed without reduction of di/dr and/or TRV parameters.

Table I.8 – Percentage of d.c. component and di/dt at current zero for first-pole-to-clear for $f_r = 60$ Hz

τ	Minimum clearing time	Major loop		Subsequent minor loop			
		d.c. component	di/dt	d.c. component	di/dt	I_{peak}	loop duration
ms	ms	%	%	%	%	p.u.	ms
45	$8,5 < t \leq 22,5$	50,8	89,1	44,8	86,8	0,52	5,5
	$22,5 < t \leq 39,5$	35,4	95,6	30,6	93,4	0,67	6,5
	$39,5 < t \leq 56,5$	24,6	98,4	21,0	96,5	0,77	7,0
	$56,5 < t \leq 73,0$	17,1 ^a	99,5	14,5 ^a	98,1	0,84	7,5
60	$8,5 < t \leq 22,5$	59,8	82,8	55,0	81,1	0,43	5,0
	$22,5 < t \leq 39,5$	45,7	91,0	41,4	89,2	0,57	6,0
	$39,5 < t \leq 56,5$	34,8	95,3	31,2	93,6	0,67	6,5
	$56,5 < t \leq 73,0$	26,4	97,6	23,5	96,2	0,75	7,0
	$73,0 < t \leq 90,0$	20,1	98,6	17,8 ^a	97,6	0,81	7,5
75	$8,5 < t \leq 22,5$	66,1	77,4	62,1	76,2	0,36	4,5
	$22,5 < t \leq 39,5$	53,2	86,5	49,5	85,1	0,49	5,5
	$39,5 < t \leq 56,0$	42,8	91,9	39,5	90,5	0,59	6,0
	$56,0 < t \leq 73,0$	34,4	95,1	31,5	93,8	0,67	6,5
	$73,0 < t \leq 90,0$	27,6	97,1	25,2	95,9	0,74	7,0
	$90,0 < t \leq 106,5$	22,2	98,3	20,1	97,3	0,79	7,0
120	$8,5 < t \leq 22,5$	77,0	65,6	74,6	64,9	0,24	4,0
	$22,5 < t \leq 39,0$	67,2	75,6	64,7	74,8	0,34	4,5
	$39,0 < t \leq 56,0$	58,6	82,2	56,2	81,5	0,43	5,0
	$56,0 < t \leq 73,0$	51,1	87,1	48,8	86,2	0,50	5,5
	$73,0 < t \leq 89,5$	44,6	90,5	42,4	89,6	0,57	6,0
	$89,5 < t \leq 106,5$	38,8	93,0	36,9	92,2	0,62	6,5

^a Percentage of d.c. component lower than 20 %. Test to be performed without reduction of di/dt and/or TRV parameters.

I.4 Correction of the di/dt and TRV of the first-pole-to-clear for tests with intermediate asymmetry

For the last current loop parameters including di/dt , refer to Tables L.12 through L.17.

The RRRV and TRV peak can be calculated using the percentage reduction of di/dt at current zero after the intermediate major loop.

I.5 Correction of the di/dt and TRV of the second- or last-pole-to-clear with major extended loop with required asymmetry during three-phase tests

For the last current loop parameters including di/dt , refer to Tables L.12 through L.17.

The RRRV and TRV peak can be calculated using the ratio between the reduced di/dt at current zero after the major extended loop and the di/dt at current zero of the symmetrical short-circuit current of the second- or last-pole-to-clear with extended loop.

I.6 Correction of the di/dt and TRV during tests with a subsequent minor loop

For single-phase tests, the TRV for the subsequent minor loop shall be applied for the same pole-to-clear-factor as the failed major loop. The TRV values for the subsequent minor loop in case of a first-pole-to-clear may be derived from Tables I.1 through I.6 or can be calculated according I.7.

NOTE This test procedure reproduces the conditions during single-phase direct test which sufficiently covers the TRV conditions during three-phase test.

No correction is applied to three-phase tests.

I.7 Calculation of the di/dt and TRV of the first-pole-to-clear

I.7.1 General

Clause I.7 is applicable for asymmetrical fault conditions, on the phase with required asymmetry only, when values are not given in Tables I.1 through I.6, and L.12 through L.17.

I.7.2 Calculation of di/dt

For the di/dt , the maximum value is reached for symmetrical fault condition. During asymmetrical fault condition, the di/dt is reduced and is a function of the d.c. component at current zero. The di/dt at current zero is calculated by the following equations:

a) For minor loops:

$$\frac{di}{dt}(\text{p.u.})_- = \sqrt{(1-p^2)} - \frac{p}{2\pi f\tau} \quad (\text{I.1})$$

b) For major loops:

$$\frac{di}{dt}(\text{p.u.})_+ = \sqrt{(1-p^2)} + \frac{p}{2\pi f\tau} \quad (\text{I.2})$$

where

di/dt (p.u.) is the di/dt in p.u. of the symmetrical fault condition;

– is the index used to designate the minor loop;

– is the index used to designate the major loop;

p is the d.c. component at current zero in p.u.;

f is the frequency (Hz);

τ is the d.c. time constant of the short-circuit current (s).

I.7.3 Calculation of TRV

When the interruption occurs, the moment of current zero does not correspond with the peak of the applied voltage as it is the case during symmetrical fault condition. The d.c. component modifies the angular displacement between current zeros and the applied power frequency voltage. The TRV amplitude co-ordinates (u_1 , u_c) are then modified according to the phase shift between the moment of current zero and the peak of the applied power frequency voltage.

The corresponding TRV amplitude co-ordinates (u_1 , u_c) shall be calculated with the following equations:

a) Two parameter TRV:

$$u_c(\text{p.u.}) = \frac{k_1 A_1}{2\pi f} \quad (1.3)$$

and

$$k_{1-} = \sin(2\pi f t_3 - \arcsin(p)) + p \times e^{-\frac{t_3}{\tau}} \quad (\text{for the minor loop}) \quad (1.4)$$

$$k_{1+} = \sin(2\pi f t_3 + \arcsin(p)) - p \times e^{-\frac{t_3}{\tau}} \quad (\text{for the major loop}) \quad (1.5)$$

$$A_1 = \frac{2\pi f}{\sin(2\pi f t_3)} \quad (1.6)$$

where

- u_c is the TRV peak in p.u. of the symmetrical case;
- k_1 is the calculation constant;
- is the index used to designate the minor loop;
- is the index used to designate the major loop;
- A_1 is the calculation variable;
- p is the d.c. component at current zero in p.u.;
- f is the frequency (Hz);
- τ is the d.c. time constant of the short-circuit current (s);
- t_3 is the specified t_3 time co-ordinate (s).

b) Four parameter TRV:

$$u_1(\text{p.u.}) = \frac{k_1 A_1}{2\pi f} \quad (1.7)$$

and

$$k_{1-} = \sin(2\pi f t_1 - \arcsin(p)) + p \times e^{-\frac{t_1}{\tau}} \quad (\text{for the minor loop}) \quad (1.8)$$

$$k_{1+} = \sin(2\pi f t_1 + \arcsin(p)) - p \times e^{-\frac{t_1}{\tau}} \quad (\text{for the major loop}) \quad (1.9)$$

$$A_1 = \frac{2\pi f}{\sin(2\pi f t_1)} \quad (1.10)$$

where

- u_1 is the TRV peak in p.u. of the symmetrical case;
- k_1 is the calculation constant;
- is the index used to designate the minor loop;
- is the index used to designate the major loop;
- A_1 is the calculation variable;
- p is the d.c. component at current zero in p.u.;

f is the frequency (Hz);
 τ is the d.c. time constant of the short-circuit current (s);
 t_1 is the specified t_1 time co-ordinate (s).
 and

$$u_c(\text{p.u.}) = \frac{k_2 A_1}{\frac{1}{0,75} k_{af} \times 2\pi f} - \frac{k_3 A_2}{2\pi f} = \frac{0,75 \times k_2 A_1}{k_{af} \times 2\pi f} - \frac{k_3 A_2}{2\pi f} \quad (\text{I.11})$$

and

$$k_{2-} = \sin(2\pi f t_2 - \arcsin(p)) + p \times e^{-\frac{t_2}{\tau}} \quad (\text{for the minor loop}) \quad (\text{I.12})$$

$$k_{2+} = \sin(2\pi f t_2 + \arcsin(p)) - p \times e^{-\frac{t_2}{\tau}} \quad (\text{for the major loop}) \quad (\text{I.13})$$

$$k_{3-} = \sin(2\pi f (t_2 - t_1) - \arcsin(p)) + p \times e^{-\frac{(t_2 - t_1)}{\tau}} \quad (\text{for the minor loop}) \quad (\text{I.14})$$

$$k_{3+} = \sin(2\pi f (t_2 - t_1) + \arcsin(p)) - p \times e^{-\frac{(t_2 - t_1)}{\tau}} \quad (\text{for the major loop}) \quad (\text{I.15})$$

$$A_1 = \frac{2\pi f}{\sin(2\pi f t_1)} \quad (\text{I.16})$$

$$A_2 = \frac{\frac{A_1 \sin(2\pi f t_2)}{\frac{1}{0,75} k_{af}} - 2\pi f}{\sin(2\pi f (t_2 - t_1))} = \frac{\frac{0,75 \times A_1 \sin(2\pi f t_2)}{k_{af}} - 2\pi f}{\sin(2\pi f (t_2 - t_1))} \quad (\text{I.17})$$

where

u_c is the TRV peak in p.u. of the symmetrical case;
 k_{af} is the amplitude factor;
 k_2 is the calculation variable;
 k_3 is the calculation variable;
 $-$ is the index used to designate the minor loop;
 $+$ is the index used to designate the major loop;
 A_1 is the calculation variable;
 A_2 is the calculation variable;
 p is the d.c. component at current zero in p.u.;
 f is the frequency (Hz);
 τ is the d.c. time constant of the short-circuit current (s);
 t_1 is the specified t_1 time co-ordinate (s);
 t_2 is the specified t_2 time co-ordinate (s).

1.7.4 Examples of calculation of di/dt and TRV

As an example the following parameters are considered:

– rated voltage:	145 kV
– rated frequency:	50 Hz
– rated short-circuit current:	40 kA
– d.c. time constant of the short-circuit current:	45 ms
– rated first-pole-to-clear factor:	1,3
– minimum clearing time:	43 ms
– TRV (symmetrical case): u_1	115 kV
t_1	58 μ s
u_c	215 kV
t_2	232 μ s

For the first-pole-to-clear (major loop) the following parameters apply according to:

- Table I.7 percentage of the d.c. component at current zero: 28,9 % (0,289 p.u.);
- Table I.7 percentage of di/dt at current zero: 97,8 % (0,978 p.u.).

Some circuit-breakers will not clear at the end of a major loop after the required arcing time. For the subsequent minor current loop the following parameters apply according to:

- Table I.7 percentage of the d.c. component at current zero: 24,1 % (0,241 p.u.)
- Table I.7 percentage of di/dt at current zero: 95,3 % (0,953 p.u.).

The following values are calculated from the previous equations:

$$\begin{aligned}
 k_{1-} &= 0,01741; \\
 k_{1+} &= 0,01777; \\
 A_1 &= 17\,242,33; \\
 u_{1-} &= 0,95568 \text{ p.u.}; \\
 u_{1+} &= 0,97513 \text{ p.u.}; \\
 k_{2-} &= 0,07007; \\
 k_{2+} &= 0,07043; \\
 k_{3-} &= 0,05246; \\
 k_{3+} &= 0,05299; \\
 A_2 &= 6\,561,19; \\
 u_{c-} &= 0,96481 \text{ p.u.}; \\
 u_{c+} &= 0,96419 \text{ p.u.}
 \end{aligned}$$

With these results, the resultant modified di/dt and TRV to be applied to the circuit-breaker are:

a) For the major loop:

$$\begin{aligned}
 di/dt &= 0,978 \text{ p.u.} \times 40 \text{ kA} \times \sqrt{2} \times 2\pi f = 17,38 \text{ A}/\mu\text{s}; \\
 u_1 &= 0,97513 \text{ p.u.} \times 115 \text{ kV} = 112 \text{ kV}; \\
 t_1 &= 58 \mu\text{s}; \\
 u_1/t_1 &= 1,93 \text{ kV}/\mu\text{s} \\
 u_c &= 0,96419 \text{ p.u.} \times 215 \text{ kV} = 207 \text{ kV};
 \end{aligned}$$

$$t_2 = 232 \mu\text{s}.$$

b) For the subsequent minor loop:

$$di/dt = 0,953 \text{ p.u.} \times 40 \text{ kA} \times \sqrt{2} \times 2\pi f = 16,93 \text{ A}/\mu\text{s};$$

$$u_1 = 0,95568 \text{ p.u.} \times 115 \text{ kV} = 110 \text{ kV};$$

$$t_1 = 58 \mu\text{s};$$

$$u_1/t_1 = 1,89 \text{ kV}/\mu\text{s}$$

$$u_c = 0,96481 \text{ p.u.} \times 215 \text{ kV} = 207 \text{ kV};$$

$$t_2 = 232 \mu\text{s}.$$

J.3 Three-phase synthetic circuit with injection in two phases

Add, before Figure J.1, the following paragraph:

The circuit in Figure J.5 is not applying the correct voltage between phases, as no TRV and recovery voltage is applied on one phase. Therefore, care should be taken when using this circuit, for example for circuit-breaker having all three poles in the same enclosure. This circuit could be used in combination with multi-part testing.

Annex K (normative) Test procedure using a three-phase current circuit and one voltage circuit

Replace the existing text, including figures, by the following:

K.1 Test circuit

The circuit-breaker shall be connected in a test circuit, an example of which is given in Figure K.1 with the following requirements:

- A three-phase current source with the neutral point of the supply isolated and the short-circuit point earthed as shown in Figure 25a of IEC 62271-100:2008. This gives a first-pole-to-clear factor of 1,5. Alternatively, the neutral point of the supply can be connected to earth by an appropriate impedance and the short-circuit point earthed, as shown in Figure 26a of IEC 62271-100:2008, to give a first-pole-to-clear factor of 1,3;
- An auxiliary circuit-breaker used to disconnect the current circuit from the voltage circuit;
- A parallel current-injection voltage circuit is shown in IEC 62271-306. This circuit is used to apply the TRV and the recovery voltage. It is connected between the pole representing the pole-to-clear and earth as required by the test procedures given in Tables K.1 through K.10. It is possible to provide a.c. power-frequency recovery voltage by use of additional impedance, L_{ac} ;
- Re-ignition circuits connected to each phase to prolong the arcing of the test circuit-breaker through the necessary number of zeros of the power-frequency current.