

Printed boards —

Part 4: Rigid multilayer printed boards with interlayer connections — Sectional specification —

Section 1: Capability detail specification — Performance levels A, B and C

The European Standard EN 62326-4-1:1997 has the status of a British Standard

ICS 31.180

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National foreword

This British Standard is the English language version of EN 62326-4-1:1997. It is identical with IEC 2326-4-1:1996.

This Section of BS EN 62326 forms the capability detail specification in the IEC quality assessment system for electronic components (IECQ) for rigid multilayer printed boards with interlayer connections with performance levels A, B and C. In the IECQ system, this specification is numbered QC 230401.

The UK participation in its preparation was entrusted to Technical Committee EPL/52, Printed circuits, which has the responsibility to:

- aid enquirers to understand the text;
- present to the responsible international/European committee any enquiries on the interpretation, or proposals for change, and keep the UK interests informed;
- monitor related international and European developments and promulgate them in the UK.

A list of organizations represented on this committee can be obtained on request to its secretary.

Cross-references

Attention is drawn to the fact that Annex ZA lists normative references to international publications with their corresponding European publications. The British Standards which implement these international or European publications may be found in the BSI Standards Catalogue under the section entitled “International Standards Correspondence Index”, or using the “Find” facility of the BSI Standards Electronic Catalogue.

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Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, the EN title page, pages 2 to 62, an inside back cover and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

This British Standard, having been prepared under the direction of the Electrotechnical Sector board, was published under the authority of the Standards Board and comes into effect on 15 June 1997

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English version

Printed boards
Part 4: Rigid multilayer printed boards with interlayer
connections Sectional specification
Section 1: Capability Detail Specification
Performance levels A, B and C

(IEC 2326-4-1:1996)

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zum Nachweis der Befähigung

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This European Standard was approved by CENELEC on 1996-12-09. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Foreword

The text of document 52/656/FDIS, future edition 1 of IEC 2326-4-1, prepared by IEC TC 52, Printed circuits, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 62326-4-1 on 1996-12-09.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 1997-09-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) —

This section 1 of part 4 is to be used in conjunction with EN 62326-1:1997 and EN 62326-4:1997

Annexes designated “normative” are part of the body of the standard.

Annexes designated “informative” are given for information only.

In this standard, Annex ZA is normative and Annex A, Annex B and Annex C are informative. Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 2326-4-1:1996 was approved by CENELEC as a European Standard without any modification.

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1 Scope

This Capability Detail Specification (Cap DS) is based on IEC 2326-4. It relates to rigid multilayer printed boards with interlayer connections manufactured with materials specified in **3.1**. It specifies the capability qualifying component (CQC), the characteristics to be tested, the test methods and conditions to be applied and the requirements to be fulfilled for testing capability for performance level A, B or C.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of IEC 2326-4. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this section of IEC 2326-4 are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 68-2-3:1969, *Environmental testing — Part 2: Tests — Test Ca: Damp heat, steady state*.

IEC 68-2-20:1979, *Environmental testing — Part 2: Tests — Test T: Soldering*.

IEC 68-2-38:1974, *Environmental testing — Part 2: Tests — Test Z/AD: Composite temperature/humidity cyclic test*.

IEC 249-3-3:1991, *Base materials for printed circuits — Part 3: Special materials used in connection with printed circuits — Specification No. 3: Permanent polymer coating materials (solder resist) for use in the fabrication of printed boards*.

IEC/FDIS 1189-3, *Test methods for electrical materials, interconnection structures and assemblies — Part 3: Test methods for interconnection structures¹⁾*.

IEC 2326-1:1996, *Printed boards — Part 1: Generic specification*.

IEC 2326-4:1996, *Printed boards — Part 4: Rigid multilayer printed boards with interlayer connections — Sectional specifications*.

3 Capability qualifying component (CQC)

Test specimens to be used as CQCs are described in clause **6** and shall:

- be made of one of the copper clad base materials and one of the bonding sheet materials specified in **3.1**;
- have a construction that has one set of characteristics identified in Table 2;
- bear the required portions of the capability test board specified in **6.1**; as an alternative a production panel may be used. Portions of the production panel may be used as test specimens provided that they are similar to those shown in Figure 1.

¹⁾ At present at the stage of Final Draft International Standard.

3.1 Materials

Table 1 — Materials

Material group code	Base material	
	IEC	Type
M1	1249-2-7	Part 2: <i>Sectional specification set for reinforced base materials, clad and unclad —</i> Section 7: <i>Epoxide woven glass laminate</i>
	1249-4-1	Part 4: <i>Sectional specification set for prepreg materials, unclad —</i> Section 1: <i>Epoxide woven glass prepregs</i>
M2	1249-2-11	Part 2: <i>Sectional specification set for reinforced base materials, clad and unclad —</i> Section 11: <i>Polyimide woven glass laminate</i>
	1249-4-1	Part 4: <i>Sectional specification set for prepreg materials, unclad —</i> Section 1: <i>Epoxide woven glass prepregs</i>
M3	1249-2-9	Part 2: <i>Sectional specification set for reinforced base materials, clad and unclad —</i> Section 9: <i>Bismaleimide/Triazine modified epoxide woven glass laminate</i>
	1249-4-1	Part 4: <i>Sectional specification set for prepreg materials, unclad —</i> Section 1: <i>Epoxide woven glass prepregs</i>

3.2 Product capability

The individual test specimens (ITS) containing the CQC for capability testing shall represent the grade of capability. This grade may be described by an alphanumeric codification developed from Table 2. To each codification letter from Table 2 representing three or one properties (three for the characteristics A, B, C, D and one for E) belong three or one of the figures (digit) 1 to 9 representing the grade of the relevant property. The sequence of these figures corresponds to the sequence of the properties stated in Table 2. For example: A356B435C456D334E6.

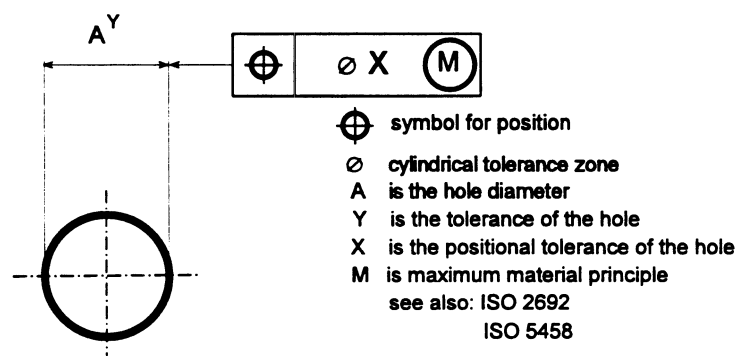
Table 2 — Product capability

Criteria			Code indication	1	2	3	4	5	6	7	8	9
BOARD	Board size (diagonal)	mm	A	≤ 150	250	350	450	550	650	750	850	> 850
	Total board thickness	mm		≤ 0,5	1,0	1,6	2,0	2,5	3,5	5,0	6,5	> 6,5
	Number of conductive layers	—		3-4	5-6	7-8	9-12	13-16	17-20	21-24	25-28	> 28
HOLES	Diameter of as-drilled holes	mm	B	≥ 0,6	0,5	0,4	0,35	0,30	0,25	0,20	0,15	< 0,15
	Total tolerance of drilled holes (min.-max.)	mm		≥ 0,300	0,250	0,200	0,150	0,125	0,100	0,075	0,050	< 0,050
	Location of hole. Positional tolerance ^b	mm		≥ 0,60	0,50	0,40	0,30	0,25	0,20	0,15	0,10	< 0,10
CONDUCTORS ^a	Unplated (inner layers)	Minimum electrical clearance	mm	C	≥ 0,500	0,350	0,250	0,200	0,150	0,125	0,100	< 0,075
		Minimum conductor width	mm		≥ 0,300	0,250	0,200	0,150	0,125	0,100	0,075	< 0,050
		Conductor process allowance (min.-max.)	mm		≥ 0,150	0,100	0,075	0,050	0,040	0,030	0,025	< 0,020
	Plated (outer layers)	Minimum electrical clearance	mm	D	≥ 0,500	0,350	0,250	0,200	0,150	0,125	0,100	< 0,075
		Minimum conductor width	mm		≥ 0,300	0,250	0,200	0,150	0,125	0,100	0,075	< 0,050
		Conductor process allowance (min.-max.)	mm		≥ 0,150	0,100	0,075	0,050	0,040	0,030	0,025	< 0,020
POSITIONAL	Location of features (conductive and non-conductive pattern) Positional tolerance ^b	mm	E	≥ 0,60	0,50	0,40	0,30	0,25	0,20	0,15	0,10	< 0,10

^a The grid (or pitch) can be calculated as follows:

minimum electrical clearance + conductor process allowance + minimum conductor width

^b Positional tolerance:



3.3 Process capability

The CQC shall be produced with one or more of the processes given in Table 3. The descriptions of the processes given in Table 3 identify the total processes used in the facility to produce printed board products. These processes include toolings and primary imagings (W), plating processes (X), coatings (Y) and testing (Z).

Not all processes need to be used on a single product CQC; however, to obtain process capability approval all processes claimed must be available for review.

Table 3 — Tooling and processes

Code indication	W Toolings and primary imagings			X Plating processes				Y Coatings			Z Testing
	Photo tooling	Electronic data	Image transfer	Initial plated holes	Conductive	Standard overplate	Precious overplate	Metallic	Permanent polymer	Organic	
1	Glass image reduction and manipulation (photographic)	CAD data acceptance (electrical)	Screen imaging	Electroless initial through-hole interconnection	Electrolytic copper plating	Tin-lead plating	Gold and gold on nickel (contact areas)	Solder (roller coated)	Dry film permanent polymer coating	Copper conservation coating flux	Electrical continuity tests
2	Film image reduction and manipulation (photographic)	CAD data and CAM (electrical)	Photo-imaging	Conductive coatings for initial through-hole interconnection	Semi-additive	Tin plating	Bond gold plating	Solder (hot levelled, air or oil)	Liquid permanent polymer coating (photodefined)	Conformal coating	Optical inspection
4	Photo tool generation (plotter)	Other image tool	Direct imaging	Other processes for initial through-hole interconnection	Electroless copper plating (additive)	Other standard platings	Other exotic platings	Other solder applications	Liquid permanent polymer coating (screened)	Other organic coatings	Other testing

The codification of the process capability shall be developed from Table 3. The process code is a series of significant letters (W, X, Y and Z, each corresponding to a group of processes), each followed by one, three or four figures representing the columns within the group of processes. According to Table 3 the figures are 1, 2 or 4. If the manufacturer uses none, two or three of the referred facilities within a column, the following figure shall be used:

0 = no capability approval for that particular process of W, X, Y or Z

1 = only 1

2 = only 2

3 = 1 and 2

4 = only 4

5 = 1 and 4

6 = 2 and 4

7 = 1, 2 and 4

Example: The code W416X2732Y150Z3 is used when a manufacturer has claimed the following facilities:

Tooling (W)	4 (first column):	Photo tool generation (plotter)
	1 (second column):	CAD data acceptance (electronic)
	6 (third column):	Photo imaging and direct imaging
Plating processes (X)	2 (first column):	Conductive coatings for initial through-hole interconnection
	7 (second column):	Electrolytic copper plating, electrolysis copper plating (additive) and semi-additive
	3 (third column):	Tin-lead plating and tin plating
	2 (fourth column):	Bond gold plating
Coatings (Y)	1 (first column):	Solder (roller coated)
	5 (second column):	Dry film permanent polymer coating and liquid permanent polymer coating (screened)
	0 (third column):	No capability approval for organic coatings
Testing (Z)	3 (first column):	Electrical continuity tests and optical inspection

4 Capability approval

4.1 Range of capability approval

Capability approval granted on testing one product combination within the limits specified in 5.7 of IEC 2326-1 and the following:

- base materials according to 3.1;
- the maximum product characteristics according to 3.2;
- processes used according to 3.3.

4.2 Qualified manufacturers list (QML) information

The QML information shall be given in accordance with 5.4 of IEC 2326-1 and shall contain the following details related to this Cap DS:

- reference to this Cap DS: 2326-4-1;
- description of features for which capability approval is granted:
 - identify the material in accordance with Table 1;
 - identify the product in accordance with Table 2;
 - identify the processes in accordance with Table 3.

For example: 2326-4-1B/M1A356B435C456D334E6W416X2732Y150Z3

Remark:

This code description is used by a computer system to establish a product type made by a manufacturer. The code facilitates using a) computer system(s) to categorize manufacturers, to help in sorting products listing by a specific product characteristic, or to provide ease of matching a users' product requirement with a manufacturers' capability. When this code is used in conjunction with a QPL or QML the manufacturer has the capability to make:

- (2326-4-1) — a rigid multilayer printed board with interlayer connections;
- (B) — of level B performance (covers both levels A and B);
- (M1) — this board is made of base materials according to IEC 1249-2-7 and IEC 1249-4-1.

The board has the following characteristics:

- (A356) maximum board size of 350 mm diagonal;
maximum total board thickness of 2,5 mm;
maximum number of conductive layers of 20;
- (B435) smallest diameter of as-drilled holes of 0,35 mm;
smallest total tolerance of drilled hole of 0,200 mm;
smallest location of hole (diameter from true position) of 0,25 mm;
- (C456) smallest electrical clearance (inner layer) of 0,200 mm;
smallest minimum conductor width (inner layer) of 0,125 mm;
smallest total required manufacturing allowance (inner layer) of 0,030 mm;
- (D334) smallest electrical clearance (outer layer) of 0,250 mm;
smallest minimum conductor width (outer layer) of 0,200 mm;
smallest total required manufacturing allowance (outer layer) of 0,050 mm;
- (E6) smallest location of features (diameter from true position) of 0,20 mm.

The toolings and processes available are:

- (W416) photo tool generation (plotter);
CAD data acceptance (electrical);
photo and direct imaging;
- (X2732) conductive coatings for initial through-hole interconnection;
electrolytic copper plating, electrolysis copper plating (additive) and semi-additive plating;
tin-lead and tin platings;
bond gold plating;

- (Y150) solder (roller coated);
dry film permanent polymer coating and liquid permanent polymer coating (screened);
- (Z3) electrical continuity tests and optical inspection.

5 Capability testing

5.1 Capability test programme

The capability test programme, the number of specimens to be tested shall be applied as specified in Table 4.

The test sequence is given in clause 6 of IEC 2326-4.

5.2 Characteristics

The characteristics given in Table 4 shall be tested. The test methods and conditions given there for the appropriate performance level shall be applied and the requirements given there shall be fulfilled. No defects are allowed.

Table 4 — Performance requirements for level A, B or C qualification

NOTE The letters GR are used to indicate that only the general requirements shall be met. For the explanation of the CTB see clause 6. For the explanation of the acronyms, see Annex A.

Test code	Characteristics	General requirements	Specific requirements for performance level			Assessment	
			A	B	C	Number of specimens to be tested	Test No. IEC 1189-3
V	VISUAL EXAMINATION						
V1	<i>Conformity</i>	Pattern, marking identification and material finishes shall comply with clause 6 when viewed without magnification. There shall be no apparent defects.	GR	GR	GR	2 TP or PP (before sub-division)	3V04
V2	<i>Appearance and workmanship</i>	The boards shall appear to have been processed in a careful and workmanlike manner, in accordance with good current practice.	GR	GR	GR	2 TP or PP (before sub-division)	3V01
V3	<i>Plated holes as received</i>	Plated holes shall be clean and free from inclusions of any sort that could affect component insertion and solderability when viewed without magnification.	GR	GR	GR	2 TP or PP (before sub-division)	3V04
		The number of holes with plating voids shall not exceed the specified percentage of the total number of plated holes when viewed without magnification.	5 %	2 %	0,1 %		
	<i>Holes showing plating voids</i>	The total area of the plating voids within a hole shall not exceed the specified percentage of the total area.	5 %	2 %	2 %		
		The largest dimension of voids shall not exceed the specified percentage of the hole circumference in the horizontal plane or the same percentage of the board thickness in the vertical plane.	15 %	10 %	5 %		
V4	<i>Plated holes after microsection</i>	Plated holes (levels B and C) shall be tested in as-received conditioning and after preconditioning according to test code Y4. Voids shall not coincide with internal or external copper layers. <i>Remarks</i> 1) All examinations at 100 × magnification. 2) Process control data may be used to supplement/minimize this test.	—	GR	GR	1 specimen A or B (CTB), 3 holes	3X09

Table 4 — Performance requirements for level A, B or C qualification

Test code	Characteristics	General requirements	Specific requirements for performance level			Assessment	
			A	B	C	Number of specimens to be tested	Test No. IEC 1189-3
V4.1	Resin smear at interface	Resin smear between the edge of the inner layer copper and the continuous plated copper shall not interrupt electrical continuity or exceed the specified percentage of inner layer copper thickness at the interface (see Figure 1 of IEC 2326-4).	≤ 30 %	≤ 15 %	None		
V4.2	Circumferential cracks of copper plating	There shall be no circumferential cracks of the copper, or circumferential separation of the copper from the wall in the plated hole (see Figure 2 of IEC 2326-4).	GR	GR	GR		
V4.3	Copper barrel to hole separation	There shall be no separation of plating from the hole wall exceeding the specified percentage of the hole circumference (see Figure 2 of IEC 2326-4). <i>Remark</i> Where necessary, this shall be verified by dimensional examination using test 3D01.	≤ 50 %	≤ 40 %	≤ 30 %		
V4.4	Foil cracking	There shall be no foil cracking.	GR	GR	GR		
V5	Conductors						
V5.1	External conductors	There shall be neither cracks nor breaks. Imperfections such as voids or edge defects are permissible provided that the conductor width or land area is not reduced by more than the specified percentage (see Figure 3 of IEC 2326-4). <i>Remarks</i> 1) Where necessary, this shall be verified by dimensional examination using test 3D01. 2) In the effective contact areas there shall be no imperfections. 3) For test specimens supplied with solderable temporary protective coating, the above requirement is not applicable. When specified the conductors shall be covered with a smooth and bright solder coating with no more than 5 % of scattered imperfections, such as pinholes, unwetted or dewetted areas. The imperfections shall not be concentrated on one area.	≤ 30 % (no occurrence > 10 mm)	≤ 20 % (no occurrence > 5 mm)	≤ 10 % (no occurrence > 3 mm)	2 TP or PP	3V02
			GR	GR	GR	2 specimens N (CTB)	3V02

Table 4 — Performance requirements for level A, B or C qualification

Test code	Characteristics	General requirements	Specific requirements for performance level			Assessment	
			A	B	C	Number of specimens to be tested	Test No. IEC 1189-3
V5.2	Internal conductors	There shall be neither cracks nor breaks. Imperfections such as voids or edge defects are permissible provided that the conductor width is not reduced by more than the specified percentage (see Figure 3 of IEC 2326-4). <i>Remarks</i> 1) Where necessary, this shall be verified by dimensional examination using test 3D01. 2) This examination shall be in-process.	≤ 30 % (no occurrence > 10 mm)	≤ 20 % (no occurrence > 5 mm)	≤ 10 % (no occurrence > 3 mm)	1 TP or PP (not laminated)	3V02
V6	Particles between conductors						
V6.1	External conductors	Residual metallic particles are permissible provided that the leakage path is not reduced by more than the specified percentage or to less than the distance required for the circuit voltages in isolated areas discounting conductor undercut, edge roughness, spikes, etc. (see Figure 3 of IEC 2326-4). <i>Remark</i> Where necessary, this shall be verified by dimensional examination using test 3D01.	≤ 30 %	≤ 30 %	≤ 20 %	2 TP or PP	3V02
V6.2	Internal conductors	Residual metallic particles are permissible provided that the leakage path is not reduced by more than the specified percentage or to less than the distance required for the circuit voltages in isolated areas discounting conductor undercut, edge roughness, spikes, etc. (see Figure 3 of IEC 2326-4). <i>Remarks</i> 1) Where necessary, this shall be verified by dimensional examination using test 3D01. 2) This examination shall be in-process.	≤ 30 %	≤ 20 %	≤ 10 %	1 TP or PP (not laminated)	3V02

Table 4 — Performance requirements for level A, B or C qualification

Test code	Characteristics	General requirements	Specific requirements for performance level			Assessment	
			A	B	C	Number of specimens to be tested	Test No. IEC 1189-3
V7	<i>Permanent polymer coating</i> (including solder resist)	The polymer coating according to IEC 1249-8-5 shall meet the requirements given below. Specimens D shall have clearances in the coating. Specimens G and N shall be covered completely. There shall be no apparent defects. <i>Remark</i> When necessary this shall be verified by dimensional examination using test 3D01.	GR	GR	GR	2 specimens D, G and N (CTB)	3V01
		When noted in the CDS that the polymer coating is used as an insulation all parts shall be completely covered.	GR	GR	GR		
		Imperfections, in the polymer coating on the base material, such as pinholes, small uncovered areas, scratches, etc. are permitted.	GR	GR	GR		
		Polymer coating used as solder resist shall cover the top surface of the conductor and shall be substantially free of pinholes. At least one or two adjacent conductor edges shall be covered.	GR	GR	GR		
		Board edges and the areas near slots, notches, etc. shall be free from polymer coating (as specified on the master drawing, when using a production board).	GR	GR	GR		
		All metallic areas intended for solder attachment, electrical contact, or indexing marker shall be free from polymer coating residues.	GR	GR	GR		3V02

Table 4 — Performance requirements for level A, B or C qualification

Test code	Characteristics	General requirements	Specific requirements for performance level			Assessment	
			A	B	C	Number of specimens to be tested	Test No. IEC 1189-3
D	DIMENSIONAL EXAMINATION						
D1	Board dimensions (external boundary)	Dimensions shall achieve the claimed sizes given in Table 2.	GR	GR	GR	2 TP or PP, at 3 places	3D04
D2	Board thickness in the zone of edge board contacts	Not applicable					
D3	Holes (see also D8)						
D3.1	Diameter	Diameters of tooling holes, mounting holes and component holes shall comply with Table 2 and clause 6. <i>Remark</i> A recommended range of hole sizes and tolerances are given in IEC 1188-6.	GR	GR	GR	2 TP or PP, 10 holes random selection at four comers and centre per TP or PP	3D04
D3.2	Plating thickness	The plating thickness shall be at least 20 µm. <i>Remark</i> Examinations at 400 × magnification.	GR	GR	GR	1 specimen A or B (CTB), 3 holes	3X09
D4	Slots, cut-outs and notches	Not applicable					
D5	Conductor width						
D5.1	External layer	The width shall achieve the claimed conductor tolerances given in Table 2. <i>Remark</i> To be measured together with V5.1	GR	GR	GR	2 specimens E (CTB)	3D01
D5.2	Internal layer	The width shall achieve the claimed conductor tolerances given in Table 2. <i>Remarks</i> 1) To be measured together with V5.2 2) This measurement shall be in-process.	GR	GR	GR	2 specimens H, layer 5 (CTB) (not laminated)	3D01
D6	Spacing between conductors						
D6.1	External layer	The spacing shall achieve the minimum electrical clearance given in Table 2. <i>Remark</i> To be measured together with V6.1.	GR	GR	GR	2 specimens E (CTB)	3D01

Table 4 — Performance requirements for level A, B or C qualification

Test code	Characteristics	General requirements	Specific requirements for performance level			Assessment	
			A	B	C	Number of specimens to be tested	Test No. IEC 1189-3
D6.2	Internal layer	The spacing shall achieve the minimum electrical clearance given in Table 2. <i>Remarks</i> 1) To be measured together with V6.2. 2) This measurement shall be in-process.	GR	GR	GR	2 specimens H, layer 5 (CTB) (not laminated)	3D01
D7	Alignment of hole and conductive pattern	There shall be no interruption of the conductive pattern and there shall be no hole break-out (land cut off) at the junction of the land and the conductor in excess of that specified below. This applies to both internal and external layers (see Figures 4, 5 and 6 of IEC 2326-4).				2 specimens A or B or D (CTB), 5 holes each side of the TP or PP	3D01
D7.1	External pattern alignment to plated holes	The requirements shall be as specified. Minimum annular width W_1 of external land at conductor junction (see Figure 4 of IEC 2326-4) Minimum annular width W_1 of external land at the other parts	There shall be no defects at conductive pattern and through-hole plating —	$W_1 \geq 0,03 \text{ mm}$ breakout $\theta \leq 90^\circ$ (see Figure 6)	$W_1 \geq 0,05 \text{ mm}$ $W_1 \geq 0,05 \text{ mm}$ (see Figure 4) No		
D7.2	External pattern alignment to plain holes	The requirements shall be as specified.	No breakout. No conductor junction reduction	No breakout. No conductor junction reduction	breakout. Minimum annular width 0,4 mm		
D7.3	Internal pattern alignment to plated holes	The requirements shall be as specified. <i>Remarks</i> 1) 100 × magnification. 2) Any other adequate method may be used. Minimum annular width W_2 of internal land at conductor junction (see Figure 5 of IEC 2326-4) Minimum annular width W_2 of internal land at the other parts	$W_2 \geq 0,03 \text{ mm}$ breakout $\theta \leq 180^\circ$ (see Figure 6)	$W_2 \geq 0,03 \text{ mm}$ breakout $\theta \leq 90^\circ$ (see Figure 6)	$W_2 \geq 0,05 \text{ mm}$ $W \geq 0 \text{ mm}$ (see Figure 5)	1 specimen A or B (CTB), 3 holes	3X09
D7.4	Landless holes	<i>Test under consideration</i>					

Table 4 — Performance requirements for level A, B or C qualification

Test code	Characteristics	General requirements	Specific requirements for performance level			Assessment	
			A	B	C	Number of specimens to be tested	Test No. IEC 1189-3
D8	<i>Positional accuracy</i>						
D8.1	Position of conductive pattern and holes relative to the position data	No continuity between hole 10 and hole 1, 2, 3, 4, or 5. <i>Remark</i> A standard continuity tester shall be used.	GR	GR	GR	2 specimens R (CTB)	3D04
D8.2	Positional tolerance of hole centres relative to the position data	<i>Not applicable</i>					
D9	<i>Permanent polymer coating</i> (including solder resist)						
D9.1	Dimensions	The dimensions of the polymer coating pattern shall comply with the overall dimensions of the specimens.	GR	GR	GR	2 specimens D, G and N (CTB), at 10 places	3D01
D9.2	Thickness of polymer coating	The thickness shall be as specified. <i>Remark</i> The thickness shall be measured at the centre of each conductor when using test 3X09 with 400 × magnification.	5 µm GR	25 µm GR	25 µm GR	2 specimens D, G and N (CTB), at 3 places 1 specimen D or N (CTB), at 3 places 2 TP or PP	3D04 or 3X09
D10	<i>Flatness</i>	The allowable bow and twist shall be not more than the specified value for printed boards with a diagonal of ≥ 100 mm.	1,5 % of the diagonal	1 % of the diagonal	0,5 % of the diagonal		3M04

Table 4 — Performance requirements for level A, B or C qualification

Test code	Characteristics	General requirements	Specific requirements for performance level			Assessment	
			A	B	C	Number of specimens to be tested	Test No. IEC 1189-3
S	SURFACE CONDITION TESTS						
S1	<i>Plating finishing</i>						
S1.1	Adhesion of plating, tape method	There shall be no evidence of plating adhering to tape after removal from the conductor. <i>Remark</i> Specimen N shall be tested prior to fusing.	GR	GR	GR	2 specimens N (CTB) (not covered with polymer coating)	3X01
	<i>or</i>						
	Adhesion of plating, burnish method	There shall be no evidence of blistering or detachment of the plating. <i>Remark</i> For contact finishes only.	GR	GR	GR	2 specimens N (CTB)	3X02
S1.2	Thickness of plating (contact area)	The thickness shall be: — for gold: $\geq 5 \mu\text{m}$; — for gold over nickel: gold $\geq 0,7 \mu\text{m}$, nickel $\geq 2,5 \mu\text{m}$.	—	GR	GR	2 specimens N (CTB)	3X06
S1.3	Thickness of plating (other than contact areas)	<i>Not applicable</i>					
S1.4	Porosity, gas exposure	<i>Not applicable</i>					
	Porosity, electrographic test	<i>Not applicable</i>					
S2	<i>Adhesion of permanent polymer coating, tape method</i>	The loss of adhesion shall not be more than the specified allowable percentage of testing area. <i>Remark</i> Applicable to permanent polymer coating only: — on bare copper; — on gold or nickel; — on base laminate; — on melting metals (tin-lead plating, fused tin-lead, etc.).	10 % 25 % 10 % 50 %	5 % 10 % 5 % 25 %	0 % 5 % 0 % 10 %	2 specimens G (CTB)	3X01
S3	<i>Solderability</i>	<i>Remark</i> When tested, the conductive surfaces of the board and the insides of the holes shall be properly wetted. When applied on production boards, only those holes having no connection with internal layers should be assessed to avoid “heat sink effect” affecting results interpretation.					

Table 4 — Performance requirements for level A, B or C qualification

Test code	Characteristics	General requirements	Specific requirements for performance level			Assessment	
			A	B	C	Number of specimens to be tested	Test No. IEC 1189-3
S3.1	When the use of a non-activated flux is agreed between customer and supplier	<i>Remarks</i> 1) Non-activated flux, as specified in IEC 68-2-20. 2) For both wetting and dewetting the holes shall comply with the well-soldered holes of Figure 7 of IEC 2326-4. 3) Accelerated ageing. Test Ca of IEC 68-2-3, 10 days.				2 specimens M and S (CTB)	3X07
		As-received condition Wetting: the specimen shall wet within 3 s. When temporarily protective coating intended to preserve the wettability is used, the specimen shall be wet within 4 s.	—	—	GR		
		Dewetting: the specimen shall remain in contact with the molten solder for 5 s to 6 s and shall not be dewetted.	—	—	GR		
		After accelerated ageing Wetting: the specimen shall be wet within 4 s. Dewetting: The specimen shall remain in contact with the molten solder for 5 s to 6 s and shall not be dewetted.	— —	— —	GR GR		
S3.2	When the use of an activated flux is agreed between purchaser and vendor	<i>Remarks</i> 1) Activated flux (0,2 %) as specified in IEC 68-2-20. 2) For both wetting and dewetting the holes shall comply with the well-soldered holes in Figure 7 of IEC 2326-4. 3) Accelerated ageing: test Ca of IEC 68-2-3, for 10 days.				2 specimens M and S (CTB)	3X07
		As-received condition and after accelerated ageing For boards with or without (solderable) temporary protective coating: Wetting: the specimen shall be wet within 3 s. Dewetting: the specimen shall remain in contact with the molten solder for 5 s to 6 s and shall not be dewetted.	GR GR	GR GR	— —		