

Printed boards —

Part 4: Rigid multilayer printed boards with interlayer connections — Sectional specification

The European Standard EN 62326-4:1997 has the status of a British Standard

ICS 31.180

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National foreword

This British Standard is the English language version of EN 62326-4:1997. It is identical with IEC 2326-4:1996.

This Part of BS EN 62326 forms the sectional specification in the IEC quality assessment system for electronic components (IECQ) for rigid multilayer printed boards with interlayer connections. In the IECQ system, this specification is numbered QC 230500.

The UK participation in its preparation was entrusted to Technical Committee EPL/52, Printed circuits, which has the responsibility to:

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- present to the responsible international/European committee any enquiries on the interpretation, or proposals for change, and keep the UK interests informed;
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Cross-references

Attention is drawn to the fact that Annex ZA lists normative references to international publications with their corresponding European publications. The British Standards which implement these international or European publications may be found in the BSI Standards Catalogue under the section entitled “International Standards Correspondence Index”, or using the “Find” facility of the BSI Standards Electronic Catalogue.

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Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, the EN title page, pages 2 to 32 and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

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Contents

	Page
National foreword	Inside front cover
Foreword	2
Text of EN 62326-4	3

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English version

Printed boards
Part 4: Rigid multilayer printed boards with interlayer
connections
Sectional specification

(IEC 2326-4:1996)

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(CEI 2326-4:1996)

Leiterplatten Teil 4: Starre
Mehrlagen-Leiterplatten mit
Durchverbindungen Rahmenspezifikation
(IEC 2326-4:1996)

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Comité Européen de Normalisation Electrotechnique
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Central Secretariat: rue de Stassart 35, B-1050 Brussels

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Foreword

The text of document 52/655/FDIS, future edition 1 of IEC 2326-4, prepared by IEC TC 52, Printed circuits, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 62326-4 on 1996-12-09.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 1997-09-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) —

This part 4 is to be used in conjunction with EN 62326-1:1997 and EN 62326-4-1:1997.

Annexes designated “normative” are part of the body of the standard.

Annexes designated “informative” are given for information only.

In this standard, Annex ZA is normative and Annex A, Annex B and Annex C are informative. Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 2326-4:1996 was approved by CENELEC as a European Standard without any modification.

Contents

	Page
Foreword	2
1 Scope	3
2 Normative references	3
3 General	3
4 Capability approval and maintenance of capability approval	4
5 Test specimens	4
6 Test sequence	5
7 Quality assessment	6
8 Customer Detail Specification (CDS) data	6
9 Characteristics of printed boards	6
10 Capability test programme	21
11 Quality conformance inspection	21
12 Test specimens	22
Annex A (informative) Acronyms related to IECQ and their explanations	27
Annex B (informative) Conversion table	28
Annex C (informative) Bibliography	31
Annex ZA (normative) Normative references to international publications with their corresponding European publications	32
Figure 1 — Resin smear at interface	22
Figure 2 — Circumferential defects	23
Figure 3 — Conductor pattern defects	23
Figure 4 — Minimum annular width (W_1) of external land	24
Figure 5 — Minimum annular width (W_2) of internal land	24
Figure 6 — Hole break-out	25
Figure 7 — Examples of soldered holes	26
Table 1 — Performance requirements	7

1 Scope

This part of IEC 2326 is applicable to rigid multilayer printed boards irrespective of their method of manufacture. It is the basis on which agreements between manufacturer and user are to be made.

This standard provides additional information necessary to supplement the requirements of the Generic Specification, IEC 2326-1, for the printed boards intended to be accepted under the IEC Quality Assessment System for Electronic Components (IECQ).

This standard establishes uniform requirements, specifies the characteristics to be assessed and the test methods to be used for quality conformance (whether by lot-by-lot inspection, process control, or periodic inspection).

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 2326. At the time of publication, the editions indicated were valid. All normative documents are subject to revision, and parties to agreements based on this part of IEC 2326 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 68-2-3:1969, *Environmental testing — Part 2: Tests — Test Ca: Damp heat, steady state*.

IEC 68-2-20:1979, *Environmental testing — Part 2: Tests — Test T: Soldering*.

IEC 68-2-38:1974, *Environmental testing — Part 2: Tests — Test Z/AD: Composite temperature/humidity cyclic tests*.

IEC/FDIS 1189-3, *Test methods for electrical materials, interconnections structures and assemblies — Part 3: Test methods for interconnection structures*¹⁾.

IEC 1249-5-1:1995, *Materials for interconnection structures — Part 5: Sectional specification set for conductive foils and films with and without coatings — Section 1: Copper foils (for the manufacture of copper-clad base materials)*.

IEC 2326-1:1995, *Printed boards — Part 1: Generic Specification*.

IEC 2326-4-1, *Printed boards — Part 4: Rigid multilayer printed boards with interlayer connections — Section 1: Capability detail specification: Performance levels A, B and C*.

QC 001002:1986, *Rules of Procedure of the IEC Quality Assessment System for Electronic Components (IECQ)*.

3 General

Unless otherwise specified all clauses and tables given in this standard are applicable to printed boards in compliance with the IECQ system. The procedure and requirements shall be in accordance with IEC 2326-1.

3.1 Printed boards fully compliant with the requirements for standard performance levels (level A, B, or C)

This Sectional Specification (SS) applies to rigid multilayer printed boards and is intended as a basis for the preparation of

- Capability Detail Specifications (Cap DS) applying to performance levels (i.e. level A, level B or level C), used in capability approval procedures. It is usually necessary to have a Cap DS describing all the performance levels. A Cap DS is prepared by the IEC.
- Customer Detail Specifications (CDS) for printed boards as required by 7.2 of IEC 2326-1. The CDS shall specify the selected performance level according to Table 1 of this standard. The CDS data shall be provided by the customer and allocated a number within his own system.

Printed boards materials for printed board fabrication may be any combination of base materials according to IEC 1249-2-7, or IEC 1249-2-11, or IEC 1249-2-9, with prepreg according to IEC 1249-4-1 and/or copper foil according to IEC 1249-5-1 and/or permanent polymer coating according to IEC 1249-8-5.

¹⁾ At present at the stage of Final Draft International Standard.

Table 1 contains the characteristics that are used in the performance requirements important for rigid multilayer printed boards with interlayer connections and makes reference to the appropriate tests to verify these characteristics. The CDS data shall specify characteristics and tests from this table.

Where additional details for a test have to be specified in the CDS data, an asterisk is shown in the relevant column. These details shall then be specified in accordance with IEC 1189-3.

Clause 6 prescribes the test sequence.

3.2 Printed boards with non-standard requirements (performance level X)

This Sectional Specification (SS) applies to rigid multilayer printed boards and is intended as a basis for the preparation of Customer Detail Specifications (CDS) for printed boards as required by 7.2 of IEC 2326-1.

The CDS shall be provided by the customer and he shall allocate a number within his own system.

The customer has the responsibility for establishing the requirements using Table 1 of this standard but in no case the performance level will be lower than performance level A. When another Risk Management Factor (RMF) is chosen the CDS data shall specify one of the more severe RMFs of Table 1 of IEC 2326-1.

Printed board materials used for printed board fabrication shall be specified in the CDS.

Where additional details for a test have to be specified in the CDS data, an asterisk is shown in the relevant column of Table 1. These details shall then be specified in accordance with IEC 1189-3.

Clause 6 prescribes the test sequence.

4 Capability approval and maintenance of capability approval

In order to be a participant in the IECQ system the printed board manufacturer shall obtain capability approval in accordance with clause 5 of IEC 2326-1.

4.1 Product capability

In order to obtain product capability approval the manufacturer shall complete the test requirements detailed in the Cap DS for which approval is sought. Approval to level A is limited only to performance level A. Approval to level B is limited to performance levels A and B. Approval to level C extends to three registered performance levels (levels A, B or C).

4.2 Process capability

For process capability 5.5.3 of IEC 2326-1 shall apply.

4.3 Maintenance of capability approval

The manufacturer shall maintain the status of approved capability by successful completion of quality conformance or equivalent inspections of the product defined by CDS data for the level of the original capability approval. In the event of failure to meet the requirements of the CDS data, remedial action shall be taken to correct the discrepancy.

To maintain capability approval, the manufacturing performance shall be verified as defined above and in 5.8 of IEC 2326-1.

5 Test specimens

5.1 Printed boards fully compliant with the requirements for standard performance levels (level A, B or C)

The specimens to be used as Capability Qualifying Component (CQC) shall be the Capability Test Board (CTB) or multiple arrangements of the CTB given in clause 6 of IEC 2326-4-1, or a Production Panel (PP) that has similar specimens available for testing. For the definitions of level A, B and C see 3.2 of IEC 2326-1

5.2 Printed boards with non-standard requirements (performance level X)

The specimens shall be production panels that have suitable patterns available for testing. If additional patterns are necessary, they shall be fully defined in the CDS data.

6 Test sequence

The tests shall be carried out in the test group sequence as given below. Unless otherwise stated, the sequence of tests within a particular test group is not relevant. The test codes used for indicating the tests are the same codes as used in Table 1.

Test group 1: In-process tests

- V5.2: Visual examination of internal conductors;
- V6.2: Visual examination of particles between internal conductors;
- D5.2: Dimensional examination of conductor widths on internal layers;
- D6.2: Dimensional examination of spacing between conductors on internal layers.

Test group 2: Visual and dimensional examinations (non-destructive)

- V1: Visual examination of conformity;
- V2: Visual examination of appearance and workmanship;
- V3: Visual examination of plated-through holes as received;
- V5.1: Visual examination of external conductors;
- V6.1: Visual examination of particles between external layers;
- V7: Visual examination of permanent polymer coatings;
- D1: Dimensional examination of board dimensions (external boundary);
- D2: Dimensional examination of board thickness in the zone of edge board contacts;
- D3.1: Dimensional examination of hole diameters;
- D4: Dimensional examination of slots, cut-outs and notches;
- D5.1: Dimensional examination of conductor widths on external layers;
- D6.1: Dimensional examination of spacings between conductors on external layers;
- D7.1: Dimensional examination of external plated-through holes;
- D7.2: Dimensional examination of external plain holes;
- D8: Dimensional examination of positional accuracy;
- D9: Dimensional examination of permanent polymer coatings (without microsection);
- D10: Dimensional examination of flatness.

Test group 3: Surface condition tests (non-destructive)

- S1.2: Thickness of plating (contact areas)
 - S1.4: Porosity
 - S1.1: Adhesion of plating, tape method
 - S1.3: Thickness of plating (other than contact areas);
 - S2: Adhesion of permanent polymer coating, tape method;
 - S4: Resistance to cleaning agents and flux.
- } specimen N sequence;

Test group 4: Electrical tests (non-destructive)

- E1: Electrical integrity;
- E2: Current proof, plated-through holes;
- E3: Voltage proof;
- E6: Characteristic impedance (if applicable).

Test group 5: Destructive tests

- V4: Visual examination of plated-through holes after microsection;
- D3.2: Dimensional examination of plating thickness (microsection);
- D7.3: Dimensional examination of internal plated-through holes (microsection);

- D9.3: Dimensional examination of thickness of polymer coating (microsection);
- S1.1: Adhesion of plating, burnish method;
- S3: Solderability;
- E4: Change in resistance of plated-through holes;
- E5: Insulation resistance;
- P1: Peel strength;
- P2: Pull-out strength of landless plated-through holes;
- Y1: Delamination, thermal shock;
- Y4: Plated-through holes after preconditioning.

7 Quality assessment

- The CDS shall contain complete information on quality evaluation for printed boards fully compliant with the requirements for standard performance levels. The CDS data shall specify the appropriate level of quality conformance inspection from Table 1 (performance level A, B or C).

For printed boards with non-standard requirements all required quality evaluation shall be performed in accordance with 7.2.6 of IEC 2326-1.

Unless otherwise specified production boards and/or specially designed test specimens may be used for carrying out tests for the lot inspection and the periodic inspection.

When specially designed test specimens are to be used, they shall be included in the panel. They may be based on the appropriate pattern of the CTB given in clause 6 of IEC 2326-4-1. Consultation between manufacturer and customer will usually be necessary.

8 Customers Detail Specification (CDS) data

The CDS data shall contain all information necessary to define the printed board clearly and completely. The recommendations given in IEC 1188-1 shall preferably be followed.

Care shall be taken to avoid unnecessary requirements. Permissible deviations shall be stated where necessary and nominal values without tolerances or simple maxima or minima shall be given where sufficient. Where precise tolerances are necessary for certain areas or parts of the printed board only, they shall be applied and restricted to those areas or parts.

If there are several possibilities of presentation, of tolerance classes, etc., the selections given in IEC 1188-6 shall preferably be applied.

In the case of discrepancy between the CDS data and any other pertinent specification (for example Basic Specification, Generic Specification or Sectional Specification), the CDS data shall prevail.

9 Characteristics of printed boards

Performance requirements of rigid multilayer printed boards with interlayer connections are given in Table 1. The performance levels and their relevant assessment criteria for quality conformance are shown (performance levels A, B and C). For printed boards with non-standard requirements (performance level X) all details shall be described in the CDS.

Table 1 — Performance requirements

NOTE The letters “GR” are used to indicate that only the general requirements shall be met. For the explanation of the acronyms, see Annex A.

Test code	Characteristics	General requirements	Specific requirements for performance level			Assessment			
			A	B	C	RMF (IEC 2326-1)	Test specimen (IEC 2326-4-1)	Test No. (IEC 1189-3)	Process control code (IEC 2326-1)
V	Visual examination								
V1	<i>Conformity</i>	Pattern, marking identification and material finishes shall comply with the CDS when viewed without magnification. There shall be no apparent defects.	As specified	—	—	6,5	Complete PB/DP	3V04	C4
			—	As specified	As specified	4,0			
V2	<i>Appearance and workmanship</i>	The boards shall appear to have been processed in a careful and workmanlike manner, in accordance with good current practice.	GR	—	—	6,5	Complete PB/DP	3V01	C4
			—	GR	GR	4,0			
V3	<i>Plated-through holes as received</i>	Plated-through holes shall be clean and free from inclusions of any sort that could affect component insertion and solderability when viewed without magnification.	GR	—	—	4,0	Complete PB	3V04	C4
			—	GR	GR	2,5			
			5 %	—	—	4,0			C2
			—	1 %	None	2,5			
	<i>Holes showing plating voids</i>	Total area of plating voids within a hole shall not exceed the specified percentage of the total area.	5 %	—	—	4,0			C2
			—	2 %	2 %	2,5			
		The largest dimension of voids shall not exceed the specified percentage of the hole circumference in the horizontal plane or the same percentage of the board thickness in the vertical plane.	15 %	—	—	4,0			C2
			—	10 %	5 %	2,5			
V4	<i>Plated-through holes after microsection</i>	Plated-through holes (levels B and C) shall be tested in as-received conditioning and after preconditioning according to test code Y4. Voids shall not coincide with internal or external copper layers. <i>Remarks</i> 1) All examinations at 100 × magnification 2) Process control data may be used to supplement/minimize this test.	—	GR	—	1,5	A or B (3 holes)	3X09	C1
			—	—	GR	1,0			

Table 1 — Performance requirements

Test code	Characteristics	General requirements	Specific requirements for performance level			Assessment			
			A	B	C	RMF (IEC 2326-1)	Test specimen (IEC 2326-4-1)	Test No. (IEC 1189-3)	Process control code (IEC 2326-1)
V4.1	Resin smear at interface	Resin smear between the edge of the inner layer copper and the continuous plating shall not interrupt electrical continuity or exceed the specified percentage of inner layer copper thickness at the interface (see Figure 1).	≤ 30 % — —	— ≤ 15 % —	— — None	2,5 1,5 1,0			C1
V4.2	Circumferential cracks of cooper plating	There shall be no circumferential cracks of the copper, or circumferential separation of the copper from the wall in the plated-through hole (see Figure 2).	GR — —	— GR —	— — GR	2,5 1,5 1,0			C1
V4.3	Copper barrel to hole separation	There shall be no separation of plating from the hole wall exceeding the specified percentage of the hole circumference (see Figure 2). <i>Remark</i> Where necessary, this shall be verified by dimensional examination using test 3D01.	≤ 50 % — —	— ≤ 40 % —	— — ≤ 30 %	2,5 1,5 1,0			C1
V4.4	Foil cracking	There shall be no foil cracking.	GR — —	— GR —	— — GR	2,5 1,5 1,0			C1
V5	<i>Conductors</i>								
V5.1	External conductors	There shall be neither cracks nor breaks. Imperfections such as voids or edge defects are permissible provided that the conductor width or land area is not reduced by more than the specified percentage (see Figure 3). <i>Remarks</i> 1) Where necessary, this shall be verified by dimensional examination using test 3D01. 2) In the effective contact areas there shall be no imperfections. 3) For test specimens supplied with solderable temporary protective coating the above requirement is not applicable.	≤ 30 % (no occurrence > 10 mm) —	— ≤ 20 % (no occurrence > 5 mm)	— ≤ 10 % (no occurrence > 3 mm)	4,0 2,5	Complete PB	3V02	C3