

# Semiconductor devices — Time Dependent Dielectric Breakdown (TDDB) test for gate dielectric films

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# National foreword

This British Standard is the UK implementation of EN 62374:2007. It is identical to IEC 62374:2007.

The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors.

A list of organizations represented on this committee can be obtained on request to its secretary.

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**Semiconductor devices -  
Time Dependent Dielectric Breakdown (TDDB) test  
for gate dielectric films  
(IEC 62374:2007)**

Dispositifs à semiconductors -  
Essai de rupture diélectrique  
en fonction du temps (TDDB)  
pour films diélectriques de grille  
(CEI 62374:2007)

Halbleiterbauelemente -  
Prüfung des zeitabhängigen  
dielektrischen Durchbruchs (TDDB)  
für dielektrische Gate-Schichten  
(IEC 62374:2007)

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### **Foreword**

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### **Endorsement notice**

The text of the International Standard IEC 62374:2007 was approved by CENELEC as a European Standard without any modification.

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## SEMICONDUCTOR DEVICES –

### TIME DEPENDENT DIELECTRIC BREAKDOWN (TDDB) TEST FOR GATE DIELECTRIC FILMS

## 1 Scope

This International Standard provides a test method of Time Dependent Dielectric Breakdown (TDDB) for gate dielectric films on semiconductor devices and a product lifetime estimation method of TDDB failure.

## 2 Terms and definitions

For the purposes of this document, the following terms and definitions apply:

### 2.1 oxide electric field (strength)

$E_{ox}$

defined as oxide voltage divided by oxide thickness.

NOTE

$$E_{ox} = V_{ox}/t_{ox} \quad (1)$$

where

$E_{ox}$  (MV/cm) is the oxide electric field;

$V_{ox}$  is the oxide voltage;

$t_{ox}$  is the oxide thickness.

$t_{ox}$  must be determined by a consistent, documented method (physical measurement method by Scanning Electron Microscope (SEM), Transmission Electron Microscope (TEM) or Capacitance-Voltage (CV) analysis). It is important to point out that the applied voltage is not necessarily the voltage across the oxide. Ultra-thin oxides exhibit quantum confinement effects and gate electrode depletion effects effectively reducing the voltage across the oxide. The method of determining  $t_{ox}$  or a reference to the documented standard must be included in the data report.

### 2.2 gate oxide leakage current

$I_g$

the leakage current flowing in the gate terminal of an insulated-gate field-effect transistor

NOTE The letter symbol " $I_g$ " is in common use for the gate leakage current.

### 2.3 initial gate oxide leakage current

$I_{g0}$

leakage current flowing in the gate terminal of an oxide insulated-gate when a use voltage is applied before stress voltage or stress electric field is applied

## 2.4 compliance current

$I_{\text{comp}}$   
maximum current of the voltage-forcing equipment

NOTE A compliance limit can be specified for a particular test.

## 2.5 measured gate oxide leakage current

$I_{\text{meas}}$   
gate leakage current measured in the pre-test or Constant Voltage Stress (CVS) test

## 2.6 stress-induced leakage oxide current

$I_{\text{SILC}}$   
stress-induced leakage current measured at  $V_{\text{SILC}}$

NOTE This value is measured and compared during the constant voltage test if the stress interruption method is used to detect breakdown.

## 2.7 use gate oxide leakage current

$I_{\text{use}}$   
typical measured current through the oxide at the normal use voltage

## 2.8 stress gate oxide leakage current

$I_{\text{stress}}$   
oxide gate current measured during the CVS test

## 2.9 previously measured gate oxide leakage current

$I_{\text{previous}}$   
previously measured oxide current in CVS test condition

## 2.10 breakdown time

$t_{\text{bd}}$   
summation of time at which stress voltage is applied to gate oxide until oxide failure

NOTE In the CVS test, the applied stress voltage is interrupted by measuring and judging repeatedly. (See Figure 1)

## 2.11 interval time

$t_{\text{int}}$   
time that stress is applied before the stress is interrupted and  $I_{\text{SILC}}$  is measured during the stress interruption technique for detecting breakdown

NOTE See Figure 3

## 2.12 gate oxide thickness

$t_{\text{ox}}$   
physical thickness of gate oxide

**2.13****wait time** $t_{\text{wait}}$ 

time before  $I_{\text{SILC}}$  is measured after a stress is interrupted during the stress interruption technique for detecting breakdown (see Figure 3)

**2.14****SILC voltage** $V_{\text{SILC}}$ 

voltage at which the stress-induced leakage current ( $I_{\text{SILC}}$ ) is measured

**2.15****stress voltage** $V_{\text{stress}}$ 

voltage applied during CVS test

**2.16****use voltage** $V_{\text{use}}$ 

voltage that is applied during the pre-test to determine device validity

NOTE This voltage is usually the power supply voltage or use voltage of the technology.

**3 Test equipment**

TDDDB test can be applied for both package level test and wafer level tests. A high temperature oven is used for the package level test. In the case of the wafer level tests, a wafer prober with a hot plate or a hot chuck is necessary. Additionally, measurement instruments are necessary that can detect failure criterion (that depends on  $t_{\text{ox}}$ , device structure and area).

**4 Test samples****4.1 General**

The test samples for TDDDB test should have the following test structure and area.

**4.2 Test structure: capacitor structure**

The test sample has a capacitor structure that consists of the gate dielectric film and gate electrode formed on a silicon substrate.

A capacitor or a field effect transistor (FET)-structure can be selected for the purpose of the test. The area and geometry can be varied.

FET-structures are preferred over capacitors, because stress should be performed in use mode, which is the inversion case. Multiple structures with variation in active area, isolation edge and gate edge perimeter are recommended in order to measure area scaling and to identify area vs. perimeter effects.

Test structure leads should be designed to minimize resistance to prevent voltage drops.