

BS EN 62386-102:2009



BSI Standards Publication

Digital addressable lighting interface —

Part 102: General requirements — Control gear

bsi.

...making excellence a habit.
AVA Documents™
Document Sharing Hub

National foreword

This British Standard is the UK implementation of EN 62386-102:2009. It is identical to IEC 62386-102:2009. Together with BS EN 62386-101:2009 and BS EN 62386-201:2009, it partially supersedes BS EN 60929:2006 which remains current.

The UK participation in its preparation was entrusted by Technical Committee CPL/34, Lamps and related equipment, to Subcommittee CPL/34/3, Auxiliaries for lamps.

A list of organizations represented on this committee can be obtained on request to its secretary.

This publication does not purport to include all the necessary provisions of a contract. Users are responsible for its correct application.

© BSI 2009

ISBN 978 0 580 57535 8

ICS 29.140.50; 29.140.99

Compliance with a British Standard cannot confer immunity from legal obligations.

This British Standard was published under the authority of the Standards Policy and Strategy Committee on 31 October 2009

Amendments issued since publication

Amd. No.	Date	Text affected
----------	------	---------------

EUROPEAN STANDARD
NORME EUROPÉENNE
EUROPÄISCHE NORM

EN 62386-102

August 2009

ICS 29.140.50; 29.140.99

Partially supersedes EN 60929:2006

English version

**Digital addressable lighting interface -
Part 102: General requirements -
Control gear
(IEC 62386-102:2009)**

Interface d'éclairage
adressable numérique -
Partie 102: Exigences générales -
Appareillages de commande
(CEI 62386-102:2009)

Digital adressierbare Schnittstelle
für die Beleuchtung -
Teil 102: Allgemeine Anforderungen -
Betriebsgeräte
(IEC 62386-102:2009)

This European Standard was approved by CENELEC on 2009-07-01. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Cyprus, the Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland and the United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: Avenue Marnix 17, B - 1000 Brussels

© 2009 CENELEC - All rights of exploitation in any form and by any means reserved worldwide for CENELEC members.

Ref. No. EN 62386-102:2009 E

 **Documents**
Document Sharing Hub

Foreword

The text of document 34C/874/FDIS, future edition 1 of IEC 62386-102, prepared by SC 34C, Auxiliaries for lamps, of IEC TC 34, Lamps and related equipment, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 62386-102 on 2009-07-01.

EN 62386-102:2009, together with EN 62386-101 and EN 62386-201, replaces Clause E.4, "Control by digital signals", and Annex G, "Test procedures for ballasts with digital control interface according to Clause E.4" of EN 60929:2006.

This Part 102 is intended to be used in conjunction with Part 101, which contains general requirements for the relevant product type (system), and with the appropriate part 2XX (particular requirements for control gear) containing clauses to supplement or modify the corresponding clauses in Parts 101 and 102 in order to provide the relevant requirements for each type of product.

The following dates were fixed:

- | | | |
|--|-------|------------|
| – latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement | (dop) | 2010-04-01 |
| – latest date by which the national standards conflicting with the EN have to be withdrawn | (dow) | 2012-07-01 |

Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 62386-102:2009 was approved by CENELEC as a European Standard without any modification.

In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 60598-1	NOTE	Harmonized as EN 60598-1:2008 (modified).
IEC 60669-2-1	NOTE	Harmonized as EN 60669-2-1:2004 (modified).
IEC 60921	NOTE	Harmonized as EN 60921:2004 (not modified).
IEC 60923	NOTE	Harmonized as EN 60923:2005 (not modified).
IEC 60925	NOTE	Harmonized as EN 60925:1991 (not modified).
IEC 61347-1	NOTE	Harmonized as EN 61347-1:2007 (modified).
IEC 61547	NOTE	Harmonized as EN 61547:2009 (not modified).
CISPR 15	NOTE	Harmonized as EN 55015:2006 (not modified).

Annex ZA (normative)

Normative references to international publications with their corresponding European publications

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 60929	2006	AC-supplied electronic ballasts for tubular fluorescent lamps - Performance requirements	EN 60929 + corr. December	2006 2006
IEC 61347-2-3	- ¹⁾	Lamp controlgear - Part 2-3: Particular requirements for a.c. supplied electronic ballasts for fluorescent lamps	EN 61347-2-3 + corr. July	2001 ²⁾ 2003
IEC 62386-101	2009	Digital addressable lighting interface - Part 101: General requirements - System	EN 62386-101	2009

¹⁾ Undated reference.

²⁾ Valid edition at date of issue.

CONTENTS

FOREWORD.....	7
INTRODUCTION.....	9
1 Scope.....	10
2 Normative references	10
3 Terms and definitions	10
4 General	12
5 Electrical specification.....	12
6 Interface power supply	12
7 Transmission protocol structure.....	12
7.1 General.....	12
7.2 Forward frame.....	12
7.2.1 Address byte 'YAAA AAAS'	12
7.2.2 Data byte 'XXXX XXXX'	13
7.3 Backward frame	13
8 Timing	13
8.1 Information bit timing.....	13
8.2 Forward frame timing	14
8.3 Backward frame timing	15
8.4 Frame sequence timing	15
9 Method of operation	16
9.1 Logarithmic dimming curve, arc power levels and accuracy.....	16
9.2 Power-on.....	19
9.3 Interface-failure	19
9.4 Min and max level	19
9.5 Fade time and fade rate	20
9.6 Reaction to commands during error state	20
9.7 Behaviour during lamp preheating and lamp ignition time	21
9.8 Memory access and memory map	21
9.8.1 Memory access commands.....	21
9.8.2 Memory map.....	21
10 Declaration of variables.....	24
11 Definition of commands	25
11.1 Arc power control commands.....	25
11.1.1 Direct arc power control command:.....	25
11.1.2 Indirect arc power control commands	26
11.2 Configuration commands:.....	28
11.2.1 General configuration commands:	28
11.2.2 Arc power parameters settings:	28
11.2.3 System parameters settings	30
11.3 Query commands	30
11.3.1 Queries related to status information	30
11.3.2 Queries related to arc power parameter settings.....	32
11.3.3 Queries related to system parameter settings	32
11.3.4 Application extended commands	33
11.4 Special Commands	33

11.4.1	Terminate special processes	33
11.4.2	Download information to the DTR	34
11.4.3	Addressing commands	34
11.4.4	Extended special commands	35
11.5	Summary of the command set	38
12	Test procedures	40
12.0	General	40
12.1	Test sequences 'Physical operational parameters'	44
12.1.1	Test sequences 'Waveform'	44
12.1.2	Test sequence 'Frame structure timing'	53
12.1.3	Insulation test	54
12.1.4	Optional test sequences	54
12.1.5	Test sequence 'Response time'	56
12.2	Test sequences 'Configuration commands'	57
12.2.1	Test sequences 'General configuration commands'	57
12.2.2	Test sequences 'Arc power parameter settings'	70
12.2.3	Test sequences 'System parameter settings'	80
12.2.4	Test sequences 'Memory Access'	84
12.3	Test sequences 'Arc power control commands'	88
12.3.1	Test sequences 'Timing'	88
12.3.2	Test sequences 'Dimming curve'	90
12.3.3	Test sequences 'Arc power commands'	95
12.4	Test sequence 'Physical address allocation'	105
12.5	Test sequences 'Random address allocation'	106
12.5.1	Test sequences 'INITIALISE / TERMINATE'	106
12.5.2	Test sequences 'RANDOMISE'	112
12.5.3	Test sequences 'COMPARE / WITHDRAW'	115
12.5.4	Test sequences 'PROGRAM / VERIFY / QUERY SHORT ADDRESS'	118
12.6	Test sequences 'Queries and reserved commands'	124
12.6.1	Test sequences 'Queries'	124
12.6.2	Test sequences 'Reserved commands'	131
Annex A (informative)	Examples of algorithms	136
Annex B (normative)	List of device types	138
Bibliography		139
Figure 1	– Bi-phase coded "1"	14
Figure 2	– Symbols for bi-phase levels: "1","0"	14
Figure 3	– Forward frame	14
Figure 4	– Forward frame timing	15
Figure 5	– Backward frame	15
Figure 6	– Backward frame timing	15
Figure 7	– Example of frame sequence timing	16
Figure 8	– Transition from forward to backward frames	16
Figure 9	– Transition from backward to forward and from forward to forward frames	16
Figure 10	– The logarithmic dimming curve with a minimum arc power of 0,1 %	17
Figure 11	– Configuration commands timing	28
Figure 12	– General test structure	40

Figure 13 – Activation state and test state	41
Figure 14 – Test sequence 'Current rating'	45
Figure 15 – Test sequence 'Voltage rating'	46
Figure 16 – Test sequence 'Back channel rise time / fall time'	47
Figure 17 – Test sequence 'Transmission rate'	48
Figure 18 – Test sequence 'Pulse width'	50
Figure 19 – 'Code violation'	51
Figure 20 – Waveforms for test 'Code violation':	52
Figure 21 – Test sequence 'Frame structure timing'	53
Figure 22 – Test sequence 'Polarity'	54
Figure 23 – Test sequence 'Overvoltage protection'	55
Figure 24 – Test sequence 'Response time'	56
Figure 25 – Test sequence 'RESET'	57
Figure 26 – Test sequence 'RESET: timeout / command in-between'	59
Figure 27 – Test sequence '100 ms-timeout'	60
Figure 28 – Test sequence 'Commands in-between'	62
Figure 29 – Test sequence 'QUERY VERSION NUMBER'	64
Figure 30 – Test sequence 'STORE ACTUAL LEVEL IN THE DTR'	65
Figure 31 – Test sequence 'Persistent memory'	66
Figure 32 – Test sequence 'DTR1'	68
Figure 33 – Test sequence 'DTR2'	69
Figure 34 – Test sequence 'STORE THE DTR AS MAX LEVEL'	70
Figure 35 – Test sequence 'STORE THE DTR AS MIN LEVEL'	71
Figure 36 – Test sequence 'STORE THE DTR AS SYSTEM FAILURE LEVEL'	73
Figure 37 – Test sequence 'STORE THE DTR AS POWER ON LEVEL'	75
Figure 38 – Test sequence 'STORE THE DTR AS FADE TIME'	77
Figure 39 – Test sequence 'STORE THE DTR AS FADE RATE'	78
Figure 40 – Test sequence 'STORE THE DTR AS SCENE' / 'GO TO SCENE'	79
Figure 41 – Test sequence 'REMOVE FROM SCENE'	80
Figure 42 – Test sequence 'ADD TO GROUP' / 'REMOVE FROM GROUP'	81
Figure 43 – Test sequence 'STORE THE DTR AS SHORT ADDRESS'	83
Figure 44 – Test sequence 'Memory Bank 0'	84
Figure 45 – Test sequence 'Memory Bank 1'	85
Figure 46 – Test sequence 'Other Memory Banks'	86
Figure 47 – Test sequence 'ENABLE WRITE MEMORY'	87
Figure 48 – Test sequence 'FADE TIME'	88
Figure 49 – Test sequence 'FADE RATE'	89
Figure 50 – Test sequence 'Logarithmic dimming curve'	90
Figure 51 – Test sequence 'Dimming curve: DIRECT ARC POWER CONTROL'	91
Figure 52 – Test sequence 'Dimming curve: UP / DOWN'	92
Figure 53 – Test sequence 'Dimming curve: STEP UP / STEP DOWN'	93
Figure 54 – Test sequence 'Dimming curve: DAPC SEQUENCE'	94
Figure 55 – Test sequence 'OFF'	95

Figure 56 – Test sequence 'DIRECT ARC POWER CONTROL'	96
Figure 57 – Test sequence 'UP'	97
Figure 58 – Test sequence 'DOWN'	98
Figure 59 – Test sequence 'STEP UP'	99
Figure 60 – Test sequence 'STEP DOWN'	100
Figure 61 – Test sequence 'RECALL MAX LEVEL'	101
Figure 62 – Test sequence 'RECALL MIN LEVEL'	102
Figure 63 – Test sequence 'ON AND STEP UP'	103
Figure 64 – Test sequence 'STEP DOWN AND OFF'	104
Figure 65 – Test sequence 'Physical address allocation'	105
Figure 66 – Test sequence 'INITIALISE: 15 minutes timer'	106
Figure 67 – Test sequence 'TERMINATE'	107
Figure 68 – Test sequence 'INITIALISE: short address'	108
Figure 69 – Test sequence 'INITIALISE: no short address'	109
Figure 70 – Test sequence 'INITIALISE: 100 ms timeout'	110
Figure 71 – Test sequence 'INITIALISE: command in-between'	111
Figure 72 – Test sequence 'RANDOMISE: reset values'	112
Figure 73 – Test sequence 'RANDOMISE: 100 ms timeout'	113
Figure 74 – Test sequence 'RANDOMISE: command in-between'	114
Figure 75 – Test sequence 'COMPARE'	115
Figure 76 – Test sequence 'WITHDRAW'	117
Figure 77 – Test sequence 'PROGRAM SHORT ADDRESS'	119
Figure 78 – Test sequence 'VERIFY SHORT ADDRESS'	120
Figure 79 – Test sequence 'QUERY SHORT ADDRESS'	122
Figure 80 – Test sequence 'SEARCH ADDRESS: reset value'	123
Figure 81 – Test sequence 'QUERY DEVICE TYPE'	124
Figure 82 – Test sequence 'QUERY LAMP FAILURE'	125
Figure 83 – Test sequence 'QUERY LAMP POWER ON'	126
Figure 84 – Test sequence 'QUERY LIMIT ERROR'	127
Figure 85 – Test sequence 'QUERY POWER FAILURE'	128
Figure 86 – Test sequence 'QUERY STATUS: control gear ok'	129
Figure 87 – Test sequence 'QUERY STATUS: fade running'	130
Figure 88 – Test sequence 'RESERVED: standard commands'	131
Figure 89 – Test sequence 'Application extended commands'	132
Figure 90 – Test sequence 'RESERVED: special commands 1'	133
Figure 91 – Test sequence 'RESERVED: special commands 2'	134
Figure 92 – Test sequence 'Not supported device types'	135
Table 1 – The logarithmic dimming curve with a minimum arc power of 0,1 %	18
Table 2 – Fade times and fade rates	20
Table 3 – Memory map of memory bank 0	22
Table 4 – Memory map of memory bank 1	23
Table 5 – Memory map of other memory banks	24

Table 6 – Declaration of variables	25
Table 7 – Summary of the command set	38
Table 8 – Timing combinations for test sequence 'Pulse width'	49
Table 9 – Parameters for test sequence 'RESET'	58
Table 10 – Parameters for test sequence '100 ms-timeout'	61
Table 11 – Parameters for test sequence 'Commands in-between'	63
Table 12 – Parameters for test sequence 'Persistent memory'	67
Table 13 – Parameters for test sequence 'DTR1'	68
Table 14 – Parameters for test sequence 'DTR2'	69
Table 15 – Parameters for test sequence 'STORE THE DTR AS MAX LEVEL'	70
Table 16 – Parameters for test sequence 'STORE THE DTR AS MIN LEVEL'	71
Table 17 – Parameters for test sequence 'STORE THE DTR AS SYSTEM FAILURE LEVEL'	72
Table 18 – Parameters for test sequence 'STORE THE DTR AS POWER ON LEVEL'	74
Table 19 – Parameters for test sequence 'STORE THE DTR AS FADE TIME'	76
Table 20 – Parameters for test sequence 'STORE THE DTR AS FADE TIME'	78
Table 21 – Parameters for test sequence 'STORE THE DTR AS FADE TIME'	79
Table 22 – Parameters for test sequence 'ADD TO GROUP' / 'REMOVE FROM GROUP'	81
Table 23 – Parameters for test sequence 'STORE THE DTR AS SHORT ADDRESS'	82
Table 24 – Parameters for test sequence 'ENABLE WRITE MEMORY'	87
Table 25 – Parameters for test sequence 'FADE TIME'	88
Table 26 – Parameters for test sequence 'FADE RATE'	89
Table 27 – Parameters for test sequence 'Logarithmic dimming curve'	90
Table 28 – Parameters for test sequence 'Dimming curve: DAPC SEQUENCE'	94
Table 29 – Parameters for test sequence 'DIRECT ARC POWER CONTROL'	96
Table 30 – Parameters for test sequence 'COMPARE'	115
Table 31 – Parameters for test sequence 'COMPARE'	116
Table 32 – Parameters for test sequence 'PROGRAM SHORT ADDRESS'	118
Table 33 – Parameters for test sequence 'QUERY SHORT ADDRESS'	121
Table 34 – Parameters for test sequence 'QUERY LIMIT ERROR'	127
Table 35 – Parameters for test sequence 'RESERVED: standard commands'	131
Table 36 – Parameters for test sequence 'RESERVED: special commands 1'	133
Table 37 – Parameters for test sequence 'RESERVED: special commands 2'	134
Table B.1 – List of device types	138

INTERNATIONAL ELECTROTECHNICAL COMMISSION

DIGITAL ADDRESSABLE LIGHTING INTERFACE –

Part 102: General requirements – Control gear

FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with an IEC Publication.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 62386-102 has been prepared by subcommittee 34C: Auxiliaries for lamps, of IEC technical committee 34: Lamps and related equipment.

This International Standard, together with IEC 62386-101 and IEC 62386-201, replaces Clause E.4, "Control by digital signals", and Annex G, "Test procedures for ballasts with digital control interface according to Clause E.4", of IEC 60929:2006.

The text of this standard is based on the following documents:

FDIS	Report on voting
34C/874/FDIS	34C/883/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

This Part 102 is intended to be used in conjunction with Part 101, which contains general requirements for the relevant product type (system), and with the appropriate part 2XX (particular requirements for control gear) containing clauses to supplement or modify the corresponding clauses in Parts 101 and 102 in order to provide the relevant requirements for each type of product.

A list of all parts of the IEC 62386 series, under the general title: *Digital addressable lighting interface*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC website under <http://webstore.iec.ch> in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

INTRODUCTION

This first edition of IEC 62386-102 is published in conjunction with IEC 62386-101 and with the various parts that make up the IEC 62386-200 series for control gear. A further number of parts covering control devices (to be published as the general requirements standard IEC 62386-103 and the various parts that make up the IEC 62386-300 series of particular requirements for control devices) is under consideration. The division of IEC 62386 into separately published parts provides for ease of future amendments and revisions. Additional requirements will be added as and when a need for them is recognized.

This International Standard, and the other parts that make up the IEC 62386-100 series, in referring to any of the clauses of IEC 62386-101 or IEC 62386-102, specify the extent to which such a clause is applicable and the order in which the tests are to be performed. The parts also include additional requirements, as necessary. All parts that make up IEC 62386-100 series are self-contained and therefore do not include references to each other.

Where the requirements of any of the clauses of IEC 62386-101 are referred to in this International Standard by the sentence "The requirements of IEC 62386-101, Clause "n" apply", this sentence is to be interpreted as meaning that all requirements of the clause in question of Part 101 apply, except any which are clearly inapplicable to the specific type of control gear.

The standardization of the control interface for control of electronic control gear by digital signals is intended to achieve interoperable multi-vendor operation between electronic control gear and lighting control devices, below the level of building management systems. All numbers used in this International Standard are decimal numbers unless otherwise noted. Hexadecimal numbers are given in the format 0xVV, where VV is the value. Binary numbers are given in the format XXXXXXXXb or in the format XXXX XXXX, where X is 0 or 1; "x" in binary numbers means "don't care".

DIGITAL ADDRESSABLE LIGHTING INTERFACE –

Part 102: General requirements – Control gear

1 Scope

This International Standard specifies a protocol and methods of test for the control by digital signals of electronic control gear for use on a.c. or d.c. supplies.

NOTE Tests in this standard are type tests. Requirements for testing individual control gear during production are not included.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60929:2006, *A.C.-supplied electronic ballasts for tubular fluorescent lamps – performance requirements*

IEC 61347-2-3, *Lamp control gear – Part 2-3: Particular requirements for a.c. supplied electronic ballasts for fluorescent lamps*

IEC 62386-101:2009, *Digital addressable lighting interface – Part 101: General requirements – System*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in Clause 3 of IEC 62386-101 and the following apply.

3.1

arc power

power supplied to the light sources (lamps), responsible for their output

3.2

arc power level

internal value representing the target arc power

3.3

forward frame

sequence of bits used to transmit data from a master to a slave

3.4

short address

kind of address used to address an individual control gear in the system

3.5

group address

kind of address used to address a group of control gear in the system at once



3.6

broadcast

kind of address used to address all control gear in the system at once

3.7

command

sequence of bits causing any reaction in the receiver

3.8

backward frame

sequence of bits used to transmit data from a slave to a master

3.9

frame sequence

group of consecutive frames

3.10

fade time

time taken for the light output to change from the actual dim level to the target dim level specified by the received command

3.11

fade rate

speed of change the light output

3.12

search address

24 bit number used to identify an individual control gear in the system during initialization

3.13

random address

24 bit address generated by the control gear during initialization

3.14

scene

preset light output level that can be configured

3.15

DTR (Data transfer register)

multipurpose registers used to transmit data from a control device to the control gear and vice versa

3.16

response time

actual time taken for a control gear to change its output without fading

3.17

reset state

state in which all configurable parameters of the control gear, as shown in Table 6 (including the actual level) have reset values

3.18

global trade item number – GTIN

number used for the unique identification of trade items worldwide

NOTE The key is comprised of a GS1 or U.P.C. company prefix followed by an item reference number and a check digit. It is described in the “GS1 General Specifications”, Version 7.0, published by the GS1, Avenue Louise 326; BE-1050 Brussels; Belgium; and GS1, 1009 Lenox Drive, Suite 202, Lawrenceville, New Jersey, 08648, U.S.A.

3.19

data byte

second byte of a forward frame

4 General

The requirements of 4.1 and 4.2 of IEC 62386-101 shall apply.

5 Electrical specification

The requirements of Clause 5 of IEC 62386-101 shall apply.

6 Interface power supply

The requirements of Clause 6 of IEC 62386-101 shall apply, if a power supply is integrated with the control gear.

7 Transmission protocol structure

7.1 General

A forward frame as well as a backward frame shall be analysed in the receiver. In case of code violation, the frame shall be ignored. 1,7 ms after the occurrence of a code violation, the control gear shall be ready again for a frame reception.

7.2 Forward frame

A forward frame shall consist of 19 bits, as shown in 8.2:

- 1 start bit: (logical '1', bi-phase code)
- 1 address byte 'YAAA AAAS': (bi-phase code)
- 1 data byte 'XXXX XXXX': (bi-phase code)
- 2 stop bits: (idle line)

7.2.1 Address byte 'YAAA AAAS'

The first byte of a forward frame is called the 'address byte'. Every control gear shall be able to react to a short address, 16 group addresses and broadcast. The following addressing scheme shall be used:

Type of addresses:		address byte:
64	short addresses	0 – 63 0AAA AAAS
16	group addresses	0 – 15 100A AAAS
	broadcast	1111 111S
	special commands	1010 0000 to 1111 1101
Y: short- or group address/broadcast:		Y = "0": short address Y = "1": group address or broadcast
A: significant address bit		
S: selector bit:		S = "0": data byte = direct arc power level S = "1": data byte = command

When the address byte contains a short address, group address or broadcast address, the least significant bit (S) is known as the "selector bit". It is used to indicate whether a direct arc power level or a command follows in the data byte.

Special commands, requirements for which are given in 11.4, shall use CCCC CCCC transmitted in the address byte for selecting the command.

7.2.2 Data byte 'XXXX XXXX'

The least significant bit of the address byte in case of a short address, group address or broadcast (selector bit 'S') shall indicate whether the data byte contains a direct arc power level or a command:

S = "0": data byte = direct arc power level (see 11.1.1)

S = "1": data byte = command (see 11.1.2 and the subsequent subclauses)

In the case of special commands the content of the data byte shall be defined with the relevant commands, as given in 11.4.

7.3 Backward frame

A backward frame shall be sent only after the reception of a query command or a write memory command.

A backward frame shall consist of 11 bits, as shown in 8.3:

- 1 start bit: (logical '1', bi-phase code)
- 1 data byte 'XXXX XXXX': (bi-phase code)
- 2 stop bits: (idle line)

Depending on the command the backward frame (= answer) shall be either a 'Yes' / 'No' or 8-bit information:

'Yes': 1111 1111

'No': The control gear shall not react (idle line)

8-bit information: XXXX XXXX

8 Timing

8.1 Information bit timing

The start bit and the information bits shall be bi-phase encoded.

The information rate shall be 1 200 bit/s.

$$T_e = \frac{1}{2 \cdot 1200} \text{ s} = 416.67 \mu\text{s}$$

The timing for a logical "1" shall be as shown in Figure 1.

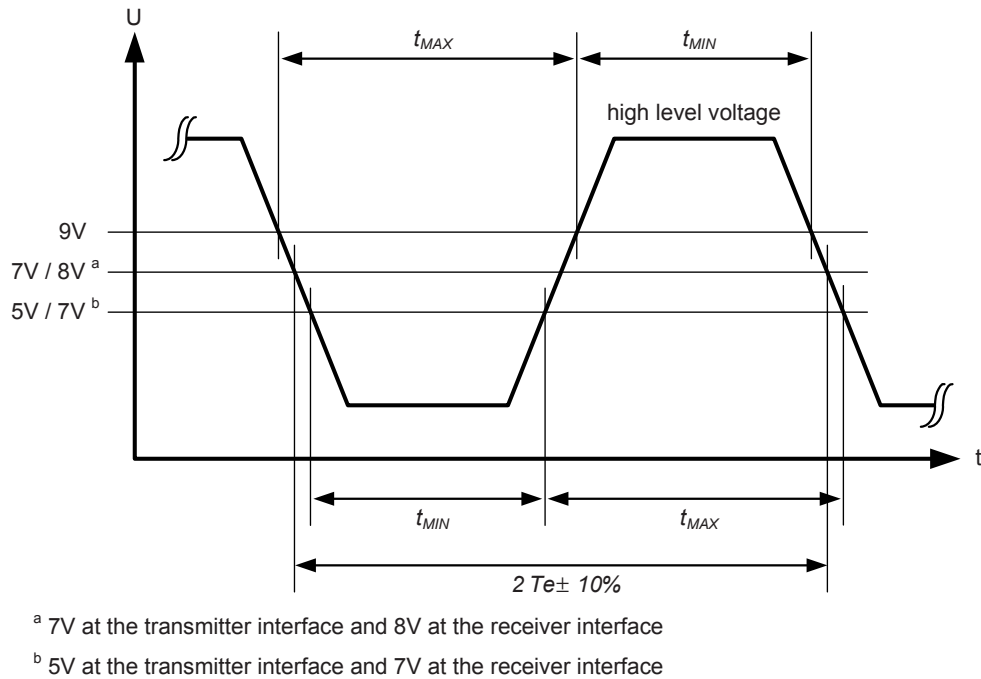


Figure 1 – Bi-phase coded "1"

The limits for the times t_{MAX} and t_{MIN} shall be:

$$t_{MAX} < 500 \mu s \text{ and } t_{MIN} > 334 \mu s$$

Symbols for the bi-phase levels "0" and "1" shall be as shown in Figure 2.



Figure 2 – Symbols for bi-phase levels: "1", "0"

8.2 Forward frame timing

A forward frame shall consist of 19 bits lasting 38 times T_e , as shown in Figure 3 and Figure 4.

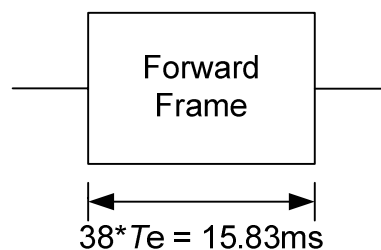


Figure 3 – Forward frame

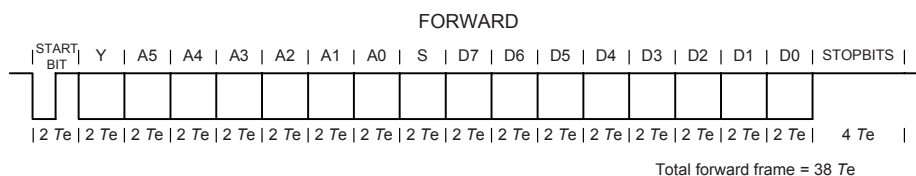


Figure 4 – Forward frame timing

8.3 Backward frame timing

A backward frame shall consist of 11 bits lasting 22 times T_e , as shown in Figures 5 and 6.

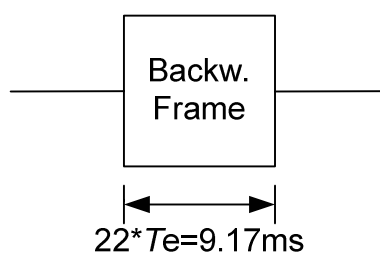


Figure 5 – Backward frame

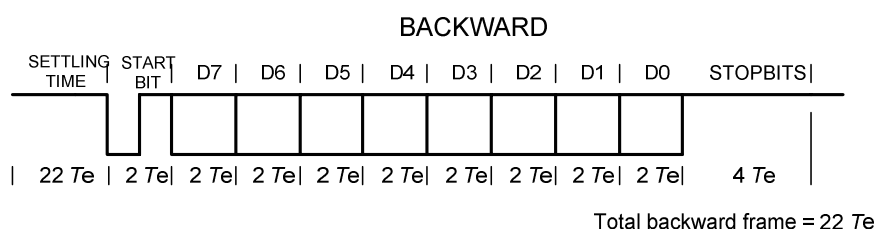


Figure 6 – Backward frame timing

8.4 Frame sequence timing

The transmission timing requirements shall be as shown in Figures 7, 8 and 9.

With the time between two consecutive frames defined as the time between the end of the last stop bit and the beginning of the start bit of the following frame:

- the time between two consecutive forward frames shall be at least 22 T_e ;
- the time between forward and backward frames shall be 7 T_e – 22 T_e ;
- the time between backward and forward frames shall be at least 22 T_e .

With the settling time defined as time between the last rising edge of a frame and the first falling edge of the following frame:

- the settling time between two consecutive forward frames shall be at least 27 T_e ;
- the settling time between forward and backward frames shall be 11 T_e – 27 T_e ;
- the settling time between backward and forward frames shall be at least 27 T_e .

The lighting control device shall wait up to 27 T_e + 10 % for an answer, timed from the last rising edge of the forward message. If no backward frame has been started by this time, this shall be interpreted as the answer "No".

NOTE 1 Answers to broadcast or group addressed queries can overlap and might result in a corrupted backward frame.

In certain cases, the command repetition time shall be 100 ms (2 forward frames within 100 ms).

NOTE 2 This is explicitly mentioned in the definitions of the relevant commands.

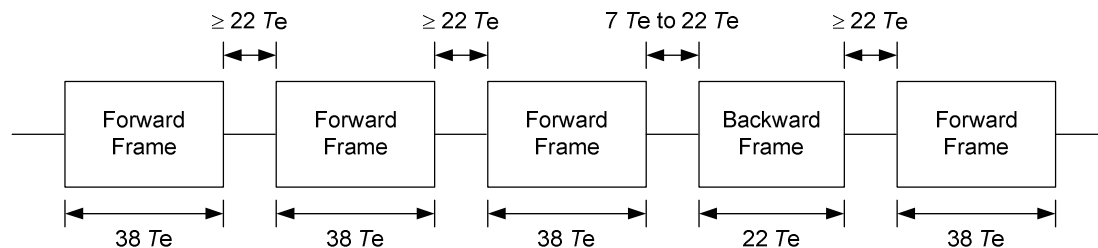


Figure 7 – Example of frame sequence timing

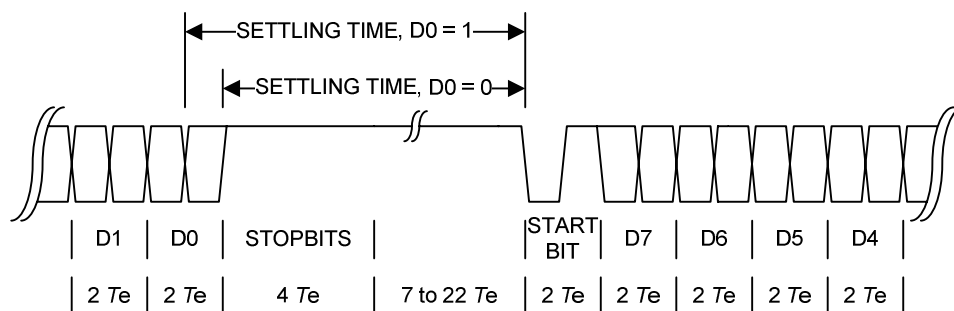


Figure 8 – Transition from forward to backward frames

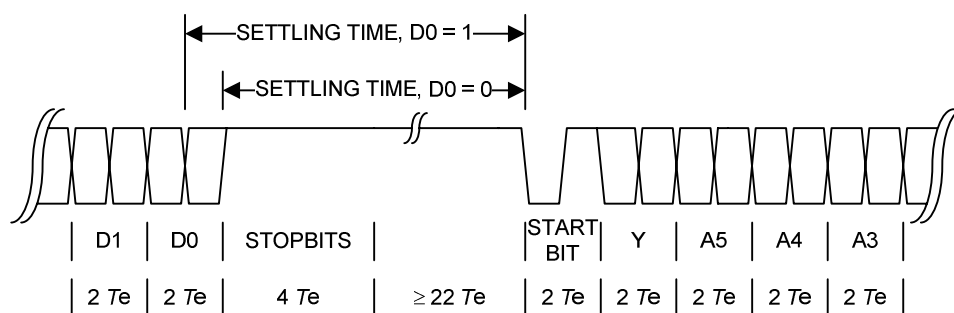


Figure 9 – Transition from backward to forward and from forward to forward frames

9 Method of operation

9.1 Logarithmic dimming curve, arc power levels and accuracy

The lowest arc power of control gear is 0,1 % and shall be coupled to the arc power level 1, as shown in Figure 10 and Table 1. The highest arc power of control gear (100 %) shall be coupled to the arc power level 254, as shown in Figure 10 and Table 1.

A logarithmic dimming curve from 0,1 % to 100 % shall be defined according to the formula:

$$X(n) = 10^{\frac{n-1}{253/3} - 1} \quad \left| \frac{X(n) - X(n+1)}{X(n)} \right| = \text{constant} = 2.8 \%$$

Figure 10 shows the graphical representation. Table 1 shows the calculated values.

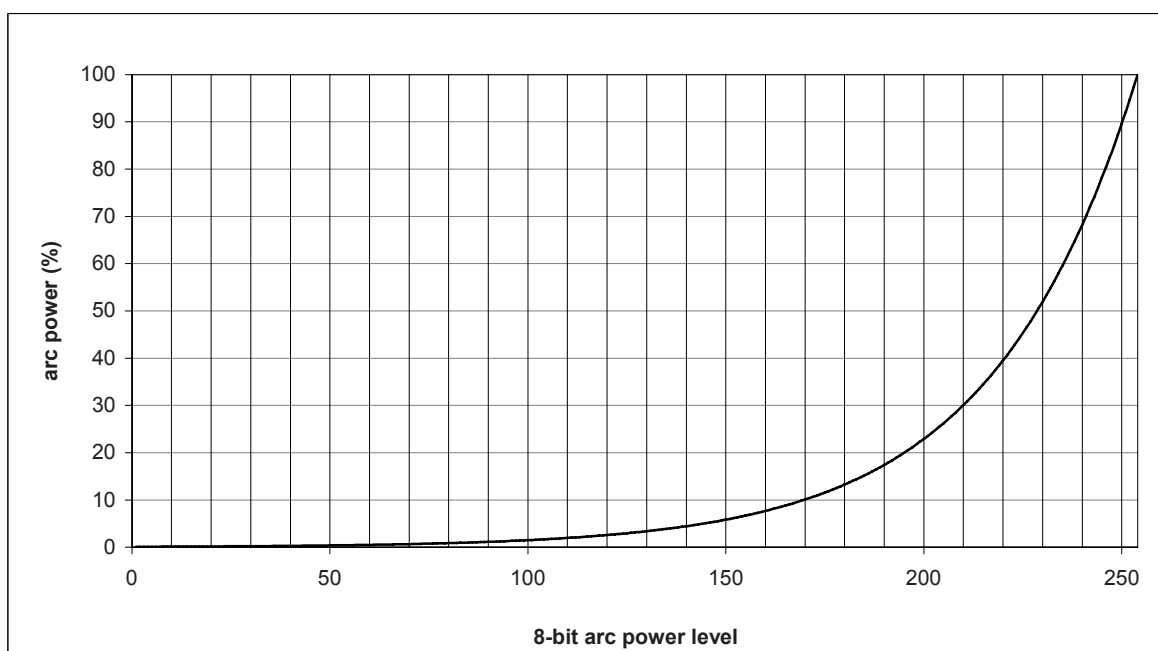


Figure 10 – The logarithmic dimming curve with a minimum arc power of 0,1 %

The relative accuracy of the dimming curve shall be $\pm 1/2$ steps, monotonically.

NOTE The absolute accuracy of the arc power should be specified by the control gear manufacturer.

Table 1 – The logarithmic dimming curve with a minimum arc power of 0,1 %

n	X	n	X	n	X	n	X	n	X
1	0,100	52	0,402	103	1,620	154	6,520	205	26,241
2	0,103	53	0,414	104	1,665	155	6,700	206	26,967
3	0,106	54	0,425	105	1,711	156	6,886	207	27,713
4	0,109	55	0,437	106	1,758	157	7,076	208	28,480
5	0,112	56	0,449	107	1,807	158	7,272	209	29,269
6	0,115	57	0,461	108	1,857	159	7,473	210	30,079
7	0,118	58	0,474	109	1,908	160	7,680	211	30,911
8	0,121	59	0,487	110	1,961	161	7,893	212	31,767
9	0,124	60	0,501	111	2,015	162	8,111	213	32,646
10	0,128	61	0,515	112	2,071	163	8,336	214	33,550
11	0,131	62	0,529	113	2,128	164	8,567	215	34,479
12	0,135	63	0,543	114	2,187	165	8,804	216	35,433
13	0,139	64	0,559	115	2,248	166	9,047	217	36,414
14	0,143	65	0,574	116	2,310	167	9,298	218	37,422
15	0,147	66	0,590	117	2,374	168	9,555	219	38,457
16	0,151	67	0,606	118	2,440	169	9,820	220	39,522
17	0,155	68	0,623	119	2,507	170	10,091	221	40,616
18	0,159	69	0,640	120	2,577	171	10,371	222	41,740
19	0,163	70	0,658	121	2,648	172	10,658	223	42,895
20	0,168	71	0,676	122	2,721	173	10,953	224	44,083
21	0,173	72	0,695	123	2,797	174	11,256	225	45,303
22	0,177	73	0,714	124	2,874	175	11,568	226	46,557
23	0,182	74	0,734	125	2,954	176	11,888	227	47,846
24	0,187	75	0,754	126	3,035	177	12,217	228	49,170
25	0,193	76	0,775	127	3,119	178	12,555	229	50,531
26	0,198	77	0,796	128	3,206	179	12,902	230	51,930
27	0,203	78	0,819	129	3,294	180	13,260	231	53,367
28	0,209	79	0,841	130	3,386	181	13,627	232	54,844
29	0,215	80	0,864	131	3,479	182	14,004	233	56,362
30	0,221	81	0,888	132	3,576	183	14,391	234	57,922
31	0,227	82	0,913	133	3,675	184	14,790	235	59,526
32	0,233	83	0,938	134	3,776	185	15,199	236	61,173
33	0,240	84	0,964	135	3,881	186	15,620	237	62,866
34	0,246	85	0,991	136	3,988	187	16,052	238	64,607
35	0,253	86	1,018	137	4,099	188	16,496	239	66,395
36	0,260	87	1,047	138	4,212	189	16,953	240	68,233
37	0,267	88	1,076	139	4,329	190	17,422	241	70,121
38	0,275	89	1,105	140	4,449	191	17,905	242	72,062
39	0,282	90	1,136	141	4,572	192	18,400	243	74,057
40	0,290	91	1,167	142	4,698	193	18,909	244	76,107
41	0,298	92	1,200	143	4,828	194	19,433	245	78,213

Table 1 (continued)

n	X	n	X	n	X	n	X	n	X
42	0,306	93	1,233	144	4,962	195	19,971	246	80,378
43	0,315	94	1,267	145	5,099	196	20,524	247	82,603
44	0,324	95	1,302	146	5,240	197	21,092	248	84,889
45	0,332	96	1,338	147	5,385	198	21,675	249	87,239
46	0,342	97	1,375	148	5,535	199	22,275	250	89,654
47	0,351	98	1,413	149	5,688	200	22,892	251	92,135
48	0,361	99	1,452	150	5,845	201	23,526	252	94,686
49	0,371	100	1,492	151	6,007	202	24,177	253	97,307
50	0,381	101	1,534	152	6,173	203	24,846	254	100,000
51	0,392	102	1,576	153	6,344	204	25,534		

9.2 Power-on

Control gear shall start to react properly to commands no later than 0,5 s after power-on. If no command affecting power level is received before 0,6 s after mains power-on, the control gear shall go to POWER-ON LEVEL immediately without fading.

If 'MASK' is stored as the POWER-ON LEVEL, the control gear shall go to the most recent arc power level.

There shall therefore be an interval of at least 0,1 s during which a control device can send an arc power control command which will be obeyed immediately, thereby preventing the gear from going automatically to POWER-ON LEVEL.

After receiving the first valid forward frame on the interface after power-on, the control gear shall not respond in any way to any control method other than that described in IEC 62386.

NOTE 1 Different manufacturers' control gear may react in different ways to relative arc power commands (such as STEP DOWN) during the 0,1 s period mentioned above.

NOTE 2 Some control gear may have a preheating or ignition phase (see 9.7).

NOTE 3 Different manufacturers' control gear may restore either the most recent actual arc power level or the most recent target arc power level if 'MASK' is stored as POWER-ON LEVEL.

9.3 Interface-failure

If the interface idle voltage remains below the specified receiver high level range (see IEC 62386-101:2009, Clause 5.) for more than 500 ms, the control gear shall check the content of the "SYSTEM FAILURE LEVEL" variable.

If "MASK" is stored, the control gear shall stay in the state it is in (no change of the arc power level, no switching on or off). If any other value is stored, the control gear shall go to this arc power level immediately without fading. On restoration of the idle voltage the control gear shall not change its state.

9.4 Min and max level

Programming a MIN LEVEL above or a MAX LEVEL below the actual arc power level shall set the actual arc power level to the new MIN LEVEL or MAX LEVEL immediately without fading. Programming a MIN LEVEL below or a MAX LEVEL above the actual arc power level shall not affect the actual arc power level.

Arc power levels stored in the control gear shall not be restricted by the MIN and MAX LEVEL settings. Nevertheless, those levels shall cause the control gear to operate at MIN LEVEL or MAX LEVEL if the stored value is below the MIN LEVEL or above the MAX LEVEL.

The arc power levels "0" (OFF) and "255" (MASK) shall not be affected by the MIN and MAX LEVEL settings.

9.5 Fade time and fade rate

The fade times and fade rates shall be as given in Table 2.

Table 2 – Fade times and fade rates

X	FADE TIME s	FADE RATE steps/s
0	No fade	Not applicable
1	0,7	358
2	1,0	253
3	1,4	179
4	2,0	127
5	2,8	89,4
6	4,0	63,3
7	5,7	44,7
8	8,0	31,6
9	11,3	22,4
10	16,0	15,8
11	22,6	11,2
12	32,0	7,9
13	45,3	5,6
14	64,0	4,0
15	90,5	2,8

Arc power control commands received during a running fading process shall stop the fading process and shall be executed immediately.

If a burning lamp is to be switched off, the step from "MIN LEVEL" to "OFF" shall be taken into consideration for the calculation of the fade time.

If a lamp is to be lit and dimmed to a certain value, the step from "OFF" to "MIN LEVEL" shall not be taken into consideration for the calculation of the fade time.

To achieve uniform behaviour, the control device shall take into consideration the differences in ignition time (strike time delay) of various types of control gear.

If a command causes a control gear to fade as fast as possible to a new level, but before that level is reached, a new command also affecting the level is received, the eventual output level shall be exactly the same as if the first command had been processed instantaneously.

NOTE All changes to the actual level refer to arc power level but the arc power may change more slowly.

9.6 Reaction to commands during error state

If the control gear is in an error state where operation of the lamp(s) is not possible (e.g. lamp failure) it shall react to arc power commands in the following way:

The control gear shall calculate “virtual” arc power levels in accordance with the appropriate fading definition, and it shall establish the actual “virtual” level when the failure is repaired (lamp operation is possible).

9.7 Behaviour during lamp preheating and lamp ignition time

Lamp preheating and lamp ignition time specify the transition time from “lamp(s) = off” to “lamp(s) = on”. During this time the status of the arc power indicated by bit 2 of the status information of command 144 shall be “off”. During preheating, fading processes are frozen at the minimum arc power level and the reaction to arc power commands shall be the same as if the lamp(s) were operating at “MIN LEVEL”.

9.8 Memory access and memory map

9.8.1 Memory access commands

There is freely accessible persistent memory defined for identification of the control gear in a system. Part of this memory is read-only and programmed by the manufacturer of the control gear. Memory access commands are used to read and write the content of this memory.

The total memory space is organized in memory banks of maximum 256 bytes. A maximum of 256 banks can be addressed.

The bank is selected by the content of DTR1. The address of the memory location inside the selected bank is given by the content of DTR.

Memory is read by means of command 197 “READ MEMORY LOCATION”.

Memory is written by means of command 275 “WRITE MEMORY LOCATION”. Before writing, the control gear shall be set into write enable state by means of command 129 “ENABLE WRITE MEMORY”. Some of the memory locations are read-only or lockable for writing.

The byte in location 0x00 of each bank contains the address of the last accessible memory location of the bank.

The byte in location 0x01 of each bank contains a checksum of the memory bank. The checksum shall be calculated by the formula

$$CS = (0 - \text{memory}[0x02] - \text{memory}[0x03] - \dots - \text{memory}[\text{memory}[0x00]]) \text{ modulo } 256$$

The checksum shall be calculated by the control gear.

The byte in location 0x02 of memory bank 0 contains the number of the highest accessible memory bank.

Memory bank 0 shall be implemented as described in 9.8.2.1, with further memory banks implemented, where necessary, as described in 9.8.2.1. to 9.8.2.3.

9.8.2 Memory map

9.8.2.1 Memory bank 0

Memory bank 0 contains information about the control gear and shall be implemented as shown in Table 3, with at least the memory locations up to address 0x0E.

Memory bank 0 shall not be affected by command 32 “RESET”.

Table 3 – Memory map of memory bank 0

Address	Description	Default value ^a	Memory access
0x00	address of last accessible memory location	factory burn in	read-only
0x01	checksum of memory bank 0	factory burn in	read-only
0x02	number of last accessible memory bank	factory burn in	read-only
0x03	GTIN byte 0 (MSB)	factory burn in	read-only
0x04	GTIN byte 1	factory burn in	read-only
0x05	GTIN byte 2	factory burn in	read-only
0x06	GTIN byte 3	factory burn in	read-only
0x07	GTIN byte 4	factory burn in	read-only
0x08	GTIN byte 5	factory burn in	read-only
0x09	control gear firmware version (major)	factory burn in	read-only
0x0A	control gear firmware version (minor)	factory burn in	read-only
0x0B	serial number byte 1 (MSB)	factory burn in	read-only
0x0C	serial number byte 2	factory burn in	read-only
0x0D	serial number byte 3	factory burn in	read-only
0x0E	serial number byte 4	factory burn in	read-only
≥ 0x0F	additional control gear information ^b	^b	^b
^a = control gear leaves the factory ^b = purpose, default value and memory access of these memory locations shall be defined by the control gear manufacturer.			
The bytes in locations 0x03 to 0x08 ("GTIN 0" to "GTIN 5") contain the Global Trade Item Number (GTIN), e.g. the EAN, in binary. The bytes shall be stored most significant first and filled with leading zeroes. The bytes in location 0x09 and 0x0A ("firmware version") contain the firmware version of the control gear. The bytes in locations 0x0B to 0x0E ("serial number byte 1" to "serial number byte 4") contain the unique serial number of the control gear. Memory bank 0 shall not be affected by command 32 "RESET". NOTE If the serial number consists of more than 4 byte additional memory locations may be used starting at address 0x0F.			

9.8.2.2 Memory bank 1

Memory bank 1 can be used by the OEM (original equipment manufacturer, e.g. luminaire manufacturer) to store additional information and shall be implemented (if memory bank 1 is accessible) as shown in Table 4, with at least the memory locations up to address 0x0F.

Table 4 – Memory map of memory bank 1

Address	Description	Default value ^a	Memory access
0x00	address of last accessible memory location	factory burn in	read-only
0x01	checksum of memory bank 1	^b	read-only
0x02	memory bank 1 lock byte (read-only if not 0x55)	0xFF	read / write
0x03	OEM GTIN byte 0 (MSB)	0xFF	read / write (lockable)
0x04	OEM GTIN byte 1	0xFF	read / write (lockable)
0x05	OEM GTIN byte 2	0xFF	read / write (lockable)
0x06	OEM GTIN byte 3	0xFF	read / write (lockable)
0x07	OEM GTIN byte 4	0xFF	read / write (lockable)
0x08	OEM GTIN byte 5	0xFF	read / write (lockable)
0x09	OEM serial number byte 1 (MSB)	0xFF	read / write (lockable)
0x0A	OEM serial number byte 2	0xFF	read / write (lockable)
0x0B	OEM serial number byte 3	0xFF	read / write (lockable)
0x0C	OEM serial number byte 4 (LSB)	0xFF	read / write (lockable)
0x0D	Subsystem (bit 4 to bit 7) Device number (bit 0 to bit 3) ^c	0xFF	read / write (lockable)
0x0E	Lamp type number (lockable) ^c	0xFF	read / write (lockable)
0x0F	Lamp type number ^c	0xFF	read / write
≥ 0x10	additional OEM information ^d	0xFF	read / write (lockable)
^a = control gear leaves the factory ^b = the checksum shall be calculated by the control gear ^c = the coding of these bytes shall be defined by the OEM ^d = the purpose of these memory locations shall be defined by the OEM			

The byte in location 0x02 ("memory lock byte") shall be used to lock the write access.

The bytes in locations 0x03 to 0x08 ("OEM GTIN 0" to "OEM GTIN 5") shall be used to identify the luminaire, e. g. by storing the EAN code. The bytes shall be stored most significant first and filled with leading zeroes.

The bytes in locations 0x09 to 0x0C ("OEM serial number byte 1" to "OEM serial number byte 4") shall be used to store the unique serial number of the luminaire.

The byte in location 0x0D shall be used to store information about the device number (bit 0 to bit 3) of the control gear inside the luminaire or about the subsystem (bit 4 to bit 7) the control gear belongs to.

The bytes in locations 0x0E and 0x0F shall be used to store information about the lamp types that might be used.

Memory bank 1 shall not be affected by command 32 "RESET".

9.8.2.3 Other memory banks

Other memory banks can be used to store additional information and may be implemented according to the memory map shown in Table 5.

Table 5 – Memory map of other memory banks

Address	Description	Default value ^a	Memory access
0x00	address of last accessible memory location	factory burn in	read-only
0x01	checksum of memory bank	^b	read-only
0x02	memory bank lock byte (read-only if not 0x55)	0xFF	read / write
≥ 0x03	for free use	0xFF	read / write (lockable)
^a = control gear leaves the factory ^b = the checksum shall be calculated by the control gear			

The byte in location 0x02 ("memory lock byte") shall be used to lock the write access.

10 Declaration of variables

The default values, the reset values, the range of validity and the type of memory of the defined variables shall be as given in Table 6.

Table 6 – Declaration of variables

VARIABLE	DEFAULT VALUE (control gear leaves the factory)	RESET VALUE	RANGE OF VALIDITY	MEMORY ^b
"ACTUAL LEVEL"	???? ???? ^c	254	0, MIN LEVEL – MAX LEVEL	1 byte RAM
"POWER ON LEVEL" ^a	254	254	0– 255("MASK")	1 byte
"SYSTEM FAILURE LEVEL" ^a	254	254	0 – 255 ("MASK")	1 byte
"MIN LEVEL"	"PHYSICAL MIN LEVEL"	"PHYSICAL MIN LEVEL"	PHYSICAL MIN LEVEL – MAX LEVEL	1 byte
"MAX LEVEL"	254	254	MIN LEVEL – 254	1 byte
"FADE RATE"	7	7	1 – 15	1 byte
"FADE TIME"	0	0	0 – 15	1 byte
"SHORT ADDRESS"	255 ("MASK") no address	no change	0 – 63, ^d 255 ("MASK"),	1 byte
"SEARCH ADDRESS"	FF FF FF ^c	FF FF FF	00 00 00 - FF FF FF	3 bytes RAM
"RANDOM ADDRESS"	FF FF FF	FF FF FF	00 00 00 - FF FF FF	3 bytes
"GROUP 0-7"	0000 0000 (no group)	0000 0000 (no group)	0 – 255	1 byte
"GROUP 8-15"	0000 0000 (no group)	0000 0000 (no group)	0 – 255	1 byte
"SCENE 0-15" ^a	255 ("MASK")	255 ("MASK")	0 – 255 ("MASK")	16 bytes
"STATUS INFORMATION"	1??? ???? ^c	0?10 0???	0 – 255	1 byte RAM
DTR	???? ???? ^c	no change	0 – 255	1 byte RAM
DTR1	???? ???? ^c	no change	0 – 255	1 byte RAM
DTR2	???? ???? ^c	no change	0 – 255	1 byte RAM
"VERSION NUMBER"	factory burn-in	no change	0 – 255	1 byte ROM
"PHYSICAL MIN. LEVEL"	factory burn-in	no change	1 – 254	1 byte ROM
? = undefined ^a The actual arc power level shall be restricted by the min/max level range (see Clause 9.4). ^b Persistent memory (storage time indefinite) if not stated otherwise. ^c Power up value ^d 0 – 63 for AAAAAA in the format 0AAA AAA1				

11 Definition of commands

11.1 Arc power control commands

11.1.1 Direct arc power control command:

Command –: YAAA AAA0 XXXX XXXX "DIRECT ARC POWER CONTROL"

The actual arc power level shall be set to the value given by the data byte using the actual fade time. During fading, bit 4 of the status register shall indicate "fade is running".

Direct control commands outside the "MAX LEVEL" to "MIN LEVEL" range shall result in setting the arc power level to the respective MAX and MIN LEVEL. The arc power levels "0" (OFF) and "255" (MASK) shall not be affected by the MIN and MAX LEVEL settings.

"255" (MASK) means "STOP FADING"; this value shall subsequently be ignored and therefore not stored in a memory. If "MASK" is received during preheating the control gear shall remain switched off.

A received arc power level of "0" or "Mask" shall not have any visible effect on a lamp which is switched off.

11.1.2 Indirect arc power control commands

Command 0: YAAA AAA1 0000 0000 "OFF"

The lamp shall be extinguished immediately without fading.

Command 1: YAAA AAA1 0000 0001 "UP"

Dim up 200 ms using the selected FADE RATE. During fading bit 4 on the status register shall indicate a "fade is running".

There shall be no change if the arc power level is already at the "MAX LEVEL".

If this command is received again while it is being executed, the command shall be re-triggered.

This command shall not cause lamps to be switched on.

Command 2: YAAA AAA1 0000 0010 "DOWN"

Dim down 200 ms using the selected FADE RATE. During fading bit 4 on the status register shall indicate a "fade is running".

There shall be no change if the arc power level is already at the "MIN LEVEL".

If this command is received again while it is being executed, the command shall be re-triggered.

This command shall not cause lamps to be switched off.

Command 3: YAAA AAA1 0000 0011 "STEP UP"

The actual arc power level shall be set one step higher immediately without fading.

There shall be no change if the arc power level is already at the "MAX LEVEL".

This command shall not cause lamps to be switched on.

Command 4: YAAA AAA1 0000 0100 "STEP DOWN"

The actual arc power level shall be set one step lower immediately without fading.

There shall be no change if the arc power level is already at the "MIN LEVEL".

This command shall not cause lamps to be switched off.

Command 5: YAAA AAA1 0000 0101 "RECALL MAX LEVEL"

The actual arc power level shall be set to the "MAX LEVEL" without fading. If the lamp is off it shall be switched on with this command.

During initialization process the control gear shall start or restart an identification procedure defined by the manufacturer after receiving this command. Any other arc power control command shall stop the identification.

NOTE Identification can be done optically simply by setting the light output to maximum level.

Command 6: YAAA AAA1 0000 0110 "RECALL MIN LEVEL"

The actual arc power level shall be set to the "MIN LEVEL" without fading. If the lamp is off it shall be switched on with this command.

During the initialization process the control gear shall start or restart an identification procedure defined by the manufacturer after receiving this command. Any other arc power control command shall stop the identification.

NOTE Identification can be done optically simply by setting the light output to minimum level.

These identification procedures shall be implemented in such a way as to facilitate the unambiguous identification of individual control gear solely by means of commands 5 and 6 during the addressing process.

Command 7: YAAA AAA1 0000 0111 "STEP DOWN AND OFF"

The actual arc power level shall be set one step lower immediately without fading.

If the actual arc power level is already at the "MIN LEVEL", the lamp shall be switched off by this command.

Command 8: YAAA AAA1 0000 1000 "ON AND STEP UP"

The actual arc power level shall be set one step higher immediately without fading.

If the lamp is switched off, the lamp shall be switched on with this command and shall be set to the "MIN LEVEL".

Command 9: YAAA AAA1 0000 1001 "ENABLE DAPC SEQUENCE"

This command shall mark the start of a direct arc power control (DAPC) sequence that allows the control device to control the dimming speed dynamically.

A DAPC sequence shall consist of an "ENABLE DAPC SEQUENCE" command, followed by several "DIRECT ARC POWER CONTROL" commands separated by no more than 200 ms.

The DAPC sequence shall end if 200 ms elapse without the gear receiving a "DIRECT ARC POWER CONTROL" command. The DAPC sequence shall be aborted on receipt of an indirect arc power control command other than command 9.

During a DAPC sequence the ordinary FADE TIME shall be replaced by a fade time greater than or equal to 200 ms. The speed of changing the arc power level may be limited to a maximum depending on the capability of the control gear; this maximum shall be at least 358 steps/s (FADE RATE 1). The ordinary FADE TIME shall be automatically restored if the DAPC sequence ends.

If the actual arc power level is zero, the new level shall be adopted without fading.

Commands 10 – 11: YAAA AAA1 0000 101X

Reserved for future needs. The control gear shall not react in any way.

Commands 12 – 15: YAAA AAA1 0000 11XX

Reserved for future needs. The control gear shall not react in any way.

Commands 16 – 31: YAAA AAA1 0001 XXXX "GO TO SCENE"

Set the actual arc power level to the value stored for scene XXXX using the actual fade time. During fading, bit 4 on the status register shall indicate a "fade is running".

If the control gear does not belong to scene XXXX ('255' / 'MASK' is stored), the arc power level shall remain unchanged.

11.2 Configuration commands:

11.2.1 General configuration commands:

Every configuration command (32 – 129) shall be received a second time within 100 ms (nominal) before it is executed, in order to reduce the probability of incorrect reception. No other commands addressing the same control gear shall be sent between these two commands, otherwise the first such command shall be ignored and the respective configuration sequence aborted. See Figure 11.

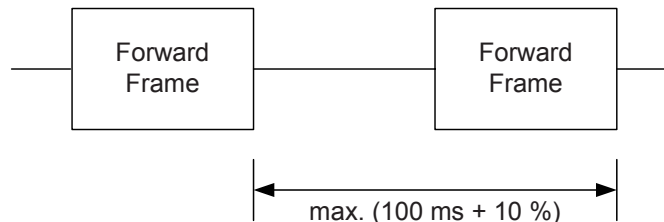


Figure 11 – Configuration commands timing

All values of DTR shall be checked against the values mentioned in Table 6. I.e. the value shall be set to the upper/lower limit if it is above/below the valid range defined in Table 6.

Command 32: YAAA AAA1 0010 0000 "RESET"

After the second reception of the command, the variables in the memory (see Clause 10) shall be changed to their reset values. It is not guaranteed that commands are received properly within the next 300 ms.

Command 33: YAAA AAA1 0010 0001 "STORE ACTUAL LEVEL IN THE DTR"

The actual arc power level shall be stored in the DTR.

In case of a lamp failure the "virtual" Arc Power Level shall be stored.

Commands 34 – 35: YAAA AAA1 0010 001X

Reserved for future needs. The control gear shall not react in any way.

Commands 36 – 39: YAAA AAA1 0010 01XX

Reserved for future needs. The control gear shall not react in any way.

Commands 40 – 41: YAAA AAA1 0010 100X

Reserved for future needs. The control gear shall not react in any way.

11.2.2 Arc power parameters settings:

Command 42: YAAA AAA1 0010 1010 "STORE THE DTR AS MAX LEVEL"

The value in "Data Transfer Register" shall be saved as the new "MAX LEVEL".

If this value is below the "MIN LEVEL" of the control gear then the "MIN LEVEL" shall be stored as the new "MAX LEVEL".

If the "ACTUAL LEVEL" is above the new "MAX LEVEL" it should be set to the new "MAX LEVEL" immediately without fading.

If the content of DTR is MASK then 254 shall be stored as MAX LEVEL.

Command 43: YAAA AAA1 0010 1011 "STORE THE DTR AS MIN LEVEL"

The value in "Data Transfer Register" shall be stored as new "MIN LEVEL". If this value is less than the "PHYSICAL MIN LEVEL" of the control gear, then the "PHYSICAL MIN LEVEL" shall be stored as the new "MIN LEVEL".

If this value is MASK or is above the "MAX LEVEL" of the control gear, then the "MAX LEVEL" shall be stored as the new "MIN LEVEL".

If the "ACTUAL LEVEL" is below the new "MIN LEVEL" it should be set to the new "MIN LEVEL" immediately without fading, but if the "ACTUAL LEVEL" is "0" (OFF) it should not be affected by "STORE THE DTR AS MIN LEVEL".

Command 44: YAAA AAA1 0010 1100 "STORE THE DTR AS SYSTEM FAILURE LEVEL"

The value in "Data Transfer Register" shall be saved as new "SYSTEM FAILURE LEVEL".

Command 45: YAAA AAA1 0010 1101 "STORE THE DTR AS POWER ON LEVEL"

The value in "Data Transfer Register" shall be saved as the new "POWER ON LEVEL".

Command 46: YAAA AAA1 0010 1110 "STORE THE DTR AS FADE TIME"

The "FADE TIME", T , shall be set to a value according to the following formula, with a tolerance of $\pm \frac{1}{2}$ step; monotonic. See also 9.5.

$$T = \frac{1}{2} \cdot \sqrt{2^X} \cdot 1s \text{ with } X = 1 - 15.$$

where $X = 0$ means no fade.

NOTE The fade time specifies the time for changing the arc power level from the actual level to the requested level. If the lamp is off, preheat and ignition (strike) time should not be included in the fade time.

The new fade time shall be valid after the reception of the next arc power command. If a new fade time is stored during a running fade process, this process shall be finished first before the new value is used.

NOTE The fade time is used by the commands "DIRECT ARC POWER CONTROL" and "GO TO SCENE".

Command 47: YAAA AAA1 0010 1111 "STORE THE DTR AS FADE RATE"

The "FADE RATE", F , shall be set to the value given by the following formula, with a tolerance of $\pm \frac{1}{2}$ step; monotonic. See 9.5.

$$F = \frac{506}{\sqrt{2^X}} \text{ steps/s}$$

with $X = 1 - 15$

NOTE The fade rate specifies the rate in steps/s for changing the arc power level.

The new fade rate shall be valid after the reception of the next arc power command. If a new fade rate is stored during a running fade process, this process shall be finished first before the new value is used.

NOTE The fade rate is used by the commands "UP" and "DOWN".

Commands 48 – 63: YAAA AAA1 0011 XXXX

Reserved for future needs. The control gear shall not react in any way.

Commands 64 – 79: YAAA AAA1 0100 XXXX "STORE THE DTR AS SCENE"

The value in the Data Transfer Register shall be stored as a new level for the scene XXXX.

11.2.3 System parameters settings

Commands 80 – 95: YAAA AAA1 0101 XXXX "REMOVE FROM SCENE"

The control gear shall be removed from scene XXXX.

Removing the control gear from scene XXXX means storing 1111 1111 ("MASK" or "DON'T CHANGE") in scene register XXXX.

Commands 96 – 111: YAAA AAA1 0110 XXXX "ADD TO GROUP"

The control gear shall be added to group XXXX.

Commands 112 – 127: YAAA AAA1 0111 XXXX "REMOVE FROM GROUP"

The control gear shall be removed from group XXXX.

Removing the control gear from group XXXX means storing "0" in the corresponding bit of the group register

Command 128: YAAA AAA1 1000 0000 "STORE DTR AS SHORT ADDRESS"

The value in the DTR shall be saved as a new short address.

The structure of the content of the DTR shall be: XXXX XXXX = 0AAA AAA1 or 1111 1111 ("MASK"). MASK shall remove the short address.

NOTE If the values are invalid, the command will be ignored.

Command 129: YAAA AAA1 1000 0001 "ENABLE WRITE MEMORY"

The command shall enable subsequent writes to memory. The write enabled state shall be cancelled by reception of any other command than "WRITE MEMORY LOCATION" or "ENABLE WRITE MEMORY" addressing the same control gear.

See 9.8 for detailed information.

Commands 130 – 131: YAAA AAA1 1000 001X

Reserved for future needs. The control gear shall not react in any way.

Commands 132 – 135: YAAA AAA1 1000 01XX

Reserved for future needs. The control gear shall not react in any way.

Commands 136 – 143: YAAA AAA1 1000 1XXX

Reserved for future needs. The control gear shall not react in any way.

11.3 Query commands

11.3.1 Queries related to status information

If the parameters listed in Table 6 have their reset values, the control gear shall be in the "RESET STATE".

Command 144: YAAA AAA1 1001 0000 "QUERY STATUS"

The answer shall be the following "STATUS INFORMATION" byte:

bit 0	Status of control gear;	"0" = OK
bit 1	Lamp failure;	"0" = OK
bit 2	Lamp arc power on;	"0" = OFF
bit 3	Query: Limit Error;	"0" = Last requested arc power level is between MIN and MAX LEVEL or OFF
bit 4	Fade running;	"0" = fade is ready; "1" = fade is running
bit 5	Query: "RESET STATE"?	"0" = "No"
bit 6	Query: Missing short address?	"0" = "No"
bit 7	Query: "POWER FAILURE"?	"0" = "No"; "RESET" or an arc power control command has been received since last power-on.

The "STATUS INFORMATION" shall be available in the RAM of the control gear and shall be updated regularly by the control gear according to the actual situation.

Command 145: YAAA AAA1 1001 0001 "QUERY CONTROL GEAR"

Ask if there is a control gear with the given address that is able to communicate. The answer shall be "Yes" or "No".

Command 146: YAAA AAA1 1001 0010 "QUERY LAMP FAILURE"

Ask if there is a lamp problem at the given address. The answer shall be "Yes" or "No".

Command 147: YAAA AAA1 1001 0011 "QUERY LAMP POWER ON"

Ask if there is a lamp operating at the given address. The answer shall be "Yes" or "No".

Command 148: YAAA AAA1 1001 0100 "QUERY LIMIT ERROR"

Ask if the last requested arc power level at the given address could not be met, because it is above the MAX LEVEL or below the MIN LEVEL. The answer shall be "Yes" or "No".

Command 149: YAAA AAA1 1001 0101 "QUERY RESET STATE"

Ask if the control gear is in "RESET STATE". The answer shall be "Yes" or "No".

Command 150: YAAA AAA1 1001 0110 "QUERY MISSING SHORT ADDRESS"

Ask if the control gear has no short address. The answer shall be "Yes" or "No".

The answer shall be "Yes" if the control gear has no short address.

Command 151: YAAA AAA1 1001 0111 "QUERY VERSION NUMBER"

The answer shall be 1.

Command 152: YAAA AAA1 1001 1000 "QUERY CONTENT DTR"

The answer shall be the content of the DTR as an 8-bit number.

Command 153: YAAA AAA1 1001 1001 "QUERY DEVICE TYPE"

The answer shall be the device type as an 8-bit number. If the control gear supports more than one device type the answer shall be 255 ("MASK").

The coding of the device types shall be as given in Annex B of this standard.

Command 154: YAAA AAA1 1001 1010 "QUERY PHYSICAL MINIMUM LEVEL"

The answer shall be the "PHYSICAL MINIMUM LEVEL" as an 8-bit number.

Command 155: YAAA AAA1 1001 1011 "QUERY POWER FAILURE"

The answer shall be "YES" if the control gear has not received a "RESET" or one of the following arc power control commands since the last power-on: "DIRECT ARC POWER CONTROL", "OFF", "RECALL MAX LEVEL", "RECALL MIN LEVEL", "STEP DOWN AND OFF", "ON AND STEP UP", "GO TO SCENE"

Command 156: YAAA AAA1 1001 1100 "QUERY CONTENT DTR1"

Answer shall be the content of the DTR1 as an 8-bit number.

Command 157: YAAA AAA1 1001 1101 "QUERY CONTENT DTR2"

The answer shall be the content of the DTR2 as an 8-bit number.

Commands 158 – 159: YAAA AAA1 1001 111X

Reserved for future needs. The control gear shall not react in any way.

11.3.2 Queries related to arc power parameter settings

Command 160: YAAA AAA1 1010 0000 "QUERY ACTUAL LEVEL"

The answer shall be the actual arc power level. During preheating and whenever there is a lamp error the answer shall be "MASK".

Command 161: YAAA AAA1 1010 0001 "QUERY MAX LEVEL"

The answer shall be this level as an 8-bit number.

Command 162: YAAA AAA1 1010 0010 "QUERY MIN LEVEL"

The answer shall be this level as an 8-bit number.

Command 163: YAAA AAA1 1010 0011 "QUERY POWER ON LEVEL"

The answer shall be this level as an 8-bit number.

Command 164: YAAA AAA1 1010 0100 "QUERY SYSTEM FAILURE LEVEL"

The answer shall be this level as an 8-bit number.

Command 165: YAAA AAA1 1010 0101 "QUERY FADE TIME/FADE RATE"

The answer shall be XXXX YYYY, where XXXX is the fade time and YYYY is the fade rate.

Commands 166 – 167: YAAA AAA1 1010 011X

Reserved for future needs. The control gear shall not react in any way.

Commands 168 – 175: YAAA AAA1 1010 1XXX

Reserved for future needs. The control gear shall not react in any way.

11.3.3 Queries related to system parameter settings

Commands 176 – 191: YAAA AAA1 1011 XXXX "QUERY SCENE LEVEL (SCENES 0- 15)"

The answer shall be the arc power level of scene XXXX as an 8-bit number.

Command 192: YAAA AAA1 1100 0000 "QUERY GROUPS 0-7"

The answer shall be the membership of groups 0-7 as an 8-bit value.

There shall be one bit for each group.

LSB = group 0.

"0" = not belonging to group. "1" = belonging to group.

Command 193: YAAA AAA1 1100 0001 "QUERY GROUPS 8-15"

The answer shall be the membership of groups 8-15 as an 8-bit value.

There shall be one bit for each group.

LSB = group 8.

"0" = not belonging to group. "1" = belonging to group.

11.4.2 Download information to the DTR

Command 257: **1010 0011 XXXX XXXX** **"DATA TRANSFER REGISTER (DTR)"**

The 8-bit value XXXX XXXX shall be stored to DTR.

11.4.3 Addressing commands

The address range shall be set to a maximum of 24-bits (3 bytes) which leads to 16 777 216 different addresses.

There are Addressing Commands where the control gear shall answer as if to a Query Command.

Command 258: **1010 0101 XXXX XXXX** **"INITIALISE"**

This command shall be received a second time within 100 ms (nominal) before it is executed in order to reduce the probability of incorrect reception. No other commands addressing the same control gear shall be sent between these two commands, otherwise the first such command and command 258 shall be ignored.

The command shall start or re-trigger a 15 minute timer; the addressing commands 259 to 270 shall only be processed whilst this timer is running. The other commands shall still be processed during this period.

This time period shall be aborted with the "TERMINATE" command.

The reaction of control gear receiving this command depends on the content of the 2nd byte:

XXXX XXXX = 0000 0000 All control gear shall react

XXXX XXXX = 0AAA AAA1 Control gear with the address AAAAAAb shall react

XXXX XXXX = 1111 1111 Control gear without short address shall react

Command 259: **1010 0111 0000 0000** **"RANDOMISE"**

This command shall be received a second time within 100 ms (nominal) before it is executed in order to reduce the probability of incorrect reception. No other commands addressing the same control gear shall be sent between these two commands; otherwise the first such command and command 259 shall be ignored.

The control gear shall generate a new random address on receipt of this command.

The new random address shall be available within a time period of 100 ms.

Command 260: **1010 1001 0000 0000** **"COMPARE"**

The control gear shall compare its random address with the combined search address stored in SEARCHADDRH, SEARCHADDRM and SEARCHADDRL. If its random address is less than or equal to the combined search address stored in SEARCHADDRH, SEARCHADDRM and SEARCHADDRL then the control gear shall answer "YES".

Command 261: **1010 1011 0000 0000** **"WITHDRAW"**

The control gear whose random address is equal to the combined search address stored in SEARCHADDRH, SEARCHADDRM and SEARCHADDRL shall be excluded from the compare process. This control gear shall not be excluded from the initialization process.

Commands 262 – 263: **1010 11X1 0000 0000**

Reserved for future needs. The control gear shall not react in any way.

Command 264: **1011 0001 HHHH HHHH** **"SEARCHADDRH"**

The 8 high bits of the search address.

Command 265: **1011 0011 MMMM MMMM "SEARCHADDRM"**

The 8 mid bits of the search address.

Command 266: **1011 0101 LLLL LLLL "SEARCHADDRL"**

The 8 low bits of the search address.

The combination of the three addresses from command 264 to 266 shall constitute the 24-bit search address HHHH HHHH MMMM MMMM LLLL LLLL.

Command 267: **1011 0111 0AAA AAA1 "PROGRAM SHORT ADDRESS"**

The control gear shall store the received 6-bit address as its short address if it is selected.

"Selected" shall mean one of the following:

- The control gear's random address is equal to the combined search address stored in SEARCHADDRH, SEARCHADDRM and SEARCHADDRL.
- The control gear is physically selected. Physical selection shall be detected by the control gear if a lamp is electrically disconnected from the control gear after reception of Command 270.

The short address shall be deleted by receiving the following completion of command 267 in the following form:

1011 0111 1111 1111 meaning "delete the short address"

Command 268: **1011 1001 0AAA AAA1 "VERIFY SHORT ADDRESS"**

The control gear shall answer "YES" if the received 6-bit short address is equal to its own short address.

Command 269: **1011 1011 0000 0000 "QUERY SHORT ADDRESS"**

The control gear shall answer its short address if the random address is equal to the search address or the control gear is physically selected. The format of the answer shall be 0AAA AAA1 or MASK.

Command 270: **1011 1101 0000 0000 "PHYSICAL SELECTION"**

If a control gear receives this command, it shall cancel its physical selection and shall set the control gear to "Physical Selection Mode". In this mode the compare of SEARCH and RANDOM ADDRESS shall be disabled.

Command 271: **1011 1111 XXXX XXXX**

Reserved for future needs. The control gear shall not react in any way.

11.4.4 Extended special commands

Command 272: **1100 0001 XXXX XXXX "ENABLE DEVICE TYPE X"**

This command shall select the device type for which the next following application extended command (224 to 255) is valid. Receiving this command shall cancel any previous selection of a device type. The selection is only valid for the next following application extended command.

If a command addressed to the same control gear is received between command 272 and an application extended command, the application extended command shall not be executed and the selection shall be cancelled.

The valid range of X shall be 0 to 254.

This command shall be processed without the use of the INITIALISE command.

A control gear shall not react to a command which belongs to the application extended commands of a device type different from its own.

All control gear shall be able to respond in an appropriate way to the standard range of commands.

The device types shall be as listed in Annex B and coded as specified in the particular parts 2XX of IEC 62386.

NOTE Control devices should be able to identify individual devices and store the relationship between device's individual address and the device type in a persistent memory.

Command 273: **1100 0011 XXXX XXXX "DATA TRANSFER REGISTER 1 (DTR1)"**

The 8-bit value XXXX XXXX shall be stored to DTR1.

Command 274: **1100 0101 XXXX XXXX "DATA TRANSFER REGISTER 2 (DTR2)"**

The 8-bit value XXXX XXXX shall be stored to DTR2.

Command 275: **1100 0111 XXXX XXXX "WRITE MEMORY LOCATION"**

If memory is write enabled, the value given by XXXX XXXX shall be stored in a memory location. The memory bank shall be selected by the content of DTR1 and the address shall be given by the content of DTR.

After the execution of this command, the content of DTR shall be incremented. Writing to the last accessible memory location shall cancel the write enabled state after processing the command.

This command shall be ignored if the memory is not write enabled, if the address is outside of the valid range or if the selected memory bank is not implemented.

Writes to valid addresses which are designated as read-only by the manufacturer shall be ignored except that the content of DTR shall be incremented by 1.

If the memory location can be written to, the command shall cause a back-channel answer containing the value written.

See 9.8 for detailed information.

NOTE Simultaneous writes to several devices are likely to cause corruption of the back-channel answer.

Commands 276 – 279: **1100 1XX1 XXXX XXXX**

Reserved for future needs. The control gear shall not react in any way.

Commands 280 – 287: **1101 XXX1 XXXX XXXX**

Reserved for future needs. The control gear shall not react in any way.

Commands 288 – 295: **1110 XXX1 XXXX XXXX**

Reserved for future needs. The control gear shall not react in any way.

Commands 296 – 299: **1111 0XX1 XXXX XXXX**

Reserved for future needs. The control gear shall not react in any way.

Commands 300 – 301: **1111 10X1 XXXX XXXX**

Reserved for future needs. The control gear shall not react in any way.

Command 302: 1111 1101 XXXX XXXX

Reserved for future needs. The control gear shall not react in any way.

Commands 303 – 318: 101X XXX0 XXXX XXXX

Reserved for future needs. The control gear shall not react in any way.

Commands 319 – 334: 110X XXX0 XXXX XXXX

Reserved for future needs. The control gear shall not react in any way.

Commands 335 – 342: 1110 XXX0 XXXX XXXX

Reserved for future needs. The control gear shall not react in any way.

Commands 343 – 346: 1111 0XX0 XXXX XXXX

Reserved for future needs. The control gear shall not react in any way.

Commands 347 – 348: 1111 10X0 XXXX XXXX

Reserved for future needs. The control gear shall not react in any way.

Command 349: 1111 1100 XXXX XXXX

Reserved for future needs. The control gear shall not react in any way.

11.5 Summary of the command set

Table 7 gives a summary of the command set.

Table 7 – Summary of the command set

Command number	Command code	Command name
–	YAAA AAA0 XXXX XXXX	DIRECT ARC POWER CONTROL
0	YAAA AAA1 0000 0000	OFF
1	YAAA AAA1 0000 0001	UP
2	YAAA AAA1 0000 0010	DOWN
3	YAAA AAA1 0000 0011	STEP UP
4	YAAA AAA1 0000 0100	STEP DOWN
5	YAAA AAA1 0000 0101	RECALL MAX LEVEL
6	YAAA AAA1 0000 0110	RECALL MIN LEVEL
7	YAAA AAA1 0000 0111	STEP DOWN AND OFF
8	YAAA AAA1 0000 1000	ON AND STEP UP
9	YAAA AAA1 0000 1001	ENABLE DAPC SEQUENCE
10 – 11	YAAA AAA1 0000 101X	^a
12 – 15	YAAA AAA1 0000 11XX	^a
16 – 31	YAAA AAA1 0001 XXXX	GO TO SCENE
32	YAAA AAA1 0010 0000	RESET
33	YAAA AAA1 0010 0001	STORE ACTUAL LEVEL IN THE DTR
34 – 35	YAAA AAA1 0010 001X	^a
36 – 39	YAAA AAA1 0010 01XX	^a
40 – 41	YAAA AAA1 0010 100X	^a
42	YAAA AAA1 0010 1010	STORE THE DTR AS MAX LEVEL
43	YAAA AAA1 0010 1011	STORE THE DTR AS MIN LEVEL
44	YAAA AAA1 0010 1100	STORE THE DTR AS SYSTEM FAILURE LEVEL
45	YAAA AAA1 0010 1101	STORE THE DTR AS POWER ON LEVEL
46	YAAA AAA1 0010 1110	STORE THE DTR AS FADE TIME
47	YAAA AAA1 0010 1111	STORE THE DTR AS FADE RATE
48 – 63	YAAA AAA1 0011 XXXX	^a
64 – 79	YAAA AAA1 0100 XXXX	STORE THE DTR AS SCENE
80 – 95	YAAA AAA1 0101 XXXX	REMOVE FROM SCENE
96 – 111	YAAA AAA1 0110 XXXX	ADD TO GROUP
112 – 127	YAAA AAA1 0111 XXXX	REMOVE FROM GROUP
128	YAAA AAA1 1000 0000	STORE DTR AS SHORT ADDRESS
129	YAAA AAA1 1000 0001	ENABLE WRITE MEMORY
130 – 131	YAAA AAA1 1000 001X	^a
132 – 135	YAAA AAA1 1000 01XX	^a
136 – 143	YAAA AAA1 1000 1XXX	^a
144	YAAA AAA1 1001 0000	QUERY STATUS
145	YAAA AAA1 1001 0001	QUERY CONTROL GEAR
146	YAAA AAA1 1001 0010	QUERY LAMP FAILURE
147	YAAA AAA1 1001 0011	QUERY LAMP POWER ON

Table 7 (continued)

Command number	Command code	Command name
148	YAAA AAA1 1001 0100	QUERY LIMIT ERROR
149	YAAA AAA1 1001 0101	QUERY RESET STATE
150	YAAA AAA1 1001 0110	QUERY MISSING SHORT ADDRESS
151	YAAA AAA1 1001 0111	QUERY VERSION NUMBER
152	YAAA AAA1 1001 1000	QUERY CONTENT DTR
153	YAAA AAA1 1001 1001	QUERY DEVICE TYPE
154	YAAA AAA1 1001 1010	QUERY PHYSICAL MINIMUM LEVEL
155	YAAA AAA1 1001 1011	QUERY POWER FAILURE
156	YAAA AAA1 1001 1100	QUERY CONTENT DTR1
157	YAAA AAA1 1001 1101	QUERY CONTENT DTR2
158 – 159	YAAA AAA1 1001 111X	^a
160	YAAA AAA1 1010 0000	QUERY ACTUAL LEVEL
161	YAAA AAA1 1010 0001	QUERY MAX LEVEL
162	YAAA AAA1 1010 0010	QUERY MIN LEVEL
163	YAAA AAA1 1010 0011	QUERY POWER ON LEVEL
164	YAAA AAA1 1010 0100	QUERY SYSTEM FAILURE LEVEL
165	YAAA AAA1 1010 0101	QUERY FADE TIME/FADE RATE
166 – 167	YAAA AAA1 1010 011X	^a
168 – 175	YAAA AAA1 1010 1XXX	^a
176 – 191	YAAA AAA1 1011 XXXX	QUERY SCENE LEVEL (SCENES 0-15)
192	YAAA AAA1 1100 0000	QUERY GROUPS 0-7
193	YAAA AAA1 1100 0001	QUERY GROUPS 8-15
194	YAAA AAA1 1100 0010	QUERY RANDOM ADDRESS (H)
195	YAAA AAA1 1100 0011	QUERY RANDOM ADDRESS (M)
196	YAAA AAA1 1100 0100	QUERY RANDOM ADDRESS (L)
197	YAAA AAA1 1100 0101	READ MEMORY LOCATION
198 – 199	YAAA AAA1 1100 011X	^a
199 – 207	YAAA AAA1 1100 1XXX	^a
208 – 223	YAAA AAA1 1101 XXXX	^a
224 – 254	YAAA AAA1 111X XXXX	See parts 2XX of this standard
255	YAAA AAA1 1111 1111	QUERY EXTENDED VERSION NUMBER
256	1010 0001 0000 0000	TERMINATE
257	1010 0011 XXXX XXXX	DATA TRANSFER REGISTER (DTR)
258	1010 0101 XXXX XXXX	INITIALISE
259	1010 0111 0000 0000	RANDOMISE
260	1010 1001 0000 0000	COMPARE
261	1010 1011 0000 0000	WITHDRAW
262 – 263	1010 11X1 0000 0000	^a
264	1011 0001 HHHH HHHH	SEARCHADDRH
265	1011 0011 MMMM	SEARCHADDRM
266	1011 0101 LLLL LLLL	SEARCHADDRL
267	1011 0111 0AAA AAA1	PROGRAM SHORT ADDRESS

Table 7 (continued)

Command number	Command code	Command name
268	1011 1001 0AAA AAA1	VERIFY SHORT ADDRESS
269	1011 1011 0000 0000	QUERY SHORT ADDRESS
270	1011 1101 0000 0000	PHYSICAL SELECTION
271	1011 1111 XXXX XXXX	^a
272	1100 0001 XXXX XXXX	ENABLE DEVICE TYPE X
273	1100 0011 XXXX XXXX	DATA TRANSFER REGISTER 1 (DTR1)
274	1100 0101 XXXX XXXX	DATA TRANSFER REGISTER 2 (DTR2)
275	1100 0111 XXXX XXXX	WRITE MEMORY LOCATION
276 – 279	1100 1XX1 XXXX XXXX	^a
280 – 287	1101 XXX1 XXXX XXXX	^a
288 – 295	1110 XXX1 XXXX XXXX	^a
296 – 299	1111 0XX1 XXXX XXXX	^a
300 – 301	1111 10X1 XXXX XXXX	^a
302	1111 1101 XXXX XXXX	^a
303 – 318	101X XXX0 XXXX XXXX	^a
319 – 334	110X XXX0 XXXX XXXX	^a
335 – 342	1110 XXX0 XXXX XXXX	^a
343 – 346	1111 0XX0 XXXX XXXX	^a
347 – 348	1111 10X0 XXXX XXXX	^a
349	1111 1100 XXXX XXXX	^a

^a Reserved for future needs. The control gear shall not react in any way.

12 Test procedures

12.0 General

A control gear shall be built in such a way that it can be tested with the test procedures given in Clause 12 and in the relevant part of the IEC 62386-200 series.

The test set-up shall consist of a computer programmed according to the test procedure and a hardware adapter, which are connected to the control interface port of the device under test (DUT), as shown in Figure 12.

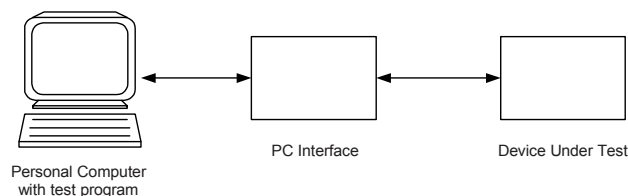


Figure 12 – General test structure

The test sequence shall consist principally of an activation phase (command output) and a validation phase. In the activation phase the command to be tested shall be sent to the DUT and in the validation phase the internal state of the DUT shall be checked by query commands. See Figure 13.