

BS EN 62418:2010



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Semiconductor devices — Metallization stress void test

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The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors.

A list of organizations represented on this committee can be obtained on request to its secretary.

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English version

Semiconductor devices - Metallization stress void test (IEC 62418:2010)

Dispositifs à semi-conducteurs -
Essai sur les cavités dues aux contraintes
de la métallisation
(CEI 62418:2010)

Halbleiterbauelemente -
Prüfverfahren zur Metallisierungs-
Stressmigration
(IEC 62418:2010)

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Foreword

The text of document 47/2043/FDIS, future edition 1 of IEC 62418, prepared by IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 62418 on 2010-07-01.

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The following dates were fixed:

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|--|-------|------------|
| – latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement | (dop) | 2011-04-01 |
| – latest date by which the national standards conflicting with the EN have to be withdrawn | (dow) | 2013-07-01 |

Endorsement notice

The text of the International Standard IEC 62418:2010 was approved by CENELEC as a European Standard without any modification.

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SEMICONDUCTOR DEVICES – METALLIZATION STRESS VOID TEST

1 Scope

This International Standard describes a method of metallization stress void test and associated criteria. It is applicable to aluminium (Al) or copper (Cu) metallization.

This standard is applicable for reliability investigation and qualification of semiconductor process.

2 Test equipment

A calibrated hot chuck or thermal chamber is required to subject the wafers or packaged test structures to the specified temperature ($\pm 5^\circ\text{C}$) for the specified time. For resistance measurements dedicated equipment is needed. For void inspection deprocessing equipment is required to remove the scratch protection layer. The inspections are performed with a scanning electron microscope (SEM).

3 Test structure

3.1 Test structure patterns

Test structures shall be used for all metal layers which have to be inspected and several different types of structure may be used. The following two types of test structures are applicable for this test standard.

NOTE For metallization without refractory shunt layers reflective notching at steps can occur in test structures with underlying topography, which will therefore tend to indicate a relatively worse stress-voiding behaviour.

3.2 Line pattern

Parallel lines which are patterned at the minimum linewidth allowed by design form an appropriate test structure. Unless otherwise specified a minimum length of 500 μm and a total length of 1 cm to 1 000 cm are recommended condition. Single long isolated lines are recommended because stress voiding is often sensitive to line-to-line separation.

NOTE 1 Narrow lines are susceptible for stress voiding because the stress in the metal is typically higher in narrower lines than in wider lines.

NOTE 2 The line length should be sufficient to insure that void nucleation sites will exist.

3.3 Via chain pattern

3.3.1 Pattern types

A via chain pattern is applicable as a test structure. For technology investigations a Kelvin-pattern for four-point measurements may also be used.

3.3.2 Pattern for aluminium (Al) process

Via chains need to consist of a pattern of vias connected by minimum linewidth. The recommended number of vias is between 1 000 and 100 000. It is recommended to use isolated and long minimum linewidths.