



BSI Standards Publication

Components for low-voltage surge protection

Part 341: Performance requirements and test circuits
for thyristor surge suppressors (TSS)

National foreword

This British Standard is the UK implementation of EN IEC 61643-341:2020. It is identical to IEC 61643-341:2020. It supersedes BS EN 61643-341:2001, which is withdrawn.

The UK participation in its preparation was entrusted to Technical Committee PEL/37/1, Surge Arresters - Low Voltage.

A list of organizations represented on this committee can be obtained on request to its committee manager.

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Date	Text affected
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English Version

Components for low-voltage surge protection - Part 341:
Performance requirements and test circuits for thyristor surge
suppressors (TSS)
(IEC 61643-341:2020)

Composants pour parafoudres basse tension - Partie 341:
Exigences de performance et circuits d'essai pour
parafoudres à thyristor (TSS)
(IEC 61643-341:2020)

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Niederspannung - Teil 341: Leistungsanforderungen sowie
Prüfschaltungen für Suppressordioden (TSS)
(IEC 61643-341:2020)

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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

CEN-CENELEC Management Centre: Rue de la Science 23, B-1040 Brussels

European foreword

The text of document 37B/218/FDIS, future edition 2 of IEC 61643-341, prepared by SC 37B "Components for low-voltage surge protection" of IEC/TC 37 "Surge arresters" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 61643-341:2020.

The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2021-03-17
- latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2023-06-17

This document supersedes EN 61643-341:2001 and all of its amendments and corrigenda (if any).

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC shall not be held responsible for identifying any or all such patent rights.

Endorsement notice

The text of the International Standard IEC 61643-341:2020 was approved by CENELEC as a European Standard without any modification.

In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 60060-1:2010	NOTE	Harmonized as EN 60060-1:2010 (not modified)
IEC 60068-2-20:2008	NOTE	Harmonized as EN 60068-2-20:2008 (not modified)
IEC 60068-2-21:2006	NOTE	Harmonized as EN 60068-2-21:2006 (not modified)
IEC 60099-4:2014	NOTE	Harmonized as EN 60099-4:2014 (not modified)
IEC 60721-3-3:2019	NOTE	Harmonized as EN IEC 60721-3-3:2019 (not modified)
IEC 60721-3-9:1993	NOTE	Harmonized as EN 60721-3-9:1993 (not modified)
IEC 60749-1:2002	NOTE	Harmonized as EN 60749-1:2003 (not modified)
IEC 60950-1:2005	NOTE	Harmonized as EN 60950-1:2006 (modified)
IEC 61000-4-5:2014	NOTE	Harmonized as EN 61000-4-5:2014 (not modified)
IEC 61643-11:2011	NOTE	Harmonized as EN 61643-11:2012 (modified)
IEC 62475:2010	NOTE	Harmonized as EN 62475:2010 (not modified)

Annex ZA

(normative)

Normative references to international publications with their corresponding European publications

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 Where an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu.

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 60050-521	-	International Electrotechnical Vocabulary - Part 521: Semiconductor devices and integrated circuits	-	-
IEC 60068-2-20	2008	Environmental testing - Part 2-20: Tests - Test T: Test methods for solderability and resistance to soldering heat of devices with leads	EN 60068-2-20	2008

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

COMPONENTS FOR LOW-VOLTAGE SURGE PROTECTION –**Part 341: Performance requirements and test circuits
for thyristor surge suppressors (TSS)**

FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as “IEC Publication(s)”). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC 61643-341 has been prepared by subcommittee 37B, Components for low-voltage surge protection, of IEC technical committee 37: Surge arresters.

This second edition of IEC 61643-341 cancels and replaces the first edition published in 2001. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition: Addition of performance values.

The text of this standard is based on the following documents:

FDIS	Report on voting
37B/218/FDIS	37B/220/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts of IEC 61643 series, under the general title *Components for low-voltage surge protective devices*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

COMPONENTS FOR LOW-VOLTAGE SURGE PROTECTION –

Part 341: Performance requirements and test circuits for thyristor surge suppressors (TSS)

1 Scope

This part of IEC 61643 specifies standard test circuits and methods for thyristor surge suppressor (TSS) components. These surge protective components, SPCs, are specially formulated thyristors designed to limit overvoltages and divert surge currents by clamping and switching actions. These SPCs are used in the construction of surge protective devices (SPDs) and equipment used in Information & Communications Technologies (ICT) networks with voltages up to AC 1 000 V and DC 1 500 V. This document is applicable to gated or non-gated TSS components with third quadrant (-v and -i) characteristics of blocking, conducting or switching.

This document contains information on

- terminology;
- letter symbols;
- essential ratings and characteristics;
- rating verification and characteristic measurement;

This document does not apply to the conventional three-terminal thyristors as covered by IEC 60747-6.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050-521, *International Electrotechnical Vocabulary – Chapter 521: Semiconductor devices and integrated circuits*

IEC 60068-2-20:2008, *Environmental testing – Part 2-20: Tests – Test T: Test methods for solderability and resistance to soldering heat of devices with leads*

3 Terms, definitions, abbreviated terms and symbols

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

3.1 Parametric terms, letter symbols and definitions

Where appropriate, terms, letter symbols and definitions are used from conventional thyristor (IEC 60747-6) and rectifier diode (IEC 60747-2) standards. TSS definitions are the same or similar to conventional thyristor definitions. To avoid the proliferation of terms, the word “thyristor”, as used in the terms of this document, is synonymous with “TSS”.

NOTE 1 IEC 60747-1, clause 2.1.1 Basic letters, states “IEC 60027 recommends the letters V and v only as reserve symbols for voltage; however, in the field of semiconductor devices, they are so widely used that in this publication they are on the same plane as U and u .” This document uses the letters V and v for voltage with the letters U and u as alternatives.

NOTE 2 Where several distinctive forms of letter symbol exist, the most commonly used form is given first.

3.2 General terms

3.2.1 information and communications technologies

ICT

group of applications using information and communications (telecommunications) technologies

[SOURCE: ISO/IEC 24704:2004, 3.1.5]

3.2.2 overcurrent

any current having a peak value exceeding the corresponding peak value of maximum steady-state current at normal operating conditions

[SOURCE: IEC 60664-2-1, ed. 2.0 (2011-01), 3.21, modified by replacing voltage with current]

3.2.3 overvoltage

any voltage having a peak value exceeding the corresponding peak value of maximum steady-state voltage at normal operating conditions

[SOURCE: IEC 60664-2-1, ed. 2.0 (2011-01), 3.21]

3.2.4 surge protective device

SPD

device that restricts the voltage of a designated port or ports, caused by a surge, when it exceeds a predetermined level

Note 1 to entry: Secondary functions may be incorporated, such as a current limiting to restrict a terminal current.

Note 2 to entry: Typically, the protective circuit has at least one non-linear voltage-limiting surge protective component.

Note 3 to entry: An SPD is a complete assembly, having terminals to connect to the circuit conductors.

[SOURCE: IEC 61643-21:2008, 3.8]

3.3 Main terminal ratings

Listed ratings cover the appropriate requirements of the blocking, conducting and switching quadrants.

3.3.1**repetitive peak off-state voltage** V_{DRM}

highest instantaneous value of the off-state voltage, including all repetitive transient voltages, but excluding all non-repetitive transient voltages

[SOURCE: IEC 60747-6:2000, 3.5.12[10]¹, modified (removal of NOTE)]

3.3.2**repetitive peak on-state current** I_{TRM}

peak value of the on-state current, including all repetitive transient currents

[SOURCE: IEC 60747-6:2000, 3.6.15[10], modified (removal of Figure)]

3.3.3**surge on-state current** I_{TSM}

on-state current pulse of short duration and specified waveshape, whose application causes or would cause the maximum rated virtual junction temperature to be exceeded, but which is assumed to occur rarely and with a limited number of such occurrences during the service life of the device and to be a consequence of unusual circuit conditions

[SOURCE: IEC 60747-6:2000, 3.6.17[10], modified (removal of "(for example, a fault) (see figure 4)")]

3.3.4**non-repetitive peak impulse current** I_{PP}

rated maximum value of peak impulse current of specified amplitude and waveshape that may be applied

3.3.5**repetitive peak reverse voltage (of a unidirectional thyristor)** V_{RRM}

highest instantaneous value of the reverse voltage, including all repetitive transient voltages, but excluding all non-repetitive transient voltages

[SOURCE: IEC 60747-6:2000, 3.5.6[10], modified (removal of NOTE)]

3.3.6**non-repetitive surge forward current** I_{FSM}

forward current pulse of short time duration and specified waveshape, whose application causes or would cause the maximum rated junction temperature to be exceeded, but which is assumed to occur rarely and with a limited number of such occurrences during the service life of the device and to be a consequence of unusual circuit conditions (for example a fault)

[SOURCE: IEC 60747-2:2000, 3.3.6[9], modified (original term did not include "non-repetitive")]

3.3.7**repetitive peak forward current (diode)** I_{FRM}

peak value of the forward current including all repetitive transient currents

¹ Numbers in square brackets refer to the bibliography.

[SOURCE: IEC 60747-2:2000, 3.3.4[9]]

3.3.8

critical rate of rise of on-state current

di_T/dt_{cr}

highest value of the rate of rise of on-state current that a thyristor can withstand without deleterious effect

[SOURCE: IEC 60747-6:2000, 3.6.23[10]]

3.4 Main terminal characteristics

3.4.1

off-state voltage

V_D

anode, principal, or thyristor voltage when the thyristor is in the off state

[SOURCE: IEC 60747-6:2000, 3.5.9[10]]

3.4.2

off-state current

I_D

anode, principal, or thyristor current when the thyristor is in the off state

[SOURCE: IEC 60747-6:2000, 3.6.26[10]]

3.4.3

peak off-state current

I_{DRM}

maximum (peak) value of off-state current that results from the application of the repetitive peak off-state voltage, V_{DRM}

3.4.4

breakover voltage

$V_{(BO)}$

voltage at the breakover point

[SOURCE: IEC 60747-6:2000, 3.5.1[10]]

3.4.5

holding current

I_H

minimum anode, principal, or thyristor current that will maintain the thyristor in the on state

[SOURCE: IEC 60747-6:2000, 3.6.25[10]]

3.4.6

off-state capacitance

C_o, C_J

differential capacitance at the specified terminals in the off-state measured at specified frequency, f , amplitude, V_d and DC bias, V_D

3.4.7

repetitive peak reverse current

I_{RRM}

maximum (peak) value of reverse current that results from the application of the repetitive peak reverse voltage, V_{RRM}

3.4.8**forward recovery voltage (diode)** V_{FRM}

varying voltage occurring during the forward recovery time after instantaneous switching from zero or a specified reverse voltage to a specified forward current

[SOURCE: IEC 60747-2:2000, 3.2.3[9]]

3.5 Additional and derived parameters

The following derived and measured parameters may be necessary or useful for comparison, certain applications or statistical process controls.

3.5.1**breakover current** $I_{(BO)}$

anode, principal, or thyristor current at the breakover point

[SOURCE: IEC 60747-6:2000, 3.6.1[10]]

3.5.2**on-state voltage** V_T

anode, principal, or thyristor voltage when the thyristor is in the on state

[SOURCE: IEC 60747-6:2000, 3.5.8[10]]

3.5.3**on-state current** I_T

anode, principal, or thyristor current when the thyristor is in the on state

[SOURCE: IEC 60747-6:2000, 3.6.9[10]]

3.5.4**forward voltage (diode)** V_F

voltage across the terminals which results from the flow of current in the forward direction

[SOURCE: IEC 60747-2:2000, 3.2.1[9]]

3.5.5**forward current (diode)** I_F

current through the device in the forward conducting state

3.6 Temperature related parameters

All the semiconductor related TSS parameters are temperature dependent. The need for temperature dependence information can often be removed by specifying that a parameter's maximum or minimum value should be valid over the intended operating temperature range. Some common temperature related terms are shown hereafter.

3.6.1**variation of holding current with temperature**

change in holding current, I_H , with changes in temperature and shown as a graph

3.6.2**temperature derating**

derating with temperature above a specified base temperature, expressed as a percentage, such as may be applied to peak pulse current

3.6.3**thermal resistance**

R_{thJL} , R_{thJC} , R_{thJA} ($R_{\theta JL}$, $R_{\theta JC}$, $R_{\theta JA}$)

effective temperature rise per unit power dissipation of a designated junction, above the temperature of a stated external reference point (lead, case or ambient) under conditions of thermal equilibrium

Note 1 to entry: Thermal resistance is usually expressed as K/W with °C/W as an alternative.

3.6.4**transient thermal impedance**

$Z_{thJL}(t)$, $Z_{thJC}(t)$, $Z_{thJA}(t)$ ($Z_{\theta JL}(t)$, $Z_{\theta JC}(t)$, $Z_{\theta JA}(t)$)

change in the difference between the virtual junction temperature and the temperature of a specified reference point or region (lead, case, or ambient) at the end of a time interval, divided by the step function change in power dissipation at the beginning of the same time interval which causes the change of temperature difference

Note 1 to entry: Thermal impedance is usually expressed as K/W with °C/W as an alternative.

Note 2 to entry: It is the thermal impedance of the junction under conditions of change and is generally given in the form of a curve as a function of the duration of an applied power pulse.

3.6.5**(virtual) junction temperature**

T_J , T_{VJ}

theoretical temperature representing the temperature of the junction(s) calculated on the basis of a simplified model of the thermal and electrical behaviour of the device

Note 1 to entry: The term “virtual-junction temperature” is particularly applicable to multijunction semiconductors and is used to denote the temperature of the active semiconductor element when required in specifications and test methods. The term “junction temperature”, T_J , is used interchangeably with the term “virtual junction temperature”, T_{VJ} , in this standard.

3.6.6**maximum junction temperature**

T_{JM}

maximum value of permissible junction temperature, due to self-heating, which a TSS can withstand without degradation

3.6.7**storage temperature range**

T_{stgmin} to T_{stgmax}

temperature range over which the device can be stored without any voltage applied

3.7 Gate terminal parameters**3.7.1****gate trigger current**

I_{GT}

lowest gate current required to switch a device from the off-state to the on-state

3.7.2**gate trigger voltage**

V_{GT}

gate voltage required to produce the gate trigger current, I_{GT}

3.7.3

gate-to-adjacent terminal peak off-state voltage

V_{GDM}

maximum gate to cathode voltage for a P-gate component or gate to anode voltage for an N-gate component that may be applied such that a specified off-state current, I_{D} , at a rated off-state voltage, V_{D} , is not exceeded

3.7.4

peak off-state gate current

I_{GDM}

maximum gate current that results from the application of the peak off-state gate voltage, V_{GDM}

3.7.5

gate reverse current, adjacent terminal open

$I_{\text{GAO}}, I_{\text{GKO}}$

current through the gate terminal when a specified gate bias voltage, V_{G} , is applied and the cathode terminal for a P-gate component or anode terminal for an N-gate component is open-circuited

3.7.6

gate reverse current, main terminals short-circuited

$I_{\text{GAS}}, I_{\text{GKS}}$

current through the gate terminal when a specified gate bias voltage, V_{G} , is applied and the cathode terminal for a P-gate component or anode terminal for an N-gate component is short-circuited to the third terminal

Note 1 to entry: This definition only applies to components with integrated series gate blocking diodes.

3.7.7

gate reverse current, on-state

$I_{\text{GAT}}, I_{\text{GKT}}$

current through the gate terminal when a specified gate bias voltage, V_{G} , is applied and a specified on-state current, I_{T} , is flowing

Note 1 to entry: This definition only applies to components with integrated series gate blocking diodes.

3.7.8

gate reverse current, forward conducting state

$I_{\text{GAF}}, I_{\text{GKF}}$

current through the gate terminal when a specified gate bias voltage, V_{G} , is applied and a specified forward conduction current, I_{F} , is flowing

Note 1 to entry: This definition only applies to conducting unidirectional components with integrated series gate blocking diodes.

3.7.9

gate switching charge

Q_{GS}

charge through the gate terminal, under impulse conditions, during the transition from the off-state to the switching point, when a specified gate bias voltage, V_{G} , is applied

3.7.10

peak gate switching current

I_{GSM}

maximum value of current through the gate terminal during the transition from the off state to the switching point, when a specified gate bias voltage, V_{G} , is applied

3.7.11**gate-to-adjacent terminal breakover voltage** $V_{GK(BO)}$, $V_{GA(BO)}$

gate-to-cathode voltage for a P-type component or gate to anode voltage for an N-gate component at the breakover point

Note 1 to entry: This is equivalent to the voltage difference between the breakover voltage, $V_{(BO)}$, and the specified gate voltage, V_G .

3.8 Abbreviated terms

AC Alternating Current

DC Direct Current

ICT Information & Communication Technology

TSS Thyristor Surge Suppressor

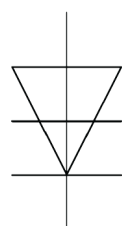
SPC Surge Protective Component

SPD Surge Protective Device

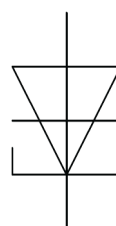
TRIAC TRIode for Alternating Current (bidirectional triode thyristor)

3.9 Circuit symbols

Thyristors can be made as two terminal components (fixed voltage) or with additional terminals connected to intermediate P or N layers (gated). In addition, they can be made with one switching quadrant or two switching quadrants. Figure 1 shows the circuit symbols for fixed voltage, one switching quadrant, two terminal TSSs based on the IEC 60617[5] S006XX series of graphical symbols for diagrams. The switching quadrant characteristic occurs when the top terminal is positive with respect to the bottom terminal (Figure 1 through Figure 3).



a) S00650



b) S00651

Figure 1 – Fixed voltage, two terminals: a) reverse blocking and b) reverse conducting

Figure 2 shows the circuit symbols for gated reverse blocking (one switching quadrant) TSSs based on the IEC 60617[5] S006XX series of graphical symbols for diagrams.

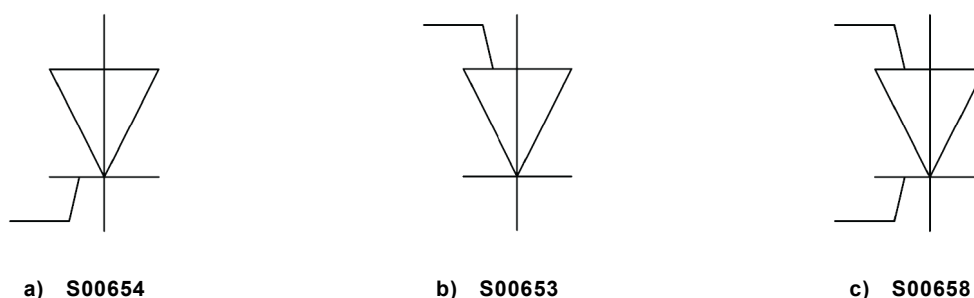


Figure 2 – Gated reverse blocking: a) P gate b) N gate and c) P & N gate

Figure 3 shows the circuit symbols for gated reverse conducting (one switching quadrant) TSSs based on the IEC 60617[5] S006XX series of graphical symbols for diagrams.



Figure 3 – Gated reverse conducting: a) P gate and b) N gate

Figure 4 shows the circuit symbols for bidirectional (two switching quadrant) TSSs based on the IEC 60617[5] S006XX series of graphical symbols for diagrams. The switching quadrant characteristic is for any top terminal polarity.



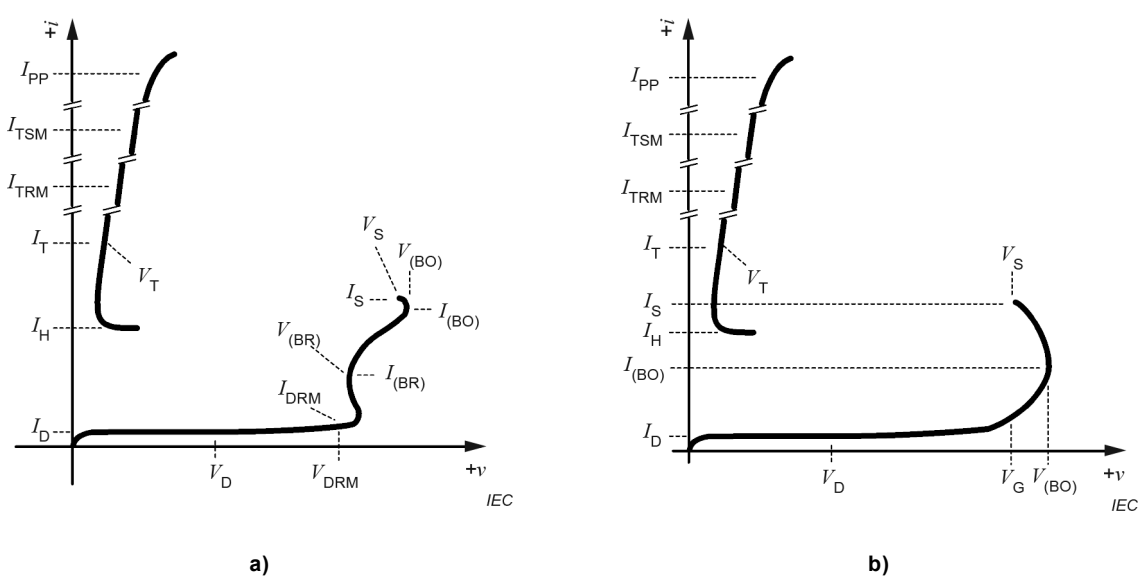
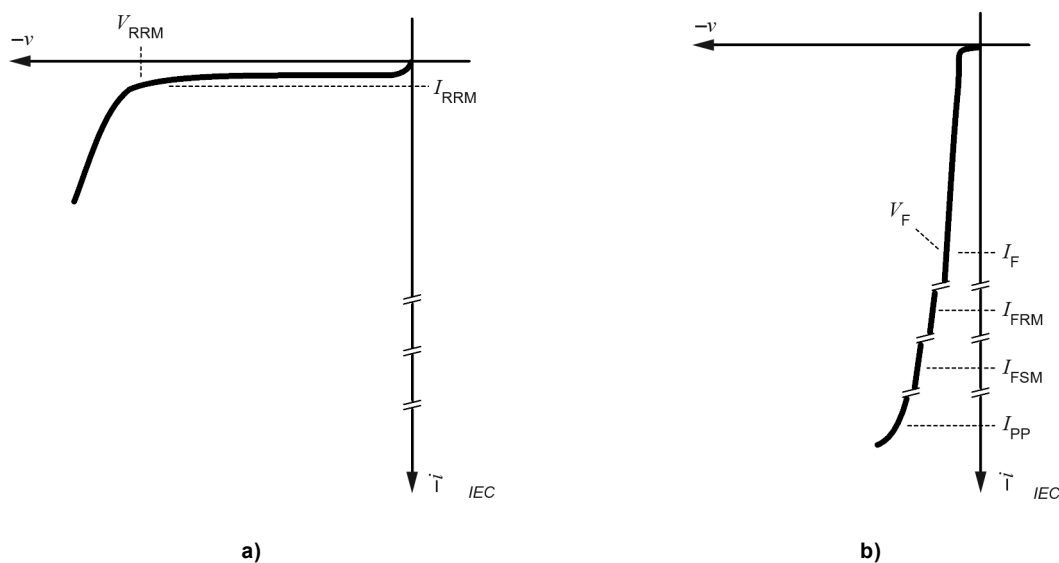
Figure 4 – Bidirectional: a) 2 terminal fixed voltage and b) gated

4 TSS types

The TSS is classified by the type of characteristic in the first and third quadrants, and the number of terminals (see Table 1). At least one quadrant will have a switching characteristic (see Figure 5). The other quadrant may have a switching, blocking or diode conduction characteristic (see Figure 5 and Figure 6). Thyristors with only one switching quadrant are called unidirectional and may have two (diode), three (triode) or four (tetraode) terminals. In addition, thyristors with two switching quadrants are called bidirectional.

Table 1 – Types of TSS

Number of terminals	Other quadrant characteristics		
	Blocking	Conducting	Switching
2 (diode)	Reverse blocking diode TSS Figure 1	Reverse conducting TSS Figure 1	Bidirectional diode TSS Figure 4
3 (triode)	Reverse blocking triode TSS P-gate or N-gate Figure 2	Reverse conducting triode TSS P-gate or N-gate Figure 3	Bidirectional triode TSS P-gate or N-gate or combined P-gate and N- gate (TRIAC) Figure 4
4 (tetraode)	Reverse blocking tetraode TSS P-gate and N-gate Figure 2		

**Figure 5 – Switching quadrant characteristics: a) fixed-voltage TSS and b) gated TSS****Figure 6 – TSS non-switching characteristics: a) reverse blocking b) reverse conducting**

5 Service conditions

5.1 Normal service conditions

The TSS is normally mounted inside an equipment or module which results in a micro-climate class condition (see IEC 60721-3-9[7]). A TSS which conforms to this document shall be suitable for stationary use at weather-protected locations (see IEC 60721-3-3[6]). In the absence of specific requirements, the TSS shall be suitable for operation under the following common service conditions and one or both of the two microclimates:

a) Normal microclimate

ambient air temperature within the range of 0 °C to 70 °C;

air pressure within the range of 80 kPa to 106 kPa;

relative humidity within the range of 25 % to 75 %.

b) Extended microclimate

ambient air temperature within the range of –40 °C to 85 °C;

air pressure within the range of 70 kPa to 106 kPa;

relative humidity 10 % to 95 %.

5.2 Storage temperature range, $T_{\text{stg min}}$ to $T_{\text{stg max}}$.

The temperatures over which the thyristor can be stored without any voltage applied has the following preferred temperature ranges (selected from IEC 60747-1[8] and IEC 60749[11])

0 °C to 125 °C

–55 °C to 125 °C

–65 °C to 150 °C

6 Mechanical requirements and identification

6.1 Robustness of terminations

If applicable, the user shall specify a suitable test from IEC 60068-2-21[3].

6.2 Solderability

Solder terminations shall meet the requirements of IEC 60068-2-20[2].

6.3 Marking

Legible and permanent marking shall be applied to the surge protective component, as necessary, to ensure that the user can determine the following information by inspection:

a) manufacturer;

b) year of manufacture;

c) component number or code.

If requested and agreed, the customer's identification should be marked on each component.

NOTE The necessary information can also be coded.

6.4 Documentation

Documents shall be provided by the manufacturer so that from the information in 6.3, the manufacturer can determine the following additional information:

a) appropriate component parameters as set out in this document;

- b) component mounting requirements and processes.
- c) ordering information

The following information should be supplied by the user:

- a) drawing giving all dimensions, finishes and termination details;
- b) type or model;
- c) quantity;
- d) quality assurance requirements.

7 Standard test methods

7.1 Failure rates

Sampling size, electrical characteristics to be tested, etc. should be covered by the quality assurance requirements, which are not covered by this document.

7.2 Test conditions

7.2.1 General

The rating and characteristic tests shall be performed on the TSS either as required by the application or as detailed in the component specification. The TSS shall be tested with the specified environmental conditions, such as temperature range and mounting configuration.

7.2.2 Standard atmospheric conditions

All room temperature electrical measurements, as well as recoveries followed by measurements, shall be carried out under the following conditions as recommended in Subclause 4.1 of IEC 60749-1:2002[11]:

- temperature: 20°C to 30°C;
- relative humidity 25 % to 75 %, where appropriate;
- air pressure 80 kPa to 106 kPa

Referee tests shall be carried out under the following standard atmospheric conditions (see 4.1 of IEC 60749-1:2002[11]):

- temperature: 24°C to 26°C;
- relative humidity 25 % to 75 %;
- air pressure 80 kPa to 106 kPa

Where the TSS parameters are tested over a temperature range, suitable values should be chosen from the list of recommended temperature values in IEC 60721-3-3:2019[6].

In the absence of special requirements, one of the following preferred semiconductor ambient temperature ranges should be used:

- normal 0 °C to 70 °C;
- extended –40 °C to 85 °C.

7.2.3 Measurement errors

Measurement errors can be caused by ground loops, common impedances, magnetic induction, electric induction and electromagnetic radiation. The voltage error caused by a circulating ground-loop current can be reduced by increasing the loop impedance. Normally this is done by clipping ferrite cores on to the probe cables. Common impedances can be avoided by using Kelvin contacts to the TSS for power and sense connections. Magnetic induction and inductive effects can be reduced by short lead lengths and minimizing the wiring loop area, possibly by using twisted wires. Electric induction (capacitive pick-up) can be removed by interposing a Faraday shield connected to a non-signal ground. Electromagnetic pick-up can be reduced by shielding and the techniques used for magnetic induction.

7.2.4 Measurement accuracy

Analogue oscilloscopes shall have rise times five times faster than the signal rise time. This ensures less than 2 % error in the displayed rise time. Digital oscilloscopes (refer to IEC 61083-1) shall have sample times at least $30/T_X$ where T_X is the time interval to be measured. A rated resolution of 0,4 % of full-scale deviation (2^{-8} full-scale deviation) or better is recommended for tests where only the impulse parameters are to be evaluated. For referee tests which require comparison of records, a rated resolution of 0,2 % of full-scale deviation (2^{-9} full-scale deviation) or better shall be used.

7.2.5 Designated impulse shape and values

The waveshape of an impulse is designated by a combination of two numbers. The first, represents the virtual front time (T_1) and the second the virtual time to half value on tail (T_2). It is written as T_1/T_2 , both in microseconds, the sign "/" having no mathematical meaning, see Annex A.

The quoted TSS current ratings are the short-circuit test generator values. Under test conditions, the actual thyristor current will be different, due to the interaction of the generator with the thyristor characteristic.

7.2.6 Multiple TSS

Where multiple TSS are packaged together, the application may simultaneously operate them. If the individual TSS parameters are significantly affected by the operation of the other TSS, then the testing shall emulate this condition as well as the single TSS operation.

7.2.7 Gated TSS testing

All fixed-voltage TSS tests shall be performed on a gated TSS to verify and determine the protection terminal performance. Gated TSS shall be tested with the appropriate values of gate bias voltage, V_{GG} , and of the network. Unless otherwise specified, the gate bias voltages used for testing shall be the maximum and minimum values of the intended application. For any tests where the gated TSS limits the voltage, the gate supply shall be low impedance (decoupled) and a TSS without internal gate blocking shall have an appropriately poled blocking diode connected directly in series with the gate terminal. When a gated TSS has been designed to give gate controlled and fixed-voltage protection, the fixed-voltage TSS tests shall also be performed with the gate open-circuited (i.e. $I_G = 0$).

7.3 Rating test procedures

7.3.1 General

The overvoltage and overcurrent test levels used shall be from one or more of the IEC and ITU-T bibliographic references cited in the bibliography. These test levels may be modified to the final equipment level by including in the test circuit any of the surge coordinating components from the equipment.