



BSI Standards Publication

Integrated circuits — EMC evaluation of transceivers

Part 5: Ethernet transceivers

National foreword

This British Standard is the UK implementation of EN IEC 62228-5:2021. It is identical to IEC 62228-5:2021.

The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors.

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(IEC 62228-5:2021)

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récepteurs - Partie 5 : Émetteurs-récepteurs
(IEC 62228-5:2021)

Integrierte Schaltungen - Bewertung der
elektromagnetischen Verträglichkeit von Sende-
Empfangsgeräten - Teil 5: Ethernet-Sende-Empfangsgerät
(IEC 62228-5:2021)

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European foreword

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The following dates are fixed:

- latest date by which the document has to be implemented at national (dop) 2022-02-28 level by publication of an identical national standard or by endorsement
- latest date by which the national standards conflicting with the (dow) 2024-05-31 document have to be withdrawn

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In the official version, for Bibliography, the following notes have to be added for the standards indicated:

CISPR 16-1-1	NOTE	Harmonized as EN IEC 55016-1-1
IEC 61000-4-2	NOTE	Harmonized as EN 61000-4-2
IEC 61000-4-4	NOTE	Harmonized as EN 61000-4-4
IEC 61000-4-5	NOTE	Harmonized as EN 61000-4-5
IEC 61967-2	NOTE	Harmonized as EN 61967-2
IEC 61967-8	NOTE	Harmonized as EN 61967-8
IEC 62132-2	NOTE	Harmonized as EN 62132-2
IEC 62132-8	NOTE	Harmonized as EN 62132-8

Annex ZA (normative)

Normative references to international publications with their corresponding European publications

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 Where an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu.

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 61967-1	-	Integrated circuits - Measurement of electromagnetic emissions - Part 1: General conditions and definitions	EN IEC 61967-1	-
IEC 61967-4	-	Integrated circuits - Measurement of electromagnetic emissions - Part 4: Measurement of conducted emissions - 1 ohm/150 ohm direct coupling method	EN IEC 61967-4	-
IEC 62132-1	-	Integrated circuits - Measurement of electromagnetic immunity - Part 1: General conditions and definitions	EN 62132-1	-
IEC 62132-4	-	Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method	EN 62132-4	-
IEC 62215-3	-	Integrated circuits - Measurement of impulse immunity - Part 3: Non-synchronous transient injection method	EN 62215-3	-
IEC 62228-1	-	Integrated circuits – EMC evaluation of transceivers – Part 1: General conditions and definitions	EN IEC 62228-1	-
ISO 10605	-	Road vehicles - Test methods for electrical disturbances from electrostatic discharge	-	-
ISO 21111-2	-	Road vehicles - In-vehicle Ethernet - Part 2: Common physical entity requirements	-	-
ISO 7637-2	-	Road vehicles - Electrical disturbances from conduction and coupling – Part 2: Electrical transient conduction along supply lines only	-	-

EN IEC 62228-5:2021 (E)

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
ISO/IEC/IEEE 8802-3	2017	Information technology - Telecommunications and information exchange between systems - Local and metropolitan area networks - Specific requirements - Part 3: Standard for Ethernet	-	-
+A1	2017		-	-
+A4	2017		-	-
EIA-198-1	-	Electronic Components Industry Association - Ceramic Dielectric Capacitors Classes I, II, III and IV	-	-

CONTENTS

FOREWORD.....	8
1 Scope.....	10
2 Normative references	10
3 Terms, definitions and abbreviated terms	11
3.1 Terms and definitions.....	11
3.2 Abbreviated terms.....	12
4 General	13
5 Test and operating conditions.....	14
5.1 Supply and ambient conditions.....	14
5.2 Test operation modes	14
5.2.1 General	14
5.2.2 Transceiver configuration for normal operation mode.....	15
5.2.3 Transceiver configuration for low power mode	15
5.3 Definition of BIN.....	15
5.4 Test configuration	16
5.4.1 General configuration for transceiver network	16
5.4.2 General configuration for single transceiver	18
5.4.3 Transceiver network tests – coupling ports and networks for conducted tests	18
5.4.4 Single transceiver tests – coupling ports and networks	21
5.5 Test communication and signals	22
5.5.1 General	22
5.5.2 Test signals for normal operation mode	22
5.5.3 Test signals for low power mode.....	23
5.6 Evaluation criteria	23
5.6.1 General	23
5.6.2 Evaluation criteria for functional operation modes.....	23
5.6.3 Evaluation criteria in unpowered condition after exposure to disturbances	24
5.6.4 Status classes	25
5.7 DUT specific information	26
6 Test and measurement.....	26
6.1 Emission of conducted RF disturbances.....	26
6.1.1 Test method	26
6.1.2 Test setup	26
6.1.3 Test procedure and parameters	27
6.2 Immunity to conducted RF disturbances.....	28
6.2.1 Test method	28
6.2.2 Test setup	28
6.2.3 Test procedure and parameters	29
6.3 Immunity to impulses	33
6.3.1 Test method	33
6.3.2 Test setup	33
6.3.3 Test procedure and parameters	34
6.4 Electrostatic Discharge (ESD).....	36
6.4.1 Test method	36
6.4.2 Test setup	36

6.4.3	Test procedure and parameters	41
7	Test report.....	43
Annex A	(normative) Ethernet test circuits	44
A.1	General.....	44
A.2	Test circuit for Ethernet transceivers for functional tests	44
A.3	Test circuit for Ethernet transceivers for ESD test	46
Annex B	(normative) Test circuit boards.....	49
B.1	Test circuit board for transceiver network configuration.....	49
B.2	Test circuit board for single transceiver configuration.....	51
Annex C	(informative) Test of Ethernet transceiver for radiated RF emission and RF immunity	53
C.1	General.....	53
C.2	General configuration for transceiver network	53
C.3	Tests	54
C.3.1	General	54
C.3.2	Emission of radiated RF disturbances.....	58
C.3.3	Immunity to radiated RF disturbances.....	59
Annex D	(informative) Examples for test limits for Ethernet transceiver in automotive application	63
D.1	General.....	63
D.2	Emission of conducted RF disturbances.....	63
D.3	Immunity to conducted RF disturbances.....	64
D.4	Immunity to impulses	68
D.5	Electrostatic discharge (ESD)	68
D.6	Emission of radiated RF disturbances	69
D.7	Immunity to radiated RF disturbances	70
Annex E	(informative) Characterization of common mode chokes for EMC evaluation of Ethernet transceivers	72
E.1	General.....	72
E.2	Test	72
E.2.1	General	72
E.2.2	S-parameter measurement mixed mode.....	73
E.2.3	ESD damage	80
E.2.4	Saturation test at RF disturbances.....	82
E.2.5	Saturation test at ESD	85
E.2.6	TDR measurement of differential mode impedance	87
Annex F	(informative) Characterization of ESD suppression devices for EMC evaluation of Ethernet transceivers	89
F.1	General.....	89
F.2	Test	90
F.2.1	General	90
F.2.2	S-parameter measurement mixed mode.....	91
F.2.3	ESD damage	97
F.2.4	ESD discharge current measurement.....	100
F.2.5	Test of unwanted clamping effect at RF immunity tests.....	104
Bibliography		108
Figure 1	– Minimum MDI interface test network (Min-BIN).....	16
Figure 2	– Standard MDI interface test network (Std-BIN).....	16

Figure 3 – Optimized MDI interface test network (Opt-BIN)	16
Figure 4 – General test configuration for tests in transceiver network for conducted tests	17
Figure 5 – General test configuration for unpowered ESD test	18
Figure 6 – Transceiver network tests – coupling ports and networks	19
Figure 7 – Coupling ports and networks for unpowered ESD tests	22
Figure 8 – Principle drawing of the maximum deviation on an I-V characteristic	25
Figure 9 – Test setup for measurement of conducted RF disturbances	27
Figure 10 – Test setup for DPI tests	29
Figure 11 – Test setup for impulse immunity tests	33
Figure 12 – Test setup for powered ESD tests – principle arrangement	36
Figure 13 – Test setup for powered ESD tests – stimulation and monitoring	37
Figure 14 – Test setup for unpowered ESD tests – principle arrangement	38
Figure 15 – Test setup for unpowered ESD tests – stimulation and monitoring for function validation pre and post ESD test	40
Figure A.1 – General drawing of the circuit diagram of test network for 100BASE-T1 and 1000BASE-T1 Ethernet transceivers for functional test using conducted test methods	45
Figure A.2 – General drawing of the circuit diagram of test network for 100BASE-TX Ethernet transceivers for functional test using conducted test methods	46
Figure A.3 – General drawing of the circuit diagram for ESD tests of Ethernet transceivers in powered mode	47
Figure A.4 – General drawing of the circuit diagram for ESD tests of Ethernet transceivers in unpowered mode	48
Figure B.1 – Example of functional conducted test board for Ethernet transceiver ICs (100BASE-T1)	49
Figure B.2 – Example of powered ESD test board for Ethernet transceivers ICs (100BASE-T1)	50
Figure B.3 – Example of unpowered ESD test board for Ethernet transceivers ICs (100BASE-T1), top layer	51
Figure B.4 – Example of unpowered ESD test board for Ethernet transceivers ICs (100BASE-T1), bottom layer	51
Figure C.1 – General test configuration for tests in transceiver network used for radiated tests	53
Figure C.2 – General drawing of the circuit diagram of test network for 100BASE-T1 and 1000BASE-T1 Ethernet transceivers for functional test using radiated RF test methods	55
Figure C.3 – Example of functional radiated test board for Ethernet transceiver ICs (100BASE-T1), top layer (DUT side)	56
Figure C.4 – Example of functional radiated test board for Ethernet transceiver ICs (100BASE-T1), bottom layer (external circuitry side)	57
Figure C.5 – Test setup for measurement of radiated RF emission	58
Figure C.6 – Test setup for radiated RF immunity tests	60
Figure D.1 – Example of limits for conducted RF emission – MDI Opt-BIN, V_{BAT} and WAKE	63
Figure D.2 – Example of limits for conducted RF emission – local supplies	64
Figure D.3 – Example of limits for conducted RF immunity for functional status class A _{IC} – MDI Opt-BIN	65

Figure D.4 – Example of limits for conducted RF immunity for functional status class A_{IC} – V_{BAT} and WAKE.....	65
Figure D.5 – Example of limits for conducted RF immunity for functional status class C_{IC} or D_{IC} – MDI Opt-BIN	67
Figure D.6 – Example of limits for conducted RF immunity for functional status class C_{IC} or D_{IC} – V_{BAT} and WAKE	67
Figure D.7 – Example of limits for radiated RF emission for IC stripline with 6,7 mm active conductor height.....	69
Figure D.8 – Example of limits for radiated RF immunity	70
Figure E.1 – General electrical drawing of a CMC	72
Figure E.2 – Test setup for S-parameter measurements at CMC.....	73
Figure E.3 – Example of test board 4-port S-parameter measurement at CMC – mixed mode, top layer.....	74
Figure E.4 – Example of test board 3-port S-parameter measurement at CMC – single ended, top layer.....	74
Figure E.5 – Recommended characteristics for S_{dd11} , S_{dd22} (RL) for CMC.....	77
Figure E.6 – Recommended characteristics for S_{dd21} (IL) for CMC.....	78
Figure E.7 – Recommended characteristics for S_{cc21} (CMR) for CMC	78
Figure E.8 – Recommended characteristics for S_{dc11} , S_{dc22} (LCL) for CMC	79
Figure E.9 – Recommended characteristics for S_{sd21} , S_{sd12} (DCMR) and S_{ds21} , S_{ds12} (CDMR) for CMC	79
Figure E.10 – Test setup for ESD damage tests at CMC	80
Figure E.11 – Example of ESD test board for CMC, top layer.....	81
Figure E.12 – Test setup for RF saturation measurements at CMC	83
Figure E.13 – Example of RF saturation / S-parameter test board for CMC, top layer.....	83
Figure E.14 – Test setup for ESD saturation measurements at CMC.....	85
Figure E.15 – Example of ESD saturation test board for CMC, top layer	85
Figure E.16 – Example of ESD saturation tests results for CMC.....	87
Figure E.17 – Test setup for TDR measurement at CMC	87
Figure E.18 – Example of TDR test board for CMC, top layer.....	88
Figure F.1 – Arrangement of ESD suppression device within the 100BASE-T1 and 1000BASE-T1 MDI interface	90
Figure F.2 – Test setup for S-parameter measurements at ESD suppression device	91
Figure F.3 – Example of test board 4-port S-parameter measurement for ESD suppression device – mixed mode, top layer.....	92
Figure F.4 – Example of test board 3-port S-parameter measurement for ESD suppression device – single ended, top layer.....	92
Figure F.5 – Recommended characteristics for S_{dd11} (RL) for ESD suppression device	95
Figure F.6 – Recommended characteristics for S_{dd21} (IL) for ESD suppression device.....	95
Figure F.7 – Recommended characteristics for S_{sd21} (DCMR) for ESD suppression device	96
Figure F.8 – Test setup for ESD damage tests at ESD suppression device	97
Figure F.9 – Example of ESD test board for ESD suppression device, top layer.....	98
Figure F.10 – Test setup for ESD discharge current measurement at ESD suppression device.....	100

Figure F.11 – Example of ESD discharge current test board for ESD suppression device, top and bottom layer	101
Figure F.12 – Example of test results and recommended limits for remaining ESD discharge current after the MDI test network for ESD suppression device	103
Figure F.13 – Test setup for RF clamping test at ESD suppression device	104
Figure F.14 – Example of test board RF clamping test at suppression device, top layer	105
Figure F.15 – Recommended test power levels for RF clamping tests at ESD suppression device	107
Table 1 – Overview of measurements and tests	13
Table 2 – Supply and ambient conditions for functional operation	14
Table 3 – Definition for transceiver configuration for normal operation mode	15
Table 4 – Definition for transceiver mode configuration for low power mode	15
Table 5 – Selection recommendation of MII interfaces for transceiver network configuration	18
Table 6 – Transceiver network tests – component value definitions of coupling ports and networks	20
Table 7 – Definitions of coupling ports for unpowered ESD tests	22
Table 8 – Definition for transceiver mode configuration for normal operation mode	23
Table 9 – Evaluation criteria for Ethernet transceiver	24
Table 10 – Definition of functional status classes	25
Table 11 – Settings of the conducted RF measurement equipment	27
Table 12 – Conducted emission measurements	28
Table 13 – Specifications for DPI tests	30
Table 14 – DPI tests for functional status class A _{IC} evaluation of Ethernet transceivers	31
Table 15 – DPI tests for functional status class C _{IC} or D _{IC} evaluation of Ethernet transceivers	32
Table 16 – Specifications for impulse immunity tests	34
Table 17 – Parameters for impulse immunity test	34
Table 18 – Impulse immunity tests for functional status class A _{IC} evaluation of Ethernet transceivers	35
Table 19 – Impulse immunity tests for functional status class C _{IC} or D _{IC} evaluation of Ethernet transceivers	35
Table 20 – Specifications for ESD tests	41
Table 21 – ESD tests in powered mode for functional status class A _{IC} , C _{IC} and D _{IC} evaluation of Ethernet transceivers	42
Table 22 – ESD tests in unpowered mode for functional status class D _{IC} evaluation of Ethernet transceiver ICs	43
Table B.1 – Parameter ESD test circuit board	52
Table C.1 – Settings of the radiated RF measurement equipment	59
Table C.2 – Radiated RF emission measurements	59
Table C.3 – Specifications for radiated RF immunity tests	61
Table C.4 – Radiated RF immunity tests for functional status class A _{IC} evaluation of Ethernet transceivers	62
Table D.1 – Example of limits for conducted RF emission – test cases with recommended limit classes	64

Table D.2 – Example of limits for conducted RF immunity – test cases with recommended limit classes for functional status class A _{IC}	66
Table D.3 – Example of limits for conducted RF immunity – test cases with recommended limit classes for functional status class C _{IC} or D _{IC}	68
Table D.4 – Example of limits for impulse immunity – Class I	68
Table D.5 – Example of limits for impulse immunity – test cases with recommended limit classes for functional status class C _{IC} or D _{IC}	68
Table D.6 – Example of limits for powered and unpowered ESD tests – test cases with recommended limits for functional status class A1 _{IC} , A2 _{IC} , A3 _{IC} , C _{IC} or D _{IC}	69
Table D.7 – Example of limits for radiated RF emission – test cases with recommended limit classes	70
Table D.8 – Example of limits for radiated RF immunity – test cases with recommended limit classes	71
Table E.1 – Test procedure and parameters for 3-port test board characterization for CMC	75
Table E.2 – Test procedure and parameters for S-parameter measurements at CMC	76
Table E.3 – Required S-parameter measurements for CMC	77
Table E.4 – Test parameters for ESD damage tests at CMC	81
Table E.5 – Required ESD tests for damage for CMC	82
Table E.6 – Test procedure and parameters for RF saturation tests at CMC	84
Table E.7 – Required RF saturation tests for CMC	84
Table E.8 – Test procedure and parameters for ESD saturation tests at CMC	86
Table E.9 – Required ESD saturation tests for CMC	86
Table E.10 – ESD saturation break down voltage classes for CMC	86
Table E.11 – Test procedure and parameters for TDR measurement at CMC	88
Table E.12 – Required TDR measurements for CMC	88
Table F.1 – Specification of ESD suppression device	89
Table F.2 – Test procedure and parameters for 3-port test board characterization for ESD suppression device	93
Table F.3 – Test procedure and parameters for S-parameter measurements at ESD suppression device	94
Table F.4 – Required S-parameter measurements for ESD suppression device	94
Table F.5 – Test parameters for ESD damage tests at ESD suppression device	99
Table F.6 – Required ESD tests for damage for ESD suppression device	99
Table F.7 – Test parameters for ESD discharge current measurement at ESD suppression device	102
Table F.8 – Required current measurement for ESD suppression device	102
Table F.9 – Recommended limits for remaining ESD discharge current after the MDI test network for ESD suppression device	103
Table F.10 – Limit classes and related applied ESD test voltages	104
Table F.11 – Test procedure and parameters for RF clamping tests at ESD suppression device	106
Table F.12 – Required RF clamping tests for ESD suppression device	107

INTERNATIONAL ELECTROTECHNICAL COMMISSION

**INTEGRATED CIRCUITS –
EMC EVALUATION OF TRANSCEIVERS –****Part 5: Ethernet transceivers****FOREWORD**

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International Standard IEC 62228-5 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47A/1115/FDIS	47A/1117/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
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- amended.

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INTEGRATED CIRCUITS – EMC EVALUATION OF TRANSCEIVERS –

Part 5: Ethernet transceivers

1 Scope

This part of IEC 62228 specifies test and measurement methods for EMC evaluation of Ethernet transceiver ICs under network condition. It defines test configurations, test conditions, test signals, failure criteria, test procedures, test setups and test boards. It is applicable for transceiver of the Ethernet systems

- 100BASE-T1 according to ISO/IEC/IEEE 8802-3/AMD1;
- 100BASE-TX according to ISO/IEC/IEEE 8802-3;
- 1000BASE-T1 according to ISO/IEC/IEEE 8802-3/AMD4

and covers

- the emission of RF disturbances;
- the immunity against RF disturbances;
- the immunity against impulses;
- the immunity against electrostatic discharges (ESD).

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61967-1, *Integrated circuits – Measurement of electromagnetic emissions – Part 1: General conditions and definitions*

IEC 61967-4, *Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part 4: Measurement of conducted emissions, 1 ohm/150 ohm direct coupling method*

IEC 62132-1, *Integrated circuits – Measurement of electromagnetic immunity – Part 1: General conditions and definitions*

IEC 62132-4, *Integrated circuits – Measurement of electromagnetic immunity 150 kHz to 1 GHz – Part 4: Direct RF power injection method*

IEC 62215-3, *Integrated circuits – Measurement of impulse immunity – Part 3: Non-synchronous transient injection method*

IEC 62228-1, *Integrated circuits – EMC evaluation of transceivers – Part 1: General conditions and definitions*

ISO 10605, *Road vehicles – Test methods for electrical disturbances from electrostatic discharge*

ISO 21111-2, *Road vehicles – In-vehicle Ethernet – Part 2: Common physical entity requirements*

ISO 7637-2, *Road vehicles – Electrical disturbances from conduction and coupling – Part 2: Electrical transient conduction along supply lines only*

ISO/IEC/IEEE 8802-3:2017, *Information technology – Telecommunications and information exchange between systems – Local and metropolitan area networks – Specific requirements – Part 3: Standard for Ethernet*

ISO/IEC/IEEE 8802-3:2017/AMD1:2017, *Amendment 1 – Information technology – Telecommunications and information exchange between systems – Local and metropolitan area networks – Specific requirements – Part 3: Standard for Ethernet – Physical layer specifications and management parameters for 100 Mb/s operation over a single balanced twisted pair cable (100BASE-T1)*

ISO/IEC/IEEE 8802-3:2017/AMD4:2017, *Amendment 4 – Information technology – Telecommunications and information exchange between systems – Local and metropolitan area networks – Specific requirements – Part 3: Standard for Ethernet – Physical layer specifications and management parameters for 1 Gb/s operation over a single twisted-pair copper cable*

Electronic Components Industry Association, EIA-198-1, *Ceramic Dielectric Capacitors Classes I, II, III and IV*

3 Terms, definitions and abbreviated terms

For the purposes of this document, the terms and definitions given in IEC 61967-1, IEC 62132-1, IEC 62228-1, as well as the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- ISO Online browsing platform: available at <http://www.iso.org/obp>
- IEC Electropedia: available at <http://www.electropedia.org/>

3.1 Terms and definitions

3.1.1

100BASE-T1 transceiver

transceiver 100 Mbit/s via single balanced twisted pair, with a functionality according to ISO/IEC/IEEE 8802-3/AMD1 (100BASE-T1)

3.1.2

100BASE-TX transceiver

transceiver 100 Mbit/s via two balanced twisted pairs, with a functionality according to ISO/IEC/IEEE 8802-3(100BASE-TX)

3.1.3

1000BASE-T1 transceiver

transceiver 1000 Mbit/s via single balanced twisted pair, with a functionality according to ISO/IEC/IEEE 8802-3/AMD4 (1000BASE-T1)

3.1.4

global pin

pin that carries a signal or power, which enters or leaves the application board without any active component in between

3.1.5

local pin

pin that carries a signal or power, which does not leave the application board

3.1.6

mandatory components

pl

components needed for proper function and/or technical requirement of IC as specified by the IC manufacturer

3.1.7

switch

IC with integrated Ethernet transceivers and switch functionality as defined in ISO/IEC/IEEE 8802-3

3.2 Abbreviated terms

ASIC	Application specific integrated circuit
BIN	Bus interface network
BIST	Built in self-test
CMC	Common mode choke
CDMR	Common to differential mode conversion ratio
CMR	Common mode rejection
DCMR	Differential to common mode conversion ratio
DPI	Direct RF power injection
DTT	Data transfer test
DUT	Device under test
FPGA	Field programmable gate array
GMII	Gigabit media independent interface
GPIO	General purpose input or output
IL	Insertion loss
INH	Inhibit
LCL	Longitudinal conversion loss
LPF	Low pass filter
MDI	Medium dependent interface
MII	Media independent interface
PCB	Printed circuit board
PRBS	Pseudo random bit stream
PHY	Ethernet single transceiver
RGMII	Reduced gigabit media independent interface
RL	Return loss
RS-FEC	Reed Solomon forward error correction
SBC	System base chip
SGMII	Serial gigabit media independent interface
SNR	Signal-to-noise ratio
S-parameter	Scattering parameter
SQI	Signal quality indicator
TDR	Time domain reflectometry

TLP Transmission line pulse
VNA Vector network analyzer

4 General

The intention of this document is to evaluate the EMC performance of Ethernet transceivers under application conditions in a minimal network.

The evaluation of the EMC characteristics of Ethernet transceivers shall be performed for the implemented functional operation modes as defined in Table 1 under network condition for conducted RF emission and RF immunity tests and impulse immunity tests and on a single transceiver IC for electrostatic discharge tests.

The aim of these tests is to determine the EMC performance on dedicated pins of the Ethernet transceiver which are considered as EMC relevant in the application. For an Ethernet transceiver, these pins are global pins like MDIP, MDIN, V_{BAT} and WAKE as well as local pins like power supply inputs (V_{DDX}). The global pin WAKE is given as an example and represents any global pin other than MDI and voltage supply V_{BAT} .

If the DUT includes additional product specific EMC relevant pins (functions), it shall be tested as well. The test conditions and failure validation criteria shall be adapted to the definitions for the standard functionality of Ethernet transceivers.

The test methods used for the EMC characterization are based on the international standards for IC EMC tests and are described in Table 1.

Table 1 – Overview of measurements and tests

Configuration	Test	Test method	Evaluation	Functional operation mode
Transceiver network	RF conducted emission (EMI)	150 Ω direct coupling (IEC 61967-4)	Spectrum	Normal
	RF conducted immunity (RF)	DPI (IEC 62132-4)	Function	Normal
				Low power
	Impulse immunity (IMP)	Non-synchronous transient injection (IEC 62215-3)	Function	Normal
	ESD powered	Contact discharge (ISO 10605)	Function	Normal
				Low power
Single transceiver	ESD unpowered	Contact discharge (ISO 10605)	Damage	Unpowered

The 150 Ω direct coupling, DPI and impulse immunity test methods are chosen for the evaluation of the conducted EMC characteristic of transceivers in network condition. These three test methods are based on the same approach using conductive coupling. Therefore, it is possible to use the same test board for all tests in functional operation mode, which reduces the effort and increases the reproducibility and comparability of test results.

Powered ESD test will be performed using the same approach of testing the Ethernet transceiver under network conditions but a modified test board is used because of RF and ESD tests cannot be combined on one test board if all specific test conditions of each test method should be covered.

The unpowered ESD test is performed on a separate test board with a single transceiver.

All measurements and tests should be done according to the general drawings of schematics given in Annex A with soldered transceivers on special test boards as described in Annex B to ensure application like conditions and avoid setup effects by sockets. Recommended limits for Ethernet transceivers in automotive application are given in Annex D.

In general, the test definition is done for Ethernet single transceiver (PHY). Ethernet transceiver cells embedded in switches, SBCs or ASICs shall follow the test methods for PHYs, adapting test conditions and targets as necessary. Such adaptations shall be done individually for the dedicated IC but shall follow the general definitions.

If an Ethernet transceiver supports more than one Ethernet system (e.g. 100BASE-T1 and 1000BASE-T1), all tests for the implemented Ethernet systems shall be performed separately.

In order to verify filter effects on the EMC performance of Ethernet transceivers, configurations with different bus interface networks for MDI are defined in this document. In consequence the frequency characteristic of these filter elements shall be taken into account for the interpretation of the test results.

5 Test and operating conditions

5.1 Supply and ambient conditions

For all tests and measurements under operating conditions, the settings are based on systems with 12 V power supply, which is the main application of Ethernet transceivers. If a transceiver is designed or targeted for other power supply voltages, the test conditions and test targets shall be adapted and documented accordingly. The defined supply and ambient conditions for functional operation are given in Table 2.

Table 2 – Supply and ambient conditions for functional operation

Parameter	Value
Voltage supply V_{BAText}	$(14 \pm 0,2) \text{ V}$ (default)
Voltage supply V_{DDx}	$V_{nominal} \pm 2 \%$
Test temperature	$(23 \pm 5) ^\circ\text{C}$

For RF emission measurements, the ambient noise floor shall be at least 6 dB below the applied target limit and documented in the test report.

For ESD tests, the requirements of ISO 10605 climatic environmental conditions shall be applied.

5.2 Test operation modes

5.2.1 General

The Ethernet transceiver shall be tested in functional operation modes and unpowered mode according to Table 1.

Depending on the transceiver the configuration for functional operation modes is controlled by hardware and/or software settings.

5.2.2 Transceiver configuration for normal operation mode

For test in normal functional operation mode, a transceiver configuration according to Table 3 shall be used.

Table 3 – Definition for transceiver configuration for normal operation mode

Topic	Content
Transceiver configuration	<ul style="list-style-type: none"> – full duplex mode with maximum data rate for DUT – automatic polarity detection enabled – transceiver configuration as specified by semiconductor manufacturer for reference application in datasheet, application note or comparable documentation (to be documented in the test report)

5.2.3 Transceiver configuration for low power mode

For test in low power mode a transceiver configuration according to Table 4 shall be used.

Table 4 – Definition for transceiver mode configuration for low power mode

Topic	Content
Transceiver configuration	<ul style="list-style-type: none"> – transceiver configuration as specified by semiconductor manufacturer for reference application in datasheet, application note or comparable documentation (to be documented in the test report)

5.3 Definition of BIN

For test of 100BASE-T1 and 1000BASE-T1 transceivers, the following MDI test networks (BIN) are defined:

- Minimum MDI interface network (Min-BIN):
DC blocking capacitor $C_{ac1} = C_{ac2} = 100 \text{ nF}$ as illustrated in Figure 1.
- Standard MDI interface (Std-BIN):
DC blocking capacitor $C_{ac1} = C_{ac2} = 100 \text{ nF}$ and a CMC that meet the recommendations of Annex E as illustrated in Figure 2.
- Optimized MDI interface (Opt-BIN):
DC blocking capacitor $C_{ac1} = C_{ac2} = 100 \text{ nF}$ and a CMC that meet the recommendations of Annex E, a Low pass filter (LPF) and a ESD suppression devices or terminations defined by semiconductor manufacturer as illustrated in Figure 3. The position of ESD suppression devices within the interface network can either be between transceiver and CMC and / or between C_{ac1} and C_{ac2} and MDI node.

NOTE 1 Min-BIN and Std-BIN are defined to provide data for comparison of the EMC characteristics of different Ethernet transceivers. Opt-BIN is intended to use for evaluation of EMC characteristics of the tested Ethernet transceivers.

NOTE 2 For DC blocking capacitors C_{ac1} and C_{ac2} , the capacitance $C = 100 \text{ nF}$ is set as default value for tests. Other capacitor values, defined by semiconductor manufacturer, are also possible to use.

NOTE 3 As an alternative to the DC blocking capacitors C_{ac1} and C_{ac2} in combination with a CMC, a magnetics according to ISO/IEC/IEEE 8802-3, defined by semiconductor manufacturer, is also possible to use.

NOTE 4 The characteristics of ESD suppression device can be evaluated according to the definitions of Annex F.

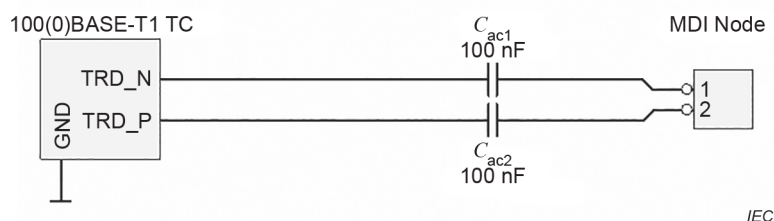


Figure 1 – Minimum MDI interface test network (Min-BIN)

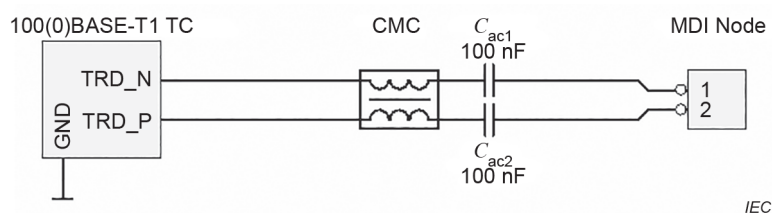


Figure 2 – Standard MDI interface test network (Std-BIN)

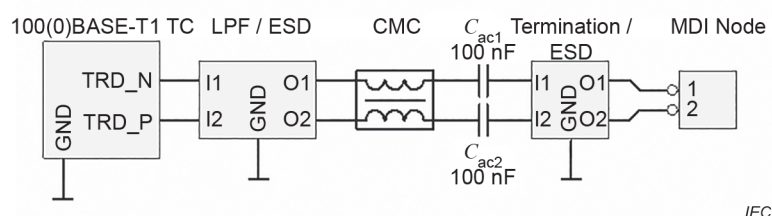


Figure 3 – Optimized MDI interface test network (Opt-BIN)

The S-parameter S_{CC21} , S_{DD21} , S_{DC21} and S_{CD21} of CMC samples used for testing may be measured or prepared by the manufacturer according to Annex E and shall be documented in the test report.

For test of 100BASE-TX transceivers, there is only an optimized MDI interface (Opt-BIN) defined. The Opt-BIN network as defined by the semiconductor manufacturer shall be used.

5.4 Test configuration

5.4.1 General configuration for transceiver network

For evaluation of conducted RF emission and RF immunity as well as impulse immunity characteristic of an Ethernet transceiver in functional operation mode, a minimal Ethernet test network consisting of two Ethernet transceivers of same type shall be used.

The test configuration in general consists of Ethernet transceivers with external mandatory components (Ethernet node) in a minimal test network, where filtered power supplies, signals, monitoring probes and coupling networks are connected as shown in Figure 4. The definitions for BIN are given in 5.3.

Both nodes are configured according to the data sheet of the semiconductor manufacturer to establish a full duplex Ethernet link. This connection is carried out as line impedance controlled PCB traces and not a wire connection.

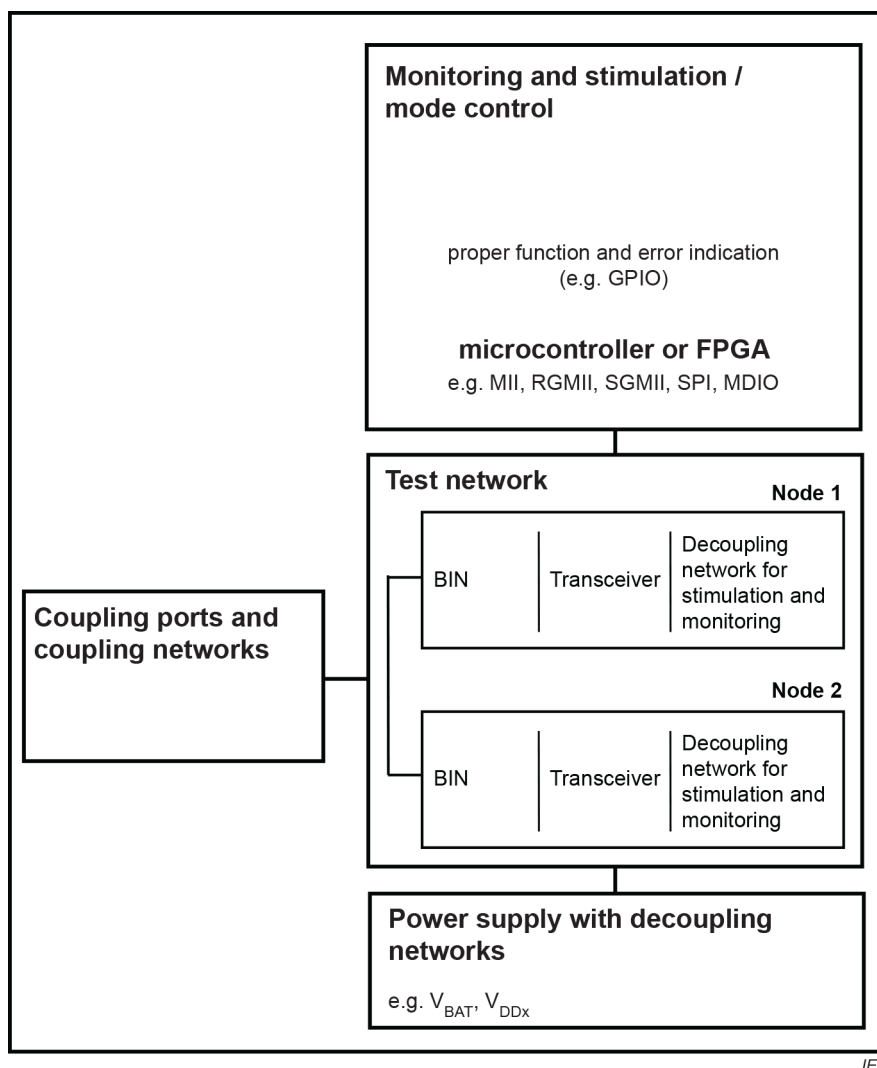


Figure 4 – General test configuration for tests in transceiver network for conducted tests

NOTE 1 In specific cases or for analyses a deviation from this setup can be agreed between the users of this document and will be noted in the test report.

The microcontroller or FPGA is used for configuring and monitoring the Ethernet transceiver and for generating a test communication. For this purpose, it should be able to operate with the communication interfaces that are supported by the tested Ethernet transceiver (e.g. MII, RGMII and SGMII).

If Ethernet transceivers support multiple MII interfaces in minimum two of them should be used for the configuration of the transceiver network. The selection recommendation is given in Table 5.

NOTE 2 Other MII interfaces e.g. RMII and GMII can be used for testing in addition but this is not required.

Table 5 – Selection recommendation of MII interfaces for transceiver network configuration

Ethernet system	MI I interface type 1	MI I interface type 2
100BASE-T1	MII	RGMII
100BASE-TX	MII	RGMII
1000BASE-T1	RGMII	SGMII

Node 1 should be configured with MII interface type 1 and node 2 with MII interface type 2. If only one interface type is implemented, both nodes are configured with the same available interface (MII or RGMII or SGMII).

In most cases, it is beneficial to use a microcontroller or FPGA per Ethernet node. The microcontroller or FPGA shall be EMC decoupled from the tested transceiver (and its EMC coupling networks) using filter networks at voltage supplies. Specific layout requirements shall be considered. A specific software implementation runs on the microcontroller or FPGA which should be adapted to the transceiver type, especially for configuration and monitoring.

If a switch or an IC with more than one integrated Ethernet transceiver (e.g. Dual PHY) shall be evaluated, each port that is intended to be used for wired Ethernet communication shall be tested separately. For that purpose, the tested port of node 1 shall be connected with the same port of node 2 (port 1 to port 1, port 2 to port 2, etc.).

General drawings of schematics with more details are given in Annex A.

5.4.2 General configuration for single transceiver

The general test configuration for unpowered ESD test of Ethernet transceivers consists of a single Ethernet transceiver with external mandatory components on a test board with discharge coupling networks as shown in Figure 5.

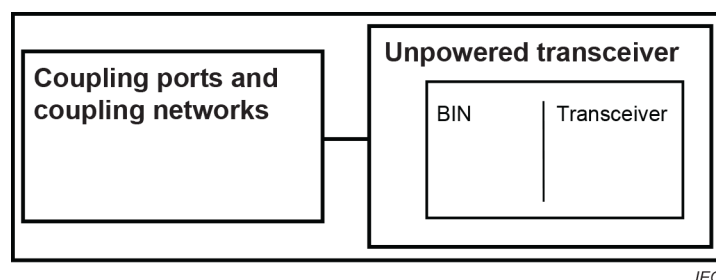
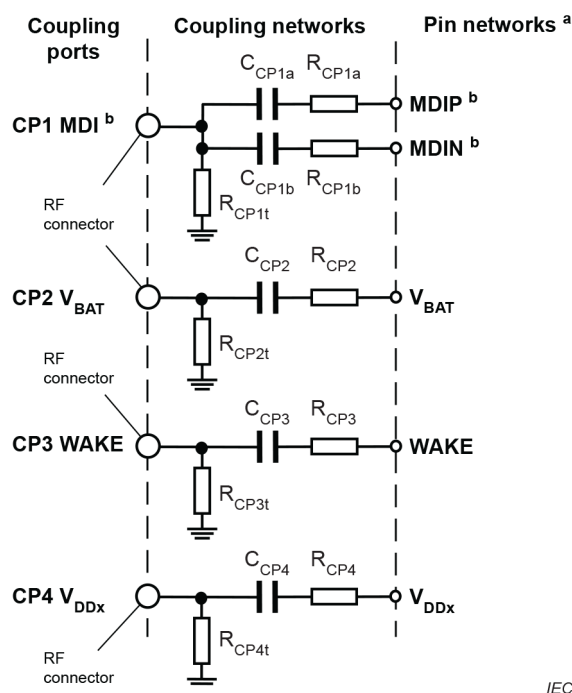


Figure 5 – General test configuration for unpowered ESD test

5.4.3 Transceiver network tests – coupling ports and networks for conducted tests

The coupling ports and coupling networks are used to transfer disturbances to or from the test network with a defined transfer characteristic. The schematic of the coupling ports, networks and pins are shown in Figure 6. The values of the components are dependent on the test method and defined in Table 6. The tolerance of the components shall be 1 % or less. For the resistors R_{CP1a} and R_{CP1b} used for symmetrical coupling, a maximum mismatch of 0,1 % is recommended.

NOTE Components can be selected by measurement of their value.



^a The pin networks include all external mandatory components for the respective pin or pins.

^b The pins MDIP and MDIN represent all pins of the transceiver that are connected to the MDI of 100BASE-T1 and 1000BASE-T1 transceivers. For 100BASE-TX transceivers a second MDI coupling network is required for testing the second path of the Ethernet link.

Figure 6 – Transceiver network tests – coupling ports and networks

Table 6 – Transceiver network tests – component value definitions of coupling ports and networks

Port	Type	Purpose	Component		
			$R_{CP1..4}$	$C_{CP1..4}$	$R_{CP1..4t}$
CP1	EMI1	RF symmetrical emission measurement on MDI	$R_{CP1a} = 120 \Omega$ $R_{CP1b} = 120 \Omega$	$C_{CP1a} = 470 \text{ pF}$ $C_{CP1b} = 470 \text{ pF}$	$R_{CP1t} = 51 \Omega$
	EMI1a	RF asymmetric emission measurement on MDI (+ 1,25 %)	$R_{CP1a} = 121 \Omega$ $R_{CP1b} = 119,5 \Omega$	$C_{CP1a} = 470 \text{ pF}$ $C_{CP1b} = 470 \text{ pF}$	$R_{CP1t} = 51 \Omega$
	EMI1b	RF asymmetric emission measurement on MDI (- 1,25 %)	$R_{CP1a} = 119,5 \Omega$ $R_{CP1b} = 121 \Omega$	$C_{CP1a} = 470 \text{ pF}$ $C_{CP1b} = 470 \text{ pF}$	$R_{CP1t} = 51 \Omega$
	EMI1c	RF asymmetric emission measurement on MDI (+ 2,5 %)	$R_{CP1a} = 121 \Omega$ $R_{CP1b} = 118 \Omega$	$C_{CP1a} = 470 \text{ pF}$ $C_{CP1b} = 470 \text{ pF}$	$R_{CP1t} = 51 \Omega$
	EMI1d	RF asymmetric emission measurement on MDI (- 2,5 %)	$R_{CP1a} = 118 \Omega$ $R_{CP1b} = 121 \Omega$	$C_{CP1a} = 470 \text{ pF}$ $C_{CP1b} = 470 \text{ pF}$	$R_{CP1t} = 51 \Omega$
	EMI1e	RF asymmetric emission measurement on MDI (+ 5 %)	$R_{CP1a} = 121 \Omega$ $R_{CP1b} = 115 \Omega$	$C_{CP1a} = 470 \text{ pF}$ $C_{CP1b} = 470 \text{ pF}$	$R_{CP1t} = 51 \Omega$
	EMI1f	RF asymmetric emission measurement on MDI (- 5 %)	$R_{CP1a} = 115 \Omega$ $R_{CP1b} = 121 \Omega$	$C_{CP1a} = 470 \text{ pF}$ $C_{CP1b} = 470 \text{ pF}$	$R_{CP1t} = 51 \Omega$
	RF1	RF symmetrical coupling for immunity test on MDI	$R_{CP1a} = 120 \Omega$ $R_{CP1b} = 120 \Omega$	$C_{CP1a} = 470 \text{ pF}$ $C_{CP1b} = 470 \text{ pF}$	not used
	RF1a	RF asymmetrical coupling for immunity test on MDI (+ 1,25 %)	$R_{CP1a} = 121 \Omega$ $R_{CP1b} = 119,5 \Omega$	$C_{CP1a} = 470 \text{ pF}$ $C_{CP1b} = 470 \text{ pF}$	not used
	RF1b	RF asymmetrical coupling for immunity test on MDI (- 1,25 %)	$R_{CP1a} = 119,5 \Omega$ $R_{CP1b} = 121 \Omega$	$C_{CP1a} = 470 \text{ pF}$ $C_{CP1b} = 470 \text{ pF}$	not used
	RF1c	RF asymmetrical coupling for immunity test on MDI (+ 2,5 %)	$R_{CP1a} = 121 \Omega$ $R_{CP1b} = 118 \Omega$	$C_{CP1a} = 470 \text{ pF}$ $C_{CP1b} = 470 \text{ pF}$	not used
	RF1d	RF asymmetrical coupling for immunity test on MDI (- 2,5 %)	$R_{CP1a} = 118 \Omega$ $R_{CP1b} = 121 \Omega$	$C_{CP1a} = 470 \text{ pF}$ $C_{CP1b} = 470 \text{ pF}$	not used
	RF1e	RF asymmetrical coupling for immunity test on MDI (+ 5 %)	$R_{CP1a} = 121 \Omega$ $R_{CP1b} = 115 \Omega$	$C_{CP1a} = 470 \text{ pF}$ $C_{CP1b} = 470 \text{ pF}$	not used
	RF1f	RF asymmetrical coupling for immunity test on MDI (- 5 %)	$R_{CP1a} = 115 \Omega$ $R_{CP1b} = 121 \Omega$	$C_{CP1a} = 470 \text{ pF}$ $C_{CP1b} = 470 \text{ pF}$	not used
	IMP1	Impulse coupling on MDI	$R_{CP1a} = 120 \Omega$ $R_{CP1b} = 120 \Omega$	$C_{CP1a} = 470 \text{ pF}$ $C_{CP1b} = 470 \text{ pF}$	not used
	ESD1 IND	Indirect ESD coupling on MDIP, MDIN ^a	$R_{CP1a} = 120 \Omega$ $R_{CP1b} = 120 \Omega$	$C_{CP1a} = 33 \text{ pF}$ $C_{CP1b} = 33 \text{ pF}$	$R_{CP1t} = 220 \text{ k}\Omega$ ^b
CP2	EMI2	RF emission measurement on V_{BAT}	$R_{CP2} = 120 \Omega$	$C_{CP2} = 6,8 \text{ nF}$	$R_{CP2t} = 51 \Omega$
	RF2	RF coupling for immunity test on V_{BAT}	$R_{CP2} = 0 \Omega$	$C_{CP2} = 6,8 \text{ nF}$	not used
	IMP2	Impulse coupling on V_{BAT}	$R_{CP2} = 0 \Omega$	Shorted	not used
CP3	EMI3	RF emission measurement on WAKE	$R_{CP3} = 120 \Omega$	$C_{CP3} = 6,8 \text{ nF}$	$R_{CP3t} = 51 \Omega$
	RF3	RF coupling for immunity test on WAKE	$R_{CP3} = 0 \Omega$	$C_{CP3} = 6,8 \text{ nF}$	not used
	IMP3	Impulse coupling on WAKE	$R_{CP3} = 0 \Omega$	$C_{CP3} = 1,0 \text{ nF}$	not used

Port	Type	Purpose	Component		
			$R_{CP1..4}$	$C_{CP1..4}$	$R_{CP1..4t}$
CP4	EMI4	RF emission measurement on V_{DDX}	$R_{CP4} = 120 \Omega$	$C_{CP4} = 6,8 \text{ nF}$	$R_{CP4t} = 51 \Omega$
<p>The parasitic inductance value of all resistors and capacitors used for RF emission and immunity coupling networks shall be less than 2 nH.</p> <p>R_{CP1a} and R_{CP1b} can be combined out of two resistors of the same type.</p> <p>^a All used resistors of the ESD coupling network shall be specified as ESD-robust up to the maximum used discharge voltage level. The specified peak voltage of used capacitors shall be at least 3 kV. The value for the coupling capacitance is estimated related to the test setup for indirect ESD test defined in ISO 10605.</p> <p>^b The resistor R_{CP1t} is used optional to avoid static pre-charge of discharge point caused by the ESD generator. A spark over at these resistors at high test levels shall be avoided. If a static pre-charge is prevented by the ESD generator construction, these resistors are not needed. Alternatively, an external resistor can be used to remove pre-charges of each discharge point before each single test.</p>					

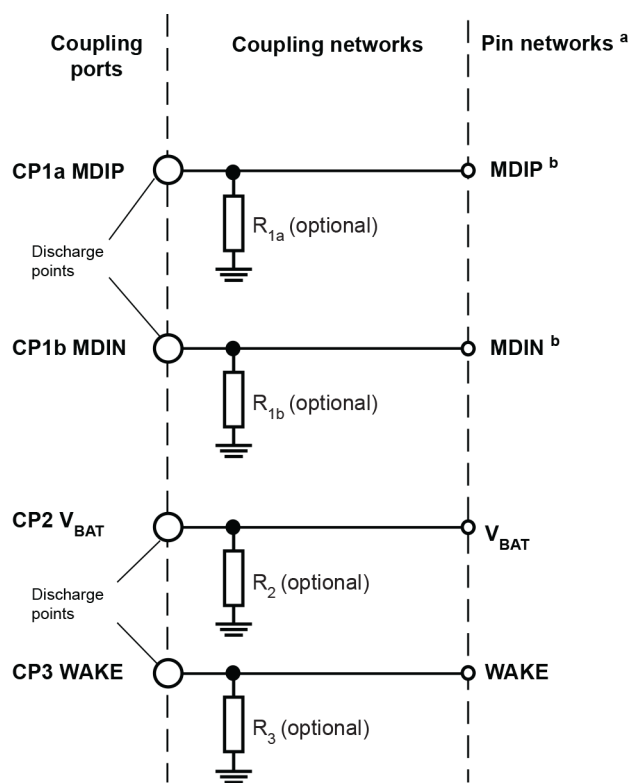
The test configurations with coupling ports and coupling networks connected to the Ethernet test network are given in the general drawing of schematics in Figure A.1.

The characterization of the coupling ports and coupling networks is carried out as follows:

The magnitude of insertion losses (S_{21} measurement) between the ports (CP1 to CP4) and the inputs of the respective transceiver pin network on the test board shall be measured and documented in the test report. The connection of signal pads using 50 Ω coaxial probe directly and ground connection shall be as short as possible. For this characterization the coupling port shall be configured for RF immunity or emission test and the Ethernet transceivers with all components of the MDI test network (BIN) shall be removed. All other components which are directly connected to the coupling port (e.g. filter to power supply or loads) remain on the test board.

5.4.4 Single transceiver tests – coupling ports and networks

The discharge points are connected by the coupling networks to the Ethernet transceiver test circuitry. The schematic and definitions of the coupling ports, networks and pins used for unpowered ESD tests are given in Figure 7 and Table 7.



^a The pin networks include all external mandatory components and for the respective pin or pins.

^b The pins MDIP and MDIN represent all pins of the transceiver that are connected to the MDI of 100BASE-T1 and 1000BASE-T1 transceivers. For 100BASE-TX transceivers a second MDI coupling network is required for testing the second path of the Ethernet link.

Figure 7 – Coupling ports and networks for unpowered ESD tests

Table 7 – Definitions of coupling ports for unpowered ESD tests

Port	Type	Purpose	Components
CP1a	ESD1a	Direct ESD coupling on MDIP	metal trace for galvanic connection ^a
CP1b	ESD1b	Direct ESD coupling on MDIN	metal trace for galvanic connection ^a
CP2	ESD2	Direct ESD coupling on V _{BAT}	metal trace for galvanic connection ^a
CP3	ESD3	Direct ESD coupling on WAKE	metal trace for galvanic connection ^a
^a The optional resistors R_{1a} , R_{1b} , R_2 and R_3 with $R \leq 220 \text{ k}\Omega$ are used to avoid static pre-charge of discharge point caused by the ESD generator. A spark over at these resistors at high test levels shall be avoided. If a static pre-charge is prevented by the ESD generator construction, these resistors are not needed. Alternatively, an external resistor can be used to remove pre-charges of each discharge point before each single test.			

5.5 Test communication and signals

5.5.1 General

Depending on the functionality of the Ethernet transceiver, different test signals are defined for communication in normal operation mode and wake-up from low power mode.

5.5.2 Test signals for normal operation mode

The communication test signal shall be used for testing Ethernet transceivers in normal operation mode. The parameters of this periodical signal are defined in Table 8.

Table 8 – Definition for transceiver mode configuration for normal operation mode

Topic	Content
Test communication	<ul style="list-style-type: none"> – data frame transmission initiated by host controller <ul style="list-style-type: none"> • Ethernet packet (e.g. ISO/IEC/IEEE 8802-3 Ethernet frame ,TCP/IP, UDP/IP...) with minimum 1000 byte data payload • minimum 80 % bus load • payload data 5A₁₆ – data frame transmission initiated by Ethernet transceiver itself (optional) <ul style="list-style-type: none"> • activation of internal BIST or PRBS test with maximum possible performance

5.5.3 Test signals for low power mode

Tests of unwanted wake-up will be performed without test signal.

For test of wanted wake-up in low power mode, the definition of test communication in normal operation mode is used for initiate the wanted wake-up event for the DUT. Depending on the transceiver type, specific definitions for wanted wake-up events may exist. In this case, the definition of the semiconductor manufacturer is used.

5.6 Evaluation criteria

5.6.1 General

For immunity performance evaluation of Ethernet transceivers, different evaluation criteria are defined during and after exposure to disturbances.

The resulting functional status of the Ethernet transceiver shall be classified in status classes A_{IC}, C_{IC} or D_{IC} according to IEC 62132-1 following the definitions in 5.6.2.

5.6.2 Evaluation criteria for functional operation modes

The evaluation criteria for functional operation modes for Ethernet transceivers are defined in Table 9.

For failure monitoring, the evaluation criteria defined in Table 9 shall be used. The failure validation applies to all transceivers in the test network if not otherwise defined. As soon as a transceiver under test violates the evaluation criteria, an error event for this test case is generated. In case of monitoring analog signals, (e.g. INH output signal) the reference values depend on the transceiver under test and shall be captured in undisturbed conditions before the test. These reference signals combined with the boundary values are used to generate the failure validation masks. Deviations from the defined boundary values can be agreed and shall be noted in the test report.

Table 9 – Evaluation criteria for Ethernet transceiver

Transceiver mode	Purpose	Test signal		
			Function	Activity
Normal	Communication and cross talk	Ethernet test communication	Link	read out of register(s) for link status defined by the semiconductor manufacturer
			DTT	error check of all transferred data between the two nodes of the test network by microcontroller or FPGA or error check for BIST or PRBS test for data frame transmission initiated by Ethernet transceiver itself
			CRC	read out of available register for CRC status ^a
			SQI/SNR	read out and documentation of all available registers for indication of SQI or SNR value ^b
			RS-FEC	read out and documentation of available registers for indication of RS-FEC events ^b
			BIST or PRBS test ^c	read out of available register for status or result of BIST or PRBS tests
			other pin functions	function validation mask using maximum deviation defined by data sheet (e.g. INH)
Low power mode	unwanted wake-up	without	wake-up indication	function validation mask using maximum deviation defined by data sheet (e.g. INH)
	wanted wake-up ^d	link pulse	wake-up indication	function validation mask using maximum deviation defined by data sheet (e.g. INH)
<p>Different evaluation criteria can be agreed for special cases and shall be noted in the test report.</p> <p>^a If no read out of required error registers at the transceiver is possible, the error validation shall be implemented into the microcontroller software in comparable way.</p> <p>^b Optional function, evaluation only if function is implemented.</p> <p>^c Optional function. If a BIST or PRBS test is used instead of a data frame transmission, initiated by host controller, this evaluation replaces the CRC and DTT function.</p> <p>^d One transceiver (DUT) of the test network is configured as Slave and is set to low power mode. The second transceiver is configured as Master and will be set into normal mode for sending out link pulses to be detected as wake-up by the DUT. Only the DUT is monitored and shall wake up at least after 100 ms (see definition in ISO 21111-2).</p>				

5.6.3 Evaluation criteria in unpowered condition after exposure to disturbances

The input I-V characteristic (current versus voltage) of a pin under test to GND including mandatory components shall be measured using e.g. a semiconductor parameter analyzer. If measurements with mandatory components are not applicable they shall be removed. The test voltage range should cover or exceed the maximum voltage rating of the pin under test up to the level where e.g. break down, snap back or clamping occurs.

NOTE Commonly used test voltages are ± 50 V to ± 70 V with test current limitations of $\pm 0,5$ mA to ± 5 mA in order to avoid damage of IC during characteristic curve measurement.

Any significant change of I-V characteristic (e.g. more than ± 5 % of maximum applied test voltage or current) measured before and after the immunity test is considered as a failure. Figure 8 shows a principle drawing of the maximum deviation on an I-V characteristic.

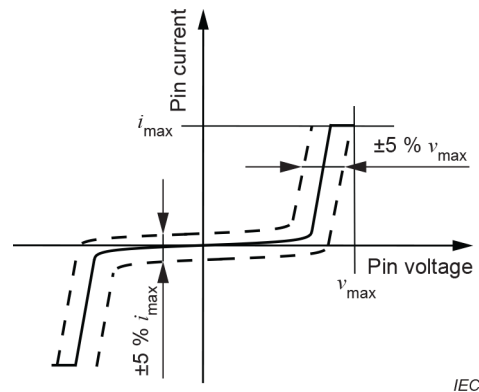


Figure 8 – Principle drawing of the maximum deviation on an I-V characteristic

Alternatively to the above described I-V characteristic test, a parameter test according to data sheet of the DUT can be used as well to verify damages of the IC.

5.6.4 Status classes

The functional status classes for Ethernet transceivers based on the evaluation criteria are defined in Table 10.

Table 10 – Definition of functional status classes

Resulting status class	Requirement
A_{IC}	<ul style="list-style-type: none"> no error occurred during exposure to disturbance, evaluation criteria of 5.6.2 for Link, DTT, CRC and other pin functions in normal mode and wake-up indication in low power mode no damage detected after exposure to disturbance, evaluation criteria of 5.6.3, that can be checked at the end of all functional tests
$A1_{IC}$	<ul style="list-style-type: none"> no error occurred during exposure to disturbance, evaluation criteria of 5.6.2 for Link
$A2_{IC}$	<ul style="list-style-type: none"> no error occurred during exposure to disturbance, evaluation criteria of 5.6.2 for DTT and CRC
$A3_{IC}$	<ul style="list-style-type: none"> no error occurred during exposure to disturbance, evaluation criteria of 5.6.2 for unwanted wake-up caused by ESD discharges during exposure, proper wake-up functionality and correct change into normal mode on request during exposure
C_{IC}	<ul style="list-style-type: none"> error occurred during exposure to disturbance, evaluation criteria of 5.6.2 no error occurred after exposure to disturbance, evaluation criteria of 5.6.2, DUT automatically comes back into proper operation no damage detected after exposure to disturbance, evaluation criteria of 5.6.3
D_{IC}	<ul style="list-style-type: none"> error occurred during exposure to disturbance, evaluation criteria of 5.6.2 no error occurred after exposure to disturbance, evaluation criteria of 5.6.2, but DUT does not automatically come back into proper operation when disturbance is removed until a simple operator action (e.g. re-initialization by MDIO or SPI ($D1_{IC}$), power off/on ($D2_{IC}$)) has been done no damage detected after exposure to disturbance, evaluation criteria of 5.6.3

5.7 DUT specific information

The following information is required for setting up and conducting the EMC tests at Ethernet transceivers and shall be supported by the semiconductor manufacturer:

- test circuit for typical application of transceiver;
- software configuration data for setting the transceiver in typical application;
- detailed information for data transmission and error register read out activity.

The following additional information should be supported by the semiconductor manufacturer, if available or needed respectively:

- EMC optimized test circuit (optimized MDI test network and optimized filter or supplier specific filter at voltage supply pins);
- information for ESD protection devices;
- layout application hints or equivalent layout requirements;
- software configuration data for setting the transceiver in EMC optimized state.

6 Test and measurement

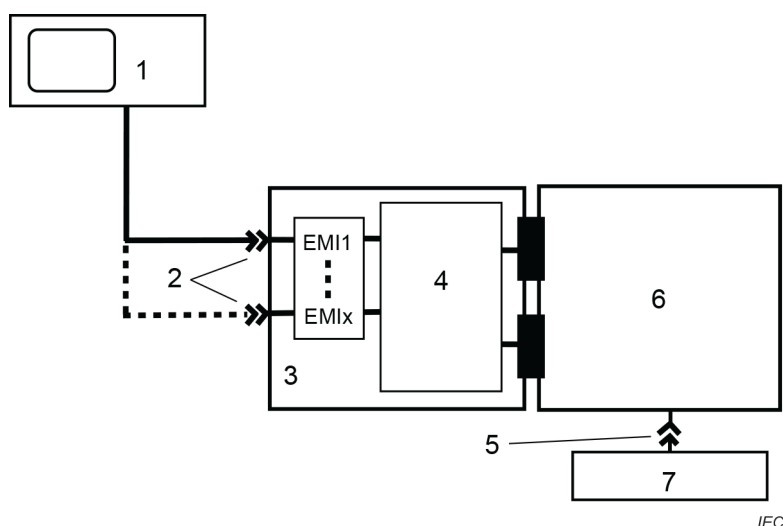
6.1 Emission of conducted RF disturbances

6.1.1 Test method

The measurement of the conducted RF emission shall be performed by 150 Ω direct coupling method according to IEC 61967-4.

6.1.2 Test setup

The conducted RF emission measurement of transceiver shall be carried out using a setup according to Figure 9 with the coupling network as defined in Table 6.



Key

1	Spectrum analyzer / EMI receiver	5	Connector
2	Coupling ports (MDI: EMI1, V_{BAT} : EMI2, WAKE: EMI3, V_{DDx} : EMIx), coaxial connector	6	Controller board
3	Test board	7	Power supply (V_{BAText} , V_{DDx_ext} , GND)
4	Test network		

Figure 9 – Test setup for measurement of conducted RF disturbances

The test equipment definitions are the following:

- spectrum analyzer / EMI receiver;
- test board;
- controller board;
- power supply.

6.1.3 Test procedure and parameters

The settings of the conducted RF measurement equipment are given in Table 11.

Table 11 – Settings of the conducted RF measurement equipment

RF Measurement equipment	Spectrum analyzer	EMI receiver
Detector	Peak	
Frequency range	0,15 MHz to 1 000 MHz (2 750 MHz optional)	
Resolution bandwidth (RBW)		
150 kHz to 30 MHz:	10 kHz	9 kHz
30 MHz to 2 750 MHz:	100 kHz	120 kHz
Video bandwidth (VBW)	≥ 3 times RBW	–
Numbers of sweeps	10 (max hold)	–
Measurement time per step	–	≥ 100 ms
Frequency sweep time	≥ 100 s	–

RF Measurement equipment	Spectrum analyzer	EMI receiver
Frequency step width		
150 kHz to 30 MHz:	–	≤ 5 kHz
30 MHz to 2 750 MHz:	–	≤ 50 kHz
FFT based EMI receivers can be used as well if they meet CISPR 16-1-1 definitions.		

The conducted RF emission measurements shall be performed according to Table 12.

Table 12 – Conducted emission measurements

Transceiver mode	Coupling port ^a	Pin	MDI test network (BIN)	Ethernet system		
				1000BASE-T1	100BASE-T1	100BASE-TX
normal mode / with Ethernet test communication	EMI1	MDI	Min-BIN	X	X	
			Std-BIN	X	X	
	Opt-BIN		X	X	X	
	Std-BIN		X			
	Opt-BIN		X			
	Std-BIN		X	X		
	Opt-BIN		X	X	X	
	Std-BIN			X		
	Opt-BIN			X	X	
	EMI2 ^b	V _{BAT}	Opt-BIN	X	X	X
	EMI3 ^b	WAKE	Opt-BIN	X	X	X
	EMI4 ^b	V _{DDx}	Opt-BIN	X	X	X

X A test shall be performed.

^a For definition of coupling ports see Table 6.

^b For transceivers with different MII interfaces emission measurements at both nodes of the transceiver network with the MII configuration according to Table 5 are required. Alternatively the MII configuration for one node can be changed between the two defined MII interfaces for emission measurement.

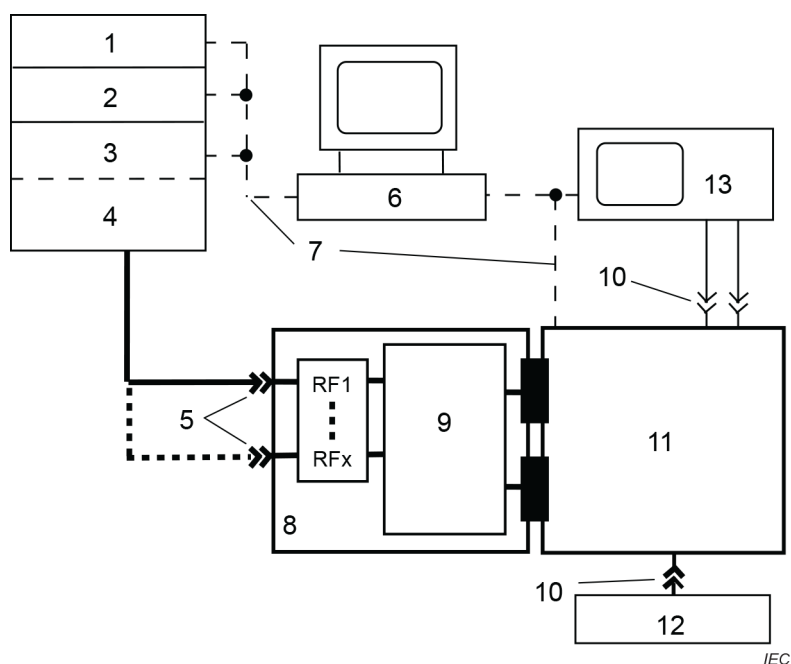
6.2 Immunity to conducted RF disturbances

6.2.1 Test method

The test of the conducted RF immunity shall be performed by using the DPI test method according to IEC 62132-4.

6.2.2 Test setup

The conducted RF immunity tests of transceiver shall be carried out using a setup according to Figure 10 with the coupling network as defined in Table 6.

**Key**

1	RF generator	8	Test board
2	RF amplifier	9	Test network
3	RF power meter	10	Connector
4	Directional coupler	11	Controller board
5	Coupling ports (MDI: RF1, V_{BAT} : RF2, WAKE: RF3), coaxial connector	12	Power supply (V_{BAText} , V_{DDx_ext} , GND)
6	Control PC (optional)	13	DSO
7	Remote control (optional)		

Figure 10 – Test setup for DPI tests

The test equipment definitions are the following:

- RF generator;
- RF amplifier (output power $P \geq 10$ W);
- power meter with directional coupler;
- test board;
- controller board;
- power supply;
- control PC (optional);
- digital storage oscilloscope (DSO, optional).

6.2.3 Test procedure and parameters

To determine the conducted RF immunity of the Ethernet transceiver, tests with the parameters given in Table 13 shall be carried out.

Table 13 – Specifications for DPI tests

Item	Parameter	
Frequency	Range	Step
	1 MHz to 10 MHz	0,25 MHz
	10 MHz to 100 MHz	1 MHz
	100 MHz to 200 MHz	2 MHz
	200 MHz to 400 MHz	4 MHz
	400 MHz to 1 000 MHz (2 000 MHz optional) ^a	10 MHz
Minimum forward power	10 dBm (10 mW)	
Maximum forward power	39 dBm (8 W)	
Power step size	0,5 dB	
Dwell time	1 s	
Modulation (including optional frequency ranges)	$f = 1 \text{ MHz to } 2\,000 \text{ MHz: CW}$ $f = 1 \text{ MHz to } 800 \text{ MHz: AM } 80 \% \text{ } 1 \text{ kHz } (\hat{P}_{PM} = \hat{P}_{CW})$ $f = 806 \text{ MHz to } 915 \text{ MHz: PM } 217 \text{ Hz, ton } 577 \text{ }\mu\text{s } (\hat{P}_{PM} = \hat{P}_{CW})$ $f = 1\,200 \text{ MHz to } 1400 \text{ MHz: PM } 300 \text{ Hz, ton } 3 \text{ }\mu\text{s } (\hat{P}_{PM} = \hat{P}_{CW})$ $f = 1\,710 \text{ MHz to } 1910 \text{ MHz: PM } 217 \text{ Hz, ton } 577 \text{ }\mu\text{s } (\hat{P}_{PM} = \hat{P}_{CW})$	
Test procedure for evaluation of functional status class A _{IC}	<p>Searching for malfunction during the complete dwell time while power is stepwise increased.</p> <p>An optimized control procedure can be used to reduce the test time but ensuring that there are no artifacts in the RF inputs during frequency or power steps.</p> <p>EXAMPLE: Procedure for each frequency step:</p> <ul style="list-style-type: none">– start with maximum forward power or with the level that caused a malfunction at the previous frequency step,– in case of malfunction at this power level reduce the power level by 6dB and repeat the test,– increase the power stepwise until a malfunction occurs or the maximum forward power is reached,– the immunity level at this frequency is the maximum forward power that causes no malfunction	
Test procedure for evaluation of functional status class C _{IC} or D _{IC}	Apply the test power for each frequency step and evaluate the functional status after each test.	
^a Test up to $f = 2000 \text{ MHz}$ is optional and only recommended for coupling to MDI of 1000BASE-T1 transceivers. In this case the requirements of IEC 62132-4 for transfer characteristic of coupling network should also be fulfilled in this frequency range. For all other configurations tests up to $f = 1\,000 \text{ MHz}$ are defined.		

The tests for functional status class A_{IC} evaluation shall be performed according to Table 14.

For each test, an immunity threshold curve with the forward power as the parameter shall be determined and documented in a diagram in the test report.