



BSI Standards Publication

High-voltage switchgear and controlgear

Part 101: Synthetic testing

National foreword

This British Standard is the UK implementation of EN IEC 62271-101:2021/AC:2021-11. It is identical to IEC 62271-101:2021/COR1:2021, incorporating corrigendum November 2021. It supersedes BS EN IEC 62271-101:2021, which is withdrawn.

The text of IEC amendment November 2021 has been provided in its entirety at the end of this document. BSI's policy of providing consolidated content remains unchanged; however, in the interest of expediency, in this instance BSI have chosen to collate the relevant content at the end of this document.

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High-voltage switchgear and controlgear

Part 101: Synthetic testing

National foreword

This British Standard is the UK implementation of EN IEC 62271-101:2021. It is identical to IEC 62271-101:2021. It supersedes BS EN 62271-101:2013+A1:2018, which will be withdrawn on 28 March 2022.

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High-voltage switchgear and controlgear - Part 101: Synthetic
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Appareillage à haute tension - Partie 101: Essais
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(IEC 62271-101:2021)

Hochspannungs-Schaltgeräte und -Schaltanlagen - Teil
101: Synthetische Prüfung
(IEC 62271-101:2021)

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European foreword

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The following dates are fixed:

- latest date by which the document has to be implemented at national (dop) 2022-05-31 level by publication of an identical national standard or by endorsement
- latest date by which the national standards conflicting with the (dow) 2024-08-31 document have to be withdrawn

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The text of the International Standard IEC 62271-101:2021 was approved by CENELEC as a European Standard without any modification.

Annex ZA (normative)

Normative references to international publications with their corresponding European publications

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 Where an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu.

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INTERNATIONAL STANDARD

NORME INTERNATIONALE



**High-voltage switchgear and controlgear –
Part 101: Synthetic testing**

**Appareillage à haute tension –
Partie 101: Essais synthétiques**

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

HIGH-VOLTAGE SWITCHGEAR AND CONTROLGEAR –

Part 101: Synthetic testing

FOREWORD

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- a) alignment with the third edition of IEC 62271-100:2021;
- b) update this document with the last methods and techniques used for synthetic tests;

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17A/1312/FDIS	17A/1315/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

This publication shall be read in conjunction with IEC 62271-100:2021, to which it refers. The numbering of the subclauses of Clause 7 is the same as in IEC 62271-100. However, not all subclauses of IEC 62271-100 are addressed; merely those where synthetic testing has introduced changes.

A list of all the parts in the IEC 62271 series, under the general title *High-voltage switchgear and controlgear*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

HIGH-VOLTAGE SWITCHGEAR AND CONTROLGEAR –

Part 101: Synthetic testing

1 Scope

This part of IEC 62271 mainly applies to AC circuit-breakers within the scope of IEC 62271-100. It provides the general rules for testing AC circuit-breakers, for making and breaking capacities over the range of test duties described in 7.102 to 7.111 of IEC 62271-100:2021, by synthetic methods.

It has been proven that synthetic testing is an economical and technically correct way to test high-voltage AC circuit-breakers according to the requirements of IEC 62271-100 and that it is equivalent to direct testing.

The methods and techniques described are those in general use. The purpose of this document is to establish criteria for synthetic testing and for the proper evaluation of results. Such criteria will establish the validity of the test method without imposing restraints on innovation of test circuitry.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 62271-100:2021, *High-voltage switchgear and controlgear – Part 100: Alternating-current circuit-breakers*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 62271-100 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

3.1

direct test

test in which the applied voltage, the current and the transient and power-frequency recovery voltages are all obtained from a circuit having a single-power source, which can be a power system or special alternators as used in short-circuit testing stations or a combination of both

3.2

synthetic test

test in which all of the current, or a major portion of it, is obtained from one source (current circuit), and in which the applied voltage and/or the recovery voltages (transient and power frequency) are obtained wholly or in part from one or more separate sources (voltage circuits)

3.3

auxiliary circuit-breaker

circuit-breaker forming part of a synthetic test circuit used to put the test circuit-breaker into the required relation with various circuits

3.4

current circuit

part of the synthetic test circuit from which all or the major part of the power-frequency current is obtained

3.5

voltage circuit

part of the synthetic test circuit from which all or the major part of the applied voltage and/or recovery voltage is obtained

3.6

prospective current

current that would flow in the circuit if each pole of the test and auxiliary circuit-breakers were replaced by a conductor of negligible impedance

Note 1 to entry: Compared with IEC 60050-441:2000, 441-17-01, the domain between brackets has been deleted. In the definition. The words "the switching device or the fuse" have been replaced by "the test and auxiliary circuit-breakers", and the Note to entry has been deleted.

3.7

actual current

current through the test circuit-breaker

Note 1 to entry: The actual current is a prospective current modified by the arc voltage of the test and auxiliary circuit-breakers.

3.8

post-arc current

current which flows through the arc gap of a circuit-breaker after the arc voltage have reached zero and the transient recovery voltage begins to rise

3.9

current injection method

synthetic test method in which the voltage circuit is applied to the test circuit-breaker before power-frequency current zero

3.10

initial transient making current

ITMC

transient current which flows through the circuit-breaker at the moment of voltage breakdown prior to the initiation of current from the current circuit during making

3.11

injected current

current supplied by the voltage circuit of a current injection circuit when it is connected to the circuit-breaker under test

3.12

voltage injection method

synthetic test method in which the voltage circuit is applied to the test circuit-breaker after power-frequency current zero

3.13**reference system conditions**

conditions of an electrical system having the parameters from which the rated and test values of IEC 62271-100 are derived

3.14**time delay of making device** t_m

time interval, during synthetic making test, between the instant of breakdown of the applied voltage and the initiation of current from the current circuit

3.15**pre-strike**

voltage breakdown between the contacts during a making operation which initiates current flow

3.16**intermediate asymmetry**

level of asymmetry in the other two phases having a reduced (intermediate) level of asymmetry when in a three-phase system the short-circuit current is initiated simultaneously in all phases and maximum asymmetry is obtained in one of the phases

3.17**rate-of-decay of dielectric strength****RDDS**

voltage withstand reduction between the contacts as a function of time or contact gap during closing

[SOURCE: IEC TR 62271-302:2010, 3.7.5, modified – The words "between the contacts" have been added after "reduction" and "of a circuit-breaker" have been deleted at the end.]

4 Synthetic testing techniques and methods for short-circuit breaking tests

4.1 Basic principles and general requirements for synthetic breaking test methods

4.1.1 General

Any particular synthetic method chosen for testing shall adequately stress the test circuit-breaker. Generally, the adequacy is established when the test method meets the requirements set forth in the following paragraphs and subclauses of 4.1, 4.2 and 4.3.

A circuit-breaker has two basic positions: closed and open. In the closed position a circuit-breaker conducts full current with negligible voltage drop across its contacts. In the open position it conducts negligible current but with full voltage across the contacts. This defines the two main stresses, the current stress and the voltage stress, which are separated in time.

If closer attention is paid to the voltage and current stresses during the interrupting process (Figure 1), three main intervals can be recognized.

- High-current interval

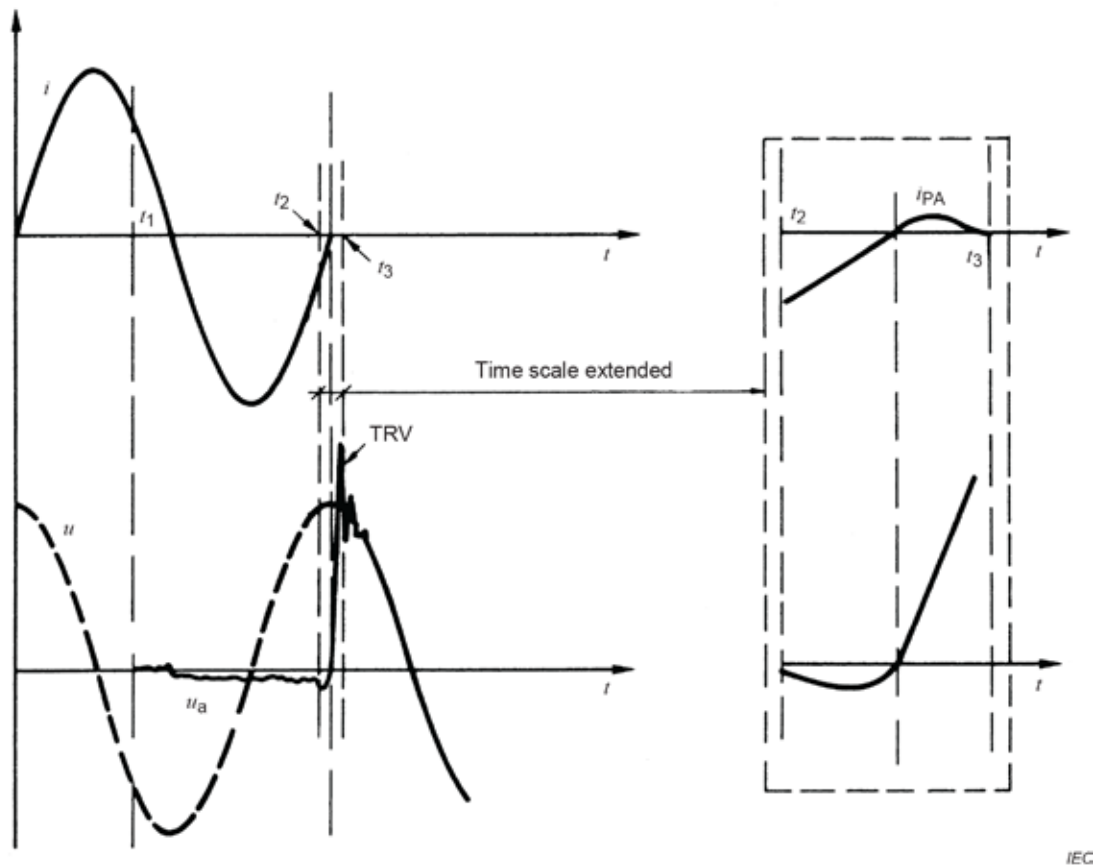
The high-current interval is the time from contact separation to the start of the significant change in arc voltage. The high-current interval precedes the interaction and high-voltage intervals.

- Interaction interval

The interaction interval is the time from the start of the significant change in arc voltage prior to current zero to the time when the current including the post-arc current, if any, ceases to flow through the test circuit-breaker (see also 14.2.4 of IEC TR 62271-306:2012/AMD1:2018).

– High-voltage interval

The high-voltage interval is the time from the moment when the current including the post-arc current, if any, ceases to flow through the test circuit-breaker to the end of the test.



Key

i	breaking current	t_2	start of significant change in arc voltage
u	power-frequency voltage	t_3	instant of cessation of post-arc current
u_a	arc voltage	$t_2 - t_1$	high-current interval
TRV	transient recovery voltage	$t_3 - t_2$	interaction interval
i_{PA}	post-arc current	After t_3	high-voltage interval
t_1	instant of contact separation		

Figure 1 – Interrupting process – Basic time intervals

4.1.2 High-current interval

The tolerance on the power-frequency of the actual breaking current is given in 7.103.2.1 of IEC 62271-100:2021. The following requirements concerning the actual current through the test circuit-breaker as shown in Table 1 shall be met.

Table 1 – Tolerances and limits required during the high-current interval

Test duty	Tolerance and limits relative to specified test values of breaking current ^a				
	At contact separation		Last loop prior to interruption		
	RMS %	DC component %	Peak value %	Duration %	Product of peak value and duration %
T10, T30, OP1, critical current test	±20	≤ 20	≥ 90	≥ 90	-
T60	±10	≤ 20	≥ 90	≥ 90	-
T100s	+5 0	≤ 20	≥ 90	≥ 90	≥ 95 ^b
T100a	±10		≤ 110 ^c ≥ 90 ^c	≤ 110 ^d ≥ 90 ^d	≤ 110 ≥ 95 ^b ≥ 90
SP, DEF	+5 0	≤ 20	≥ 90	≥ 90	
L ₉₀	+5,6 0	≤ 20	≤ 110 ≥ 95	≥ 90	≥ 95
L ₇₅	±5,3	≤ 20	≤ 110 ≥ 95	≥ 90	≥ 95
L ₆₀	±8,3	≤ 20	≤ 110 ≥ 95	≥ 90	≥ 95
OP2	+10 0	≤ 20	≥ 90	≥ 90	
^a This table lists the tolerances applicable during tests. Specified test values of breaking current, given in Annex B of IEC 62271-100:2021, are a single value excluding any tolerance. ^b Applicable only if tested with ITRV. ^c Specified peak value of breaking current multiplied by the last current loop multiplication factor given in Table E.12 to Table E.17, and Table A.7 and Table A.8. ^d Specified duration of the last current loop given in Table E.12 to Table E.17, and Table A.7 and Table A.8.					

In rare cases, where the applied voltage from the high-current circuit is of the same magnitude as the required test voltage in a direct test circuit, a higher deviation of the last current loop is accepted provided that the current loop influenced by the auxiliary circuit-breaker arcing is within the specified tolerances in Annex B of IEC 62271-100:2021.

Examples are given in 14.7 of IEC TR 62271-306:2012/AMD1:2018.

4.1.3 Interaction interval

There is no specific requirement related to the interaction interval.

See IEC TR 62271-306:2012 and IEC TR 62271:2012/AMD1:2018.

4.1.4 High-voltage interval

During the high-voltage interval, the gap of the test circuit-breaker is stressed by the recovery voltage.

The prospective TRV shall comply with the requirements of 7.105.5 of IEC 62271-100:2021.

Suitable methods for determining the prospective TRV in synthetic test circuits can be selected from Annex E of IEC 62271-100:2021.

The impedance of the voltage circuit shall be low enough to give clear evidence of breakdown, if any.

If the test circuit-breaker is fitted with opening resistors, a special procedure can be used (see Annex J).

If the TRV is obtained from more than one source, the overall waveshape should not show any appreciable discontinuity.

In principle, the power-frequency recovery voltage for the basic short-circuit test duties should preferably be AC and shall equate with the requirements of 7.103.4 of IEC 62271-100:2021. In synthetic testing, the recovery voltage is supplied from a voltage circuit, either directly or in series with the current circuit. This gives an AC voltage, or a combined AC and DC voltage, or a DC voltage, which in most cases decays due to the limited energy of the voltage circuit. It may thus not be possible to maintain the recovery voltage for at least 0,3 s as specified in 7.103.4 of IEC 62271-100:2021. Deviations from the specified recovery voltage are acceptable if the following conditions are met.

- The initial value of the power-frequency recovery voltage, excluding the transient oscillations, shall be not less than the equivalent initial value of the power-frequency recovery voltage specified in 7.103.4 of IEC 62271-100:2021 which, for a test with symmetrical current, starts with a minimum peak value of

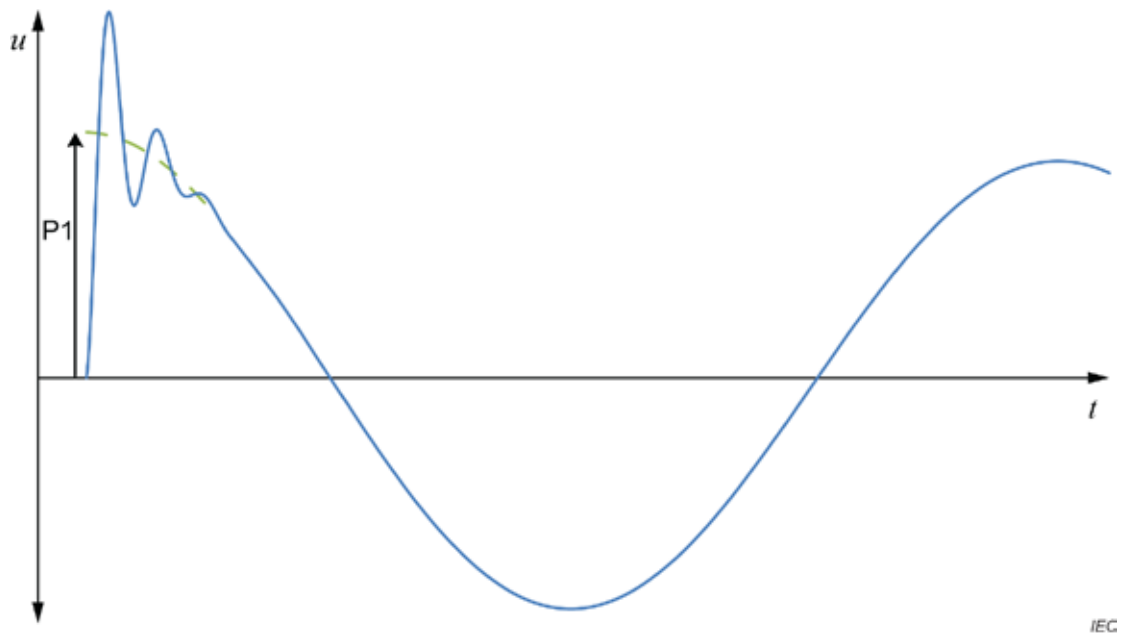
$$0,95 \times k_{pp} \times U_r \sqrt{2/3}$$

where

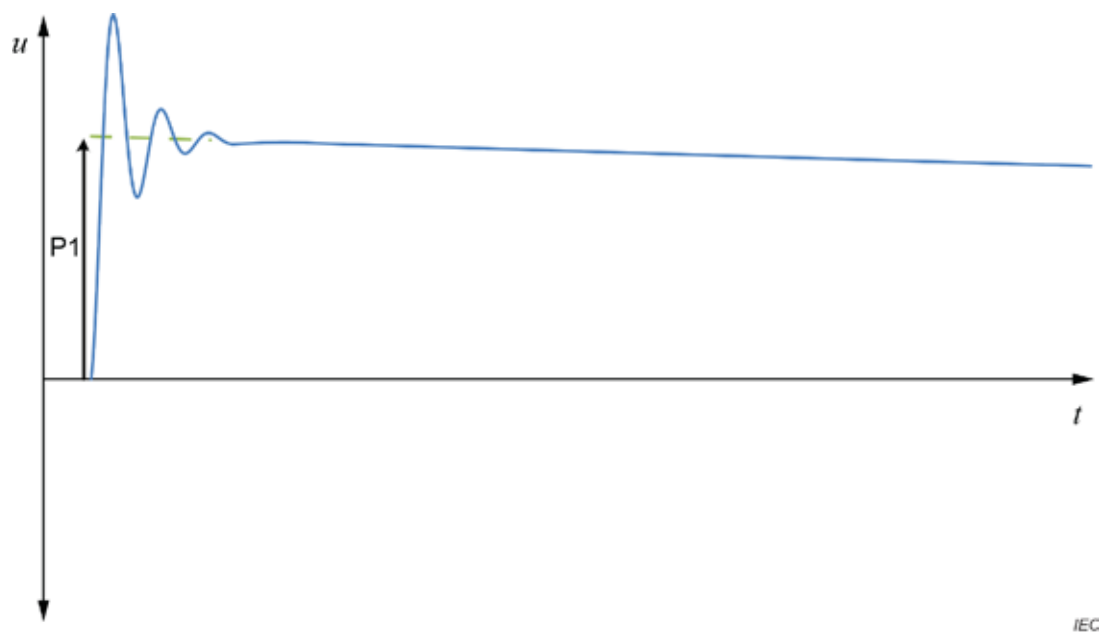
k_{pp} is the first-pole-to-clear factor;

U_r is the rated voltage of the circuit-breaker.

- Whether an exponentially decaying DC, an AC or a combined AC and DC recovery voltage is used, its instantaneous value (for DC) or its peak value (for AC or combined AC and DC) should in principle be kept as close as possible to $U_r \sqrt{2} / \sqrt{3}$ and in any case shall not fall below $0,5 U_r \sqrt{2} / \sqrt{3}$ in less than 0,1 s.
- If an exponentially decaying DC or a combined AC and DC recovery voltage imposes an inappropriate stress on the circuit-breaker compared to that due to the specified AC recovery voltage in reference system conditions, then a more appropriate circuit can be used taking into account 7.103.4 of IEC 62271-100:2021 and also the limits stated above.
- Figure 2 a) and b) gives some examples for evaluation of the recovery voltage.



a) Example of a power-frequency recovery voltage



b) Example of a DC steady state recovery voltage

Key

P1	Point of initial value of (power-frequency or DC steady-state) recovery voltage, $\geq 0,95 \times k_{pp} \times U_r \times \sqrt{\frac{2}{3}}$
Blue line	Tested recovery voltage
Green dotted line	Tested power-frequency or DC steady-state recovery voltage

Figure 2 – Examples of evaluation of initial recovery voltage

4.2 Synthetic test circuits and related specific requirements for breaking tests

4.2.1 Current injection methods

These methods can be described in terms of general principles as follows (see IEC TR 62271-306):

- the current from the voltage circuit is superimposed on the power-frequency current through the test circuit-breaker prior to the interaction interval;
- the auxiliary circuit-breaker interrupts the power-frequency current from the current circuit prior to the interaction interval.

Current injection method is mandatory for:

- short-line fault test duties;
- T100s and T100a when tested with ITRV.

Due to the lower limit of the injected current frequency of 250 Hz, it might be impossible to prepare test circuits with low RRRV (e.g. for unit test) and/or long time to peak (e.g. for high rated voltage). In this case, when current injection method is mandatory, the test can be performed using the multi-part testing method (see 7.102.4.3). The first part of the test (current zero and initial portion of TRV) shall be performed with a current injection method and the second part of the test (second part of the TRV and the RV) can be performed with a voltage injection method. For short-line fault test, it is also possible to perform the test with a test supply of limited power, as per 7.109.5 of IEC 62271-100:2021.

The time during which the arc is fed only by the injected current shall be treated as part of the length of the last loop prior to interruption.

If any device with breaking capability interrupts the current through the test circuit-breaker at the same time as the test circuit-breaker, the method is not a valid current injection method.

During the interaction interval, the test circuit-breaker is exposed to the voltage of the voltage circuit having an impedance which is representative of the reference system conditions. This explains the validity of current injection methods. Several current injection methods are known but only the conditions for parallel current injection are given below since this method is used by the majority of the test laboratories. The following conditions shall be met.

a) TRV waveshape circuit

- 1) The shape and magnitude of the prospective TRV shall comply with the specified values.
- 2) Ideally the equivalent surge impedance Z_h (see Figure 3) shall be equal to $(du/dt)/(di/dt)$ during the interaction interval. du/dt is the rate of rise of the specified transient recovery voltage and di/dt is the rate of decrease of the specified short-circuit current.
- 3) The combination of the stray and lumped capacitance C_{dh} in parallel with Z_h gives rise to the delay time $t_d = Z_h \times C_{dh}$.

b) Inductance of the voltage circuit

The value of the inductance of the voltage circuit shall be between 1,0 and 1,5 times the inductance derived from the equivalent power-frequency voltage divided by the prospective current.

c) Frequency of the injected current and the injection timing

The frequency of the injected current shall preferably be of the order of 500 Hz with a lower limit of 250 Hz and an upper limit of 1 000 Hz.

In order to prevent undue influence on the waveshape of the power-frequency current, the lower limit of the frequency of the injected current is 250 Hz.

The maximum frequency of the injected current is determined by the interval of significant change of arc voltage, the interval for which shall be smaller than the time for which the arc is fed only by the injected current. To achieve this, the period of the injected frequency should be at least four times the interval of significant change of arc voltage (see IEC TR 62271-306).

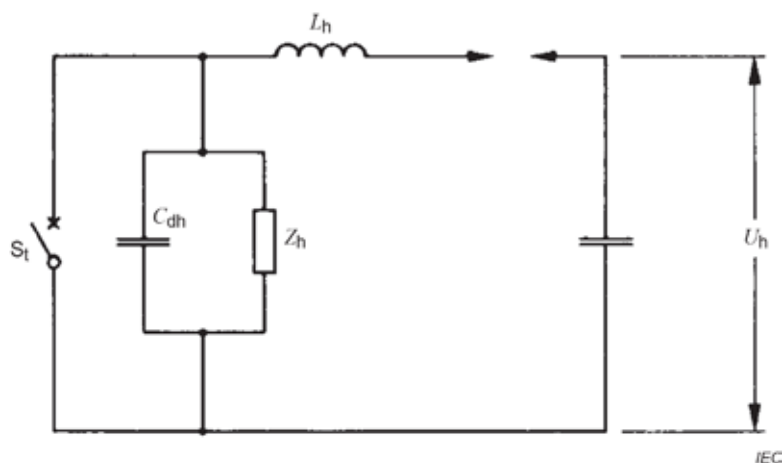
The initiation of the injected current shall be adjusted such that the time during which the test circuit-breaker is fed only by the injected current is not more than a quarter of the period of the injected current frequency with a maximum of 500 μs .

Attention should be paid to the possible overstressing of the circuit-breaker if the time that the test circuit-breaker is fed by the injected current only is less than 200 μs .

d) Waveshape of the injected current

The prospective rate of decrease (di/dt) of the injected current at current zero shall correspond to that of the prospective power-frequency current.

The injected current shall be practically free of superimposed oscillations for a time not less than 100 μs before current zero.



Key

- U_h charging voltage of voltage circuit
- L_h inductance of voltage circuit
- Z_h equivalent surge impedance
- C_{dh} capacitance for time delay of voltage circuit
- S_t test circuit-breaker

Figure 3 – Equivalent surge impedance of the voltage circuit for the current injection method

4.2.2 Voltage injection method

Several voltage injection methods are known but only series voltage injection is described here in general terms as follows (see IEC TR 62271-306):

- the voltage from the voltage circuit is applied to the test circuit-breaker after the interaction interval;
- a capacitor in parallel with the auxiliary circuit-breaker is used to apply the recovery voltage to the test circuit-breaker;
- during the high-current and interaction intervals, the test circuit-breaker is exposed to the current circuit only.

When used for tests relating to the dielectric behaviour of the circuit-breaker, the following conditions shall be met.

- The voltage circuit shall be designed in such a manner as to allow detection of re-ignitions or re-strikes, should they occur.

Therefore, the capacitance across the auxiliary circuit-breaker shall be at least 20 times the capacitance in parallel with the test circuit-breaker. Care should be taken to avoid undue distortion of the current before power-frequency current zero.

- No pause shall be introduced by the combining of the current circuit and the voltage circuit.

4.2.3 Duplicate circuit method (transformer or Skeats circuit)

This method can be described in terms of general principles as follows (see IEC TR 62271-306):

- the current and voltage are supplied from the same circuit;
- the AC recovery voltage is supplied from a step-up transformer, the primary of which is connected to the current circuit;
- the recovery voltage is applied to the test circuit-breaker through an impedance (normally a resistance).

The auxiliary circuit-breaker interrupts the current prior to the test circuit-breaker by a short time interval. During this short interval, the value of di/dt of the current in the test circuit-breaker is decreased.

The Skeats circuit can easily be adapted to supply full voltage stresses in two (or more) operations, for example at both closing and opening in a CO operation, at both openings in an O – t – CO operation or even at consecutive current zeros in an opening operation. See 14.3 of IEC TR 62271-306:2012/AMD1:2018.

4.2.4 Other synthetic test methods

Other methods may proven to be correct and advantageous for testing of circuit-breakers with specific characteristics or for testing of a circuit-breaker for specific performance. Even though these methods are not covered by this document, they can be used subject to understanding of their application and agreement between the manufacturer and the user.

4.3 Three-phase synthetic test methods

Three-phase synthetic test methods shall be applied for testing of circuit-breakers which cannot be tested single-phase as per 7.102.4.1 of IEC 62271-100:2021. They can also be used as an alternative to single phase synthetic tests if relevant. Short-circuit test sequences T10, T30 and T60 can in any case be performed in single-phase test circuits.

Annex F gives examples of three-phase test circuits.

To ensure that the appropriate stresses in the interrupting element and those between poles and, if relevant, to the enclosure are applied, the following general requirements shall be fulfilled:

- full three-phase current shall be supplied to the three-pole circuit-breaker under test;
- information about the required test circuits for test duties T100s and T100a is given in Table 2;
- the test parameters for each pole-to-clear are given in Table 3 through Table 5;
- all the above stresses preferably should be applied in the same test; if this is impossible, a multi-part testing procedure should be used;
- to avoid changing the connection of the high-voltage circuit to the circuit-breaker between the tests of each test sequence, the first-pole-to-clear is allowed to be kept in the same phase during the whole sequence, taking into account the requirements of 7.104.1 of IEC 62271-100:2021.

Table 2 – Test circuits for test duties T100s and T100a

k_{pp}	T100s		T100a	
	First-pole-to-clear	Other poles	First-pole-to-clear	Other poles
1,5	Application of synthetic circuits of 4.2.1 or 4.2.2 at all operations	Application of synthetic circuits of 4.2.1, 4.2.2 or 4.2.3 at all operations	Application of synthetic circuits of 4.2.1 or 4.2.2 for at least two operations. The third operation can be tested with 4.2.3	Application of synthetic circuit 4.2.1 or 4.2.2 at least to the operation with major extended loop and longest arcing time
1,2 or 1,3	Application of synthetic circuits of 4.2.1 or 4.2.2 for at least two operations. The third operation can be tested with 4.2.3	Application of synthetic circuits of 4.2.1 through 4.2.3 at all operations. At the second pole-to-clear at the operation with the longest arcing time application of synthetic circuits of 4.2.1 or 4.2.2 only	Application of synthetic circuits of 4.2.1 or 4.2.2 for at least two operations. The third operation can be tested with 4.2.3	Application of synthetic circuits of 4.2.1 through 4.2.3 at all other operations. At the second pole-to-clear at the operation with the major extended loop and longest arcing time application of synthetic circuits of 4.2.1 or 4.2.2 only
Key k_{pp} first-pole-to-clear factor. Voltage injection is only permitted if there are no ITRV requirements, or if these requirements are covered by SLF testing.				

Table 3 – Test parameters during three-phase interruption for test-duties T10, T30, T60 and T100s, $k_{pp} = 1,5$

TRV peak in %				Recovery voltage peak p.u.	du/dt %	di/dt %	Phase angle °
		At instant of first-pole-to-clear	At instant of second and third-pole-to-clear				
Phases	A	100	-	1	100	100	-
	B	0	58	1	70	87	90
	C	0	58	1	70	87	90
Between phases	A – B	100	58	1,732			
	B – C	0	115	1,732			
	A – C	100	58	1,732			

TRV peak first pole-to-clear: $u_c = k_{af} \times k_{pp} \times U_r \times \sqrt{2}/\sqrt{3}$ (= 100 %).

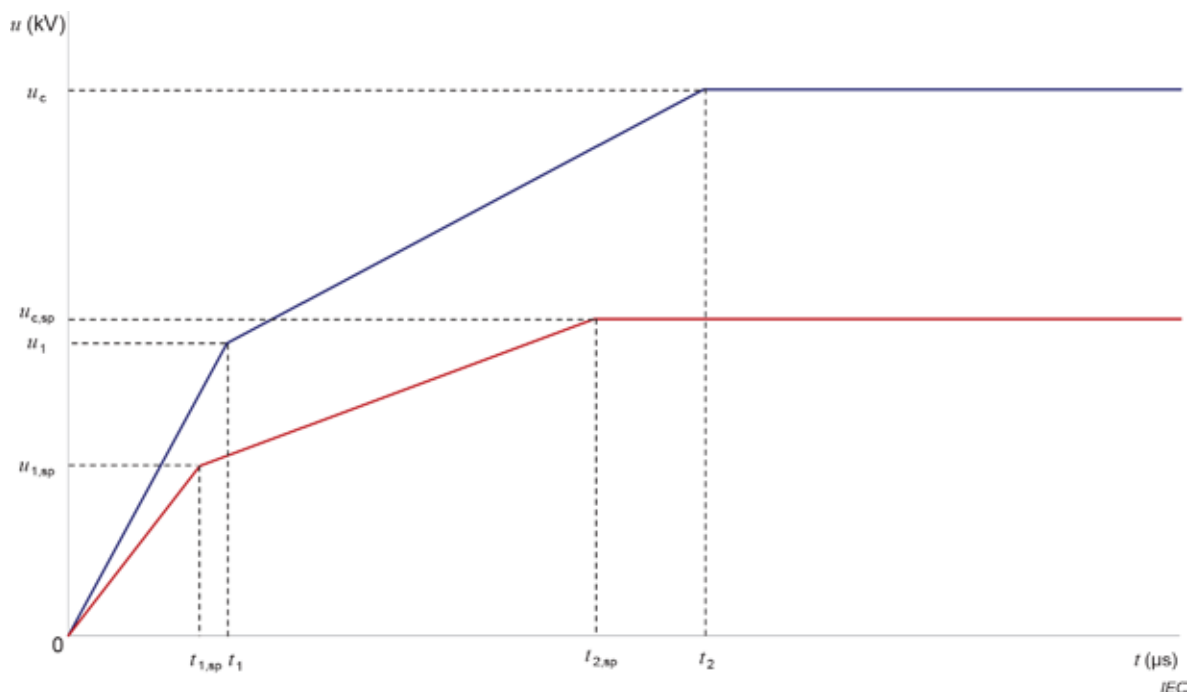
1 p.u. = $U_r \times \sqrt{2}/\sqrt{3}$.

The first-pole-to-clear is in phase A.

Test parameters are calculated based on earthing arrangements in circuits as described in IEC TR 62271-306.

TRV phases B and C for 4 parameters (see Figure 4):

- u_1 the first reference voltage is derived by applying the same reduction factor used for the TRV peak u_c .
- t_1 is derived from u_1 and the respective du/dt reduction factor.
- t_2 is derived from t_1 keeping the same ratio as for the first pole-to-clear.



Key

Blue line: first pole-to-clear

Red line: second and third pole-to-clear

Figure 4 – Reference lines of TRV with four-parameter for $k_{pp} = 1,5$

Table 4 – Test parameters during three-phase interruption for test-duties T10, T30, T60 and T100s, $k_{pp} = 1,3$

TRV peak in %				Recovery voltage peak p.u.	du/dt %	di/dt %	Phase angle °
		At instant of first-pole-to-clear	At instant of second and third-pole-to-clear				
Phases	A	100	- / -	1	100	100	-
	B	0	- / 77	1	70	57	120
	C	0	97 / -	1	95	89	77
Between phases	A – B	100	- / 91	1,732			
	B – C	0	97 / 97	1,732			
	A – C	100	89 / -	1,732			

TRV peak first pole-to-clear: $u_c = k_{af} \times k_{pp} \times U_r \times \sqrt{2}/\sqrt{3}$ (= 100 %)

1 p.u. = $U_r \times \sqrt{2}/\sqrt{3}$

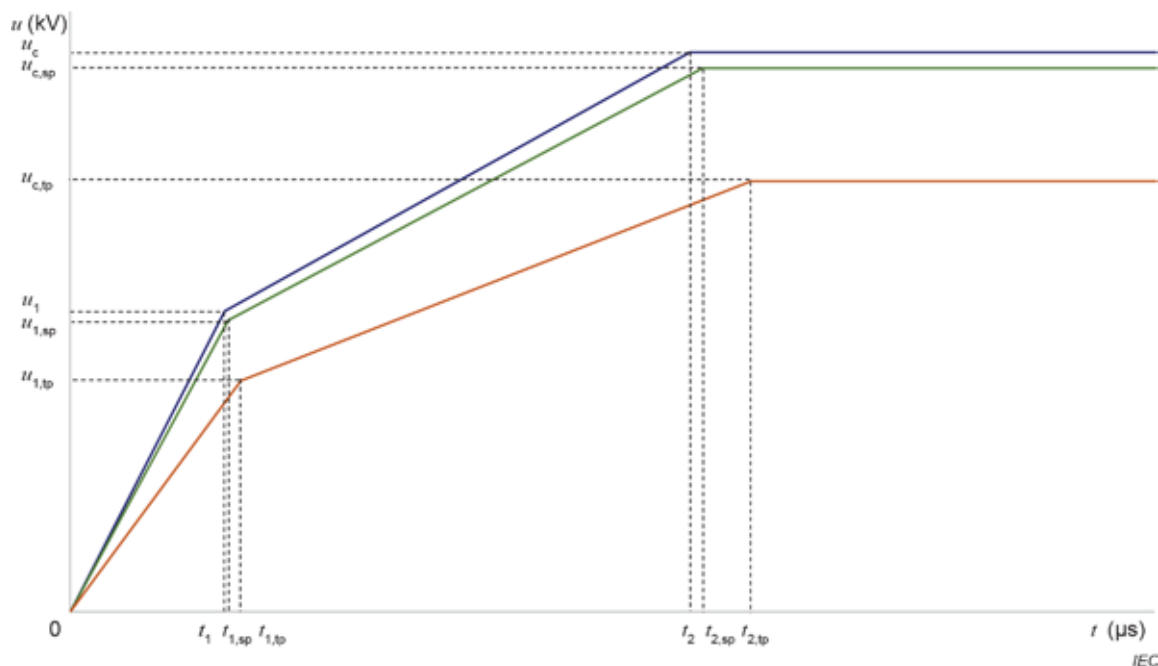
The first-pole-to-clear is in phase A.

The second pole-to-clear is in phase C.

Test parameters are calculated based on earthing arrangements in circuits as described in IEC TR 62271-306.

TRV phases B and C for 4 parameters (see Figure 5):

- u_1 the first reference voltage is derived by applying the same reduction factor used for the TRV peak u_c .
- t_1 is derived from u_1 and the respective du/dt reduction factor.
- t_2 is derived from t_1 keeping the same ratio as for the first pole-to-clear.



Key

Blue line: first pole-to-clear

Green line: second pole-to-clear

Red line: third pole-to-clear

Figure 5 – Reference lines of TRV with four-parameter for $k_{pp} = 1,3$

Table 5 – Test parameters during three phase interruption for test-duties T10, T30, T60 and T100s, $k_{pp} = 1,2$

TRV peak in %				Recovery voltage peak p.u.	du/dt %	di/dt %	Phase angle °
		At instance of first-pole-to-clear	At instance of second and third-pole-to-clear				
Phases	A	100	- / -	1	100	100	-
	B	0	- / 83	1	83	75	120
	C	0	95 / -	1	95	92	71
Between phases	A – B	100	- / 124	1,732			
	B – C	0	95 / 126	1,732			
	A – C	100	105 / -	1,732			

TRV peak first pole: $u_c = k_{af} \times k_{pp} \times U_r \times \sqrt{2} / \sqrt{3}$

1 p.u. = $U_r \times \sqrt{2} / \sqrt{3}$

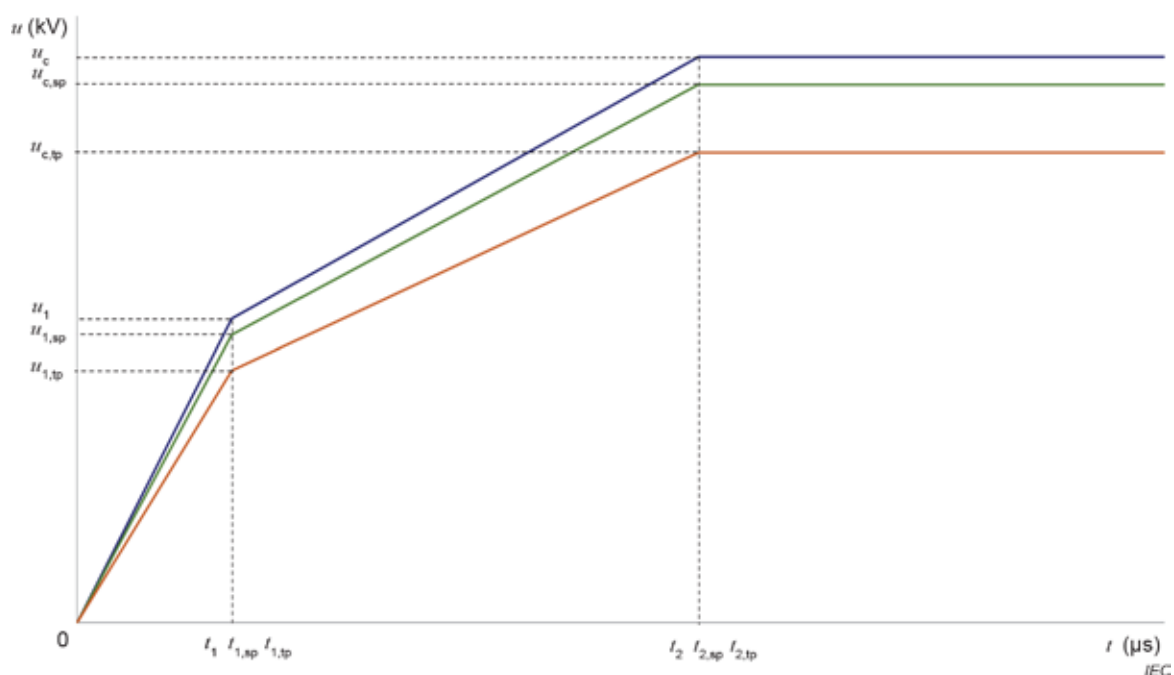
The first-pole-to-clear is in phase A.

The second pole-to-clear is in phase C.

Test parameters are calculated based on earthing arrangements in circuits as described in IEC TR 62271-306.

TRV phases B and C for 4 parameters (see Figure 6):

- u_1 the first reference voltage is derived by applying the same reduction factor used for the TRV peak u_c .
- t_1 is derived from u_1 and the respective du/dt reduction factor.
- t_2 is derived from t_1 keeping the same ratio as for the first pole-to-clear.



Key

Blue line: first pole-to-clear
 Green line: second pole-to-clear
 Red line: third pole-to-clear

Figure 6 – Reference lines of TRV with four-parameter for $k_{pp} = 1,2$

5 Synthetic testing techniques and methods for short-circuit making tests

5.1 Basic principles and general requirements for synthetic making test methods

5.1.1 General

During a closing operation onto a short-circuit, the circuit-breaker contact gap is subjected to the applied voltage as per 7.105.1 of IEC 62271-100:2021. After the moment of breakdown, the circuit-breaker is subjected to the making current as per 7.105.2.1 of IEC 62271-100:2021. In a synthetic test circuit, the applied voltage is supplied by a separate voltage circuit and the short-circuit current is supplied by a current circuit at reduced voltage. This latter is connected to the circuit-breaker immediately after breakdown of the contact gap by means of a fast making device, for example a triggered spark gap.

Any particular synthetic method chosen for testing shall adequately stress the test circuit-breaker. Generally the adequacy is established when the test method meets the requirements set forth in the following paragraphs and subclauses 5.1 and 5.2.

Prior to making, a circuit-breaker withstands the rated phase-to-earth voltage applied across its terminals: during making, it carries the rated short-circuit current. If closer attention is paid to the voltage and current stresses during the making test (see Figure 7 a) and b)), three main intervals can be recognized.

– High-voltage interval

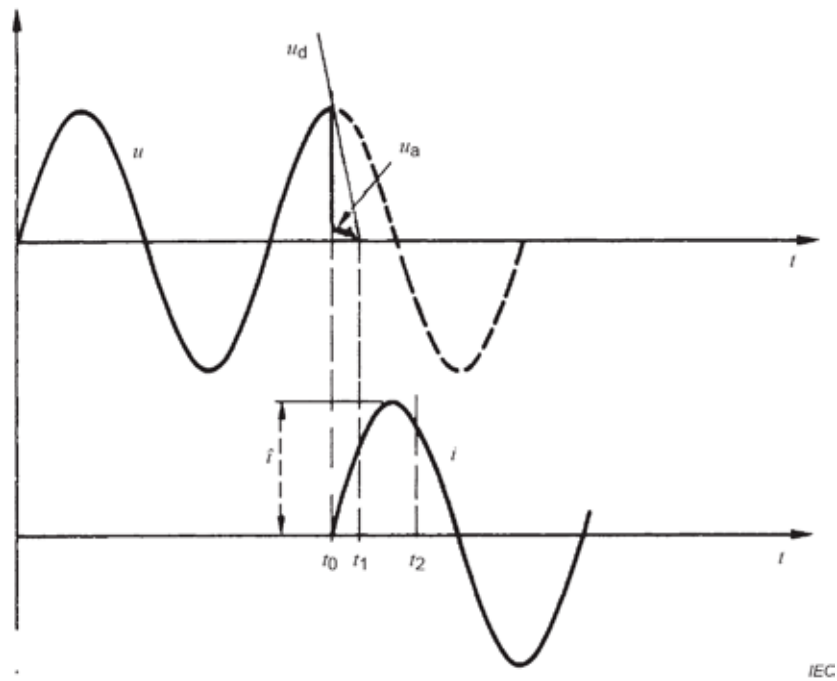
The high-voltage interval is the time from the commencement of the test, with the circuit-breaker in the open position, to the moment of breakdown across the contact gap.

- Pre-arcing interval

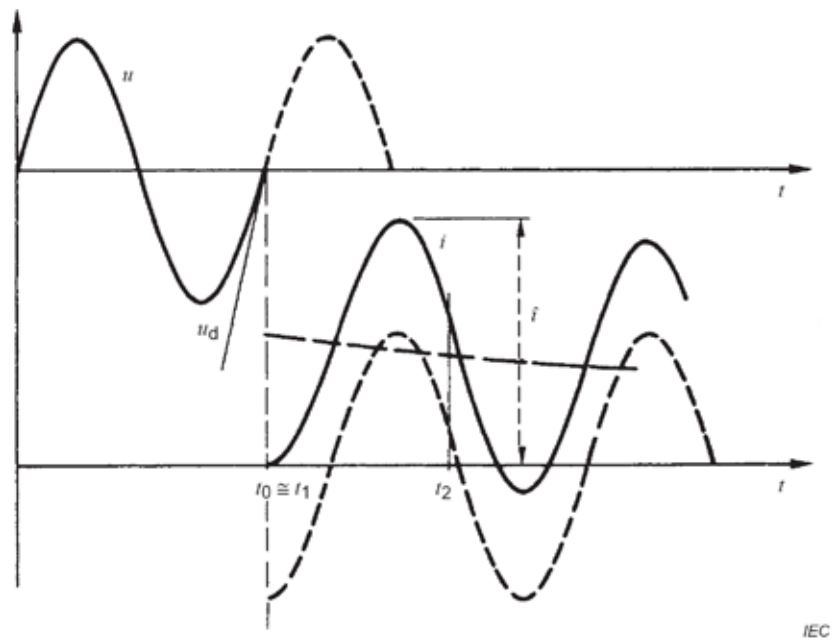
The pre-arcing interval is the time, during the closing stroke of the circuit-breaker, from the moment of breakdown across the contact gap to the touching of the contacts.

- Latching interval

The latching interval is the time, during the closing stroke of the circuit-breaker, from the touching of the contacts to the moment when the contacts reach the fully closed (latched) position.



a) Symmetrical making current



b) Asymmetrical making current

Key

i	current	u_a	arc voltage
$\hat{i}$	making current peak	t_0	instant of pre-strike
u	power-frequency voltage	t_1	instant of contact touch
u_d	RDDS	t_2	instant of reaching fully closed position

Figure 7 – Making process – Basic time intervals

5.1.2 High-voltage interval

During this interval, the circuit-breaker shall be stressed by the test circuit in such a way that the starting conditions for the pre-arcing interval, within the tolerances to be specified, are the same as the following reference system conditions. The applied voltage shall comply with the requirement set forth in 7.105.1 of IEC 62271-100:2021.

5.1.3 Pre-arcing interval

During pre-arcing, the circuit-breaker is subjected to electrodynamic forces due to the current and to deteriorating effects due to arc-energy. The current is composed of three components:

- the initial transient making current (ITMC);
- the DC and AC components of the short-circuit current.

Two typical cases can occur depending on the moment of closing:

- breakdown occurs near the crest of the applied voltage establishing an almost symmetrical current; pre-arc energy and ITMC are relatively high;
- breakdown occurs near zero of the applied voltage establishing an asymmetrical current; pre-arc energy and ITMC are negligible.

5.1.4 Latching interval and fully closed position

During these intervals, the circuit-breaker shall close in presence of the electrodynamic forces due to the current and contact friction forces. Therefore, during these intervals, the making current shall comply with 5.103 of IEC 62271-100:2021.

5.2 Synthetic test circuit and related specific requirements for making tests

5.2.1 General

Three-phase short-circuit making test can be performed with any one of the test circuits to cover applications in $k_{pp} = 1,5$, $k_{pp} = 1,3$, $k_{pp} = 1,2$ or $k_{pp} = 1,0$.

The synthetic test procedure is applied to comply with requirement a) of 7.105.2.1 of IEC 62271-100:2021.

5.2.2 Test circuit and test requirements

The test circuit is made up with two circuits, namely the current and the voltage circuit. Examples of circuits showing voltage and current wave shapes are given in Figure 8 and Figure 9 for single-phase and Figure 10 for three-phase:

- the voltage circuit supplies:
 - the applied voltage during the high-voltage interval,
 - the ITMC during the pre-arcing interval, by the discharge of the ITMC-circuit;
- the current circuit supplies the making current during the pre-arcing and latching intervals.

The high-voltage circuit can be an AC circuit, a DC circuit or a combination of both.

The injected current supplied by the voltage circuit shall ensure pre-arcing until the breakdown of the fast make gap. Therefore, the time constant of the ITMC circuit shall be long enough to ensure current flow during the time delay of the making device.

For the making operation of T100s set forth under point a) of 7.105.2.1 of IEC 62271-100:2021, the following conditions shall be fulfilled:

- the instantaneous value of the applied voltage at initiation of pre-arc for the first phase-to-make is not less than 97 % of the requirements of 7.105.1 of IEC 62271-100:2021;
- the time delay of the making device (t_m) is shorter than 300 μ s;
- the actual peak current of the 1st loop is not less than 0,74 p.u and no more than 1,26 p.u., where the peak current of 1,0 p.u. is the peak value of the symmetrical rated short-circuit breaking current;

NOTE 1 A test where an earlier current inception between -15° and -30° is achieved, resulting in an actual current up to 1,5 p.u., is considered as more severe.

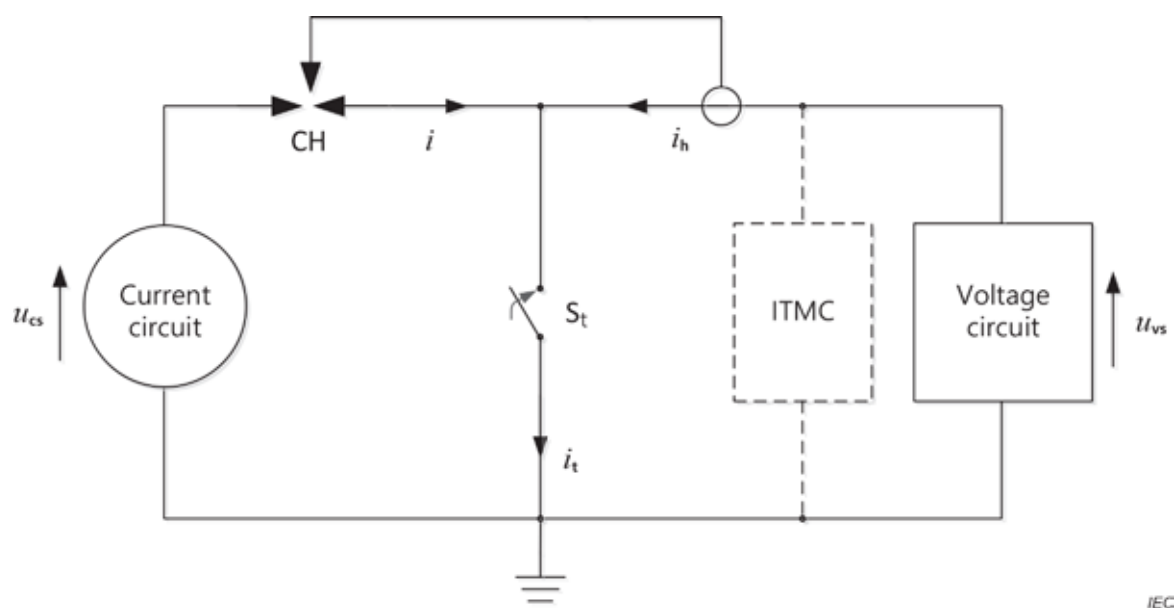
- the short-circuit current, when the test is performed as separate making operation, is maintained for an interval of at least 100 ms, as specified in 7.107.5.1 of IEC 62271-100:2021.

For the making operation of test-duty OP2, the following conditions shall be fulfilled:

- the instantaneous value of the applied voltage at initiation of pre-arc is not less than 92 % of the requirements of 7.110.3 of IEC 62271-100:2021;
- the time delay of the making device (t_m) is shorter than 300 μ s;
- if the pre-arcing time is shorter than or equal to half a cycle of power frequency, no further requirements on the current are given provided that the RMS current is not less than 1 kA;
- if the pre-arcing time is longer than half a cycle of power frequency, the actual peak current of the 1st loop is not less than 0,74 p.u and no more than 1,26 p.u. The peak current of 1,0 p.u. is the peak value of the symmetrical rated out-of-phase breaking current;

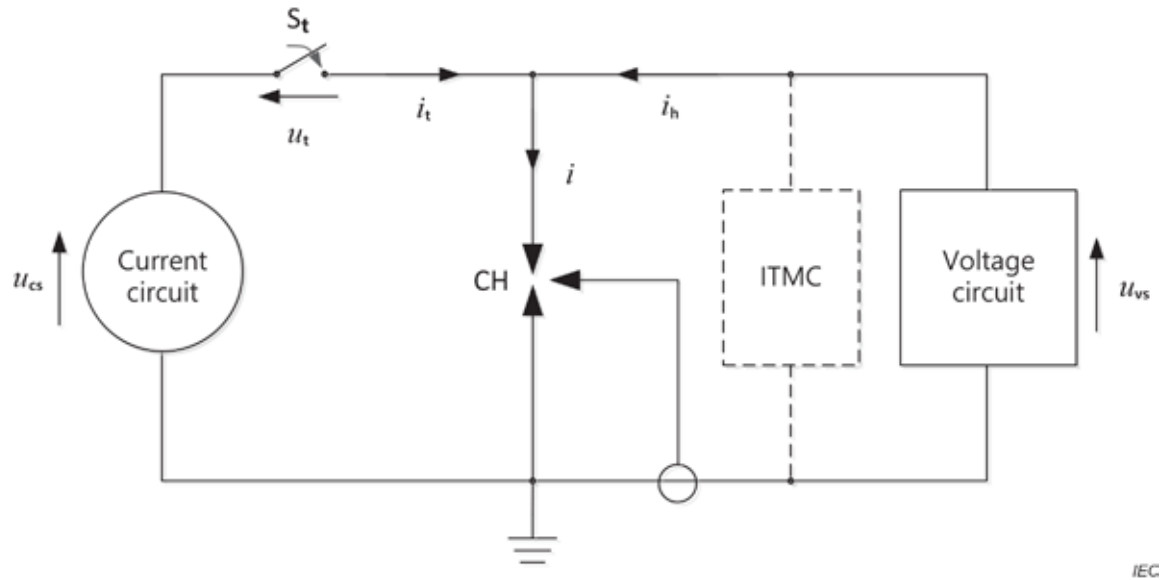
NOTE 2 A test where an earlier current inception between -15° and -30° is achieved, resulting in an actual current up to 1,5 p.u., is considered as more severe.

- the out-of-phase making current, when the test is performed as separate making operation, is maintained for an interval of at least 100 ms.

**Key**

u_{cs}	voltage of current circuit	u_{vs}	voltage of voltage circuit
CH	making device (triggered spark gap)	i_h	initial transient making current (ITMC)
i	power-frequency current supplied by current circuit	i_t	current in the test circuit-breaker
S_t	test circuit-breaker	t_m	time delay of making device

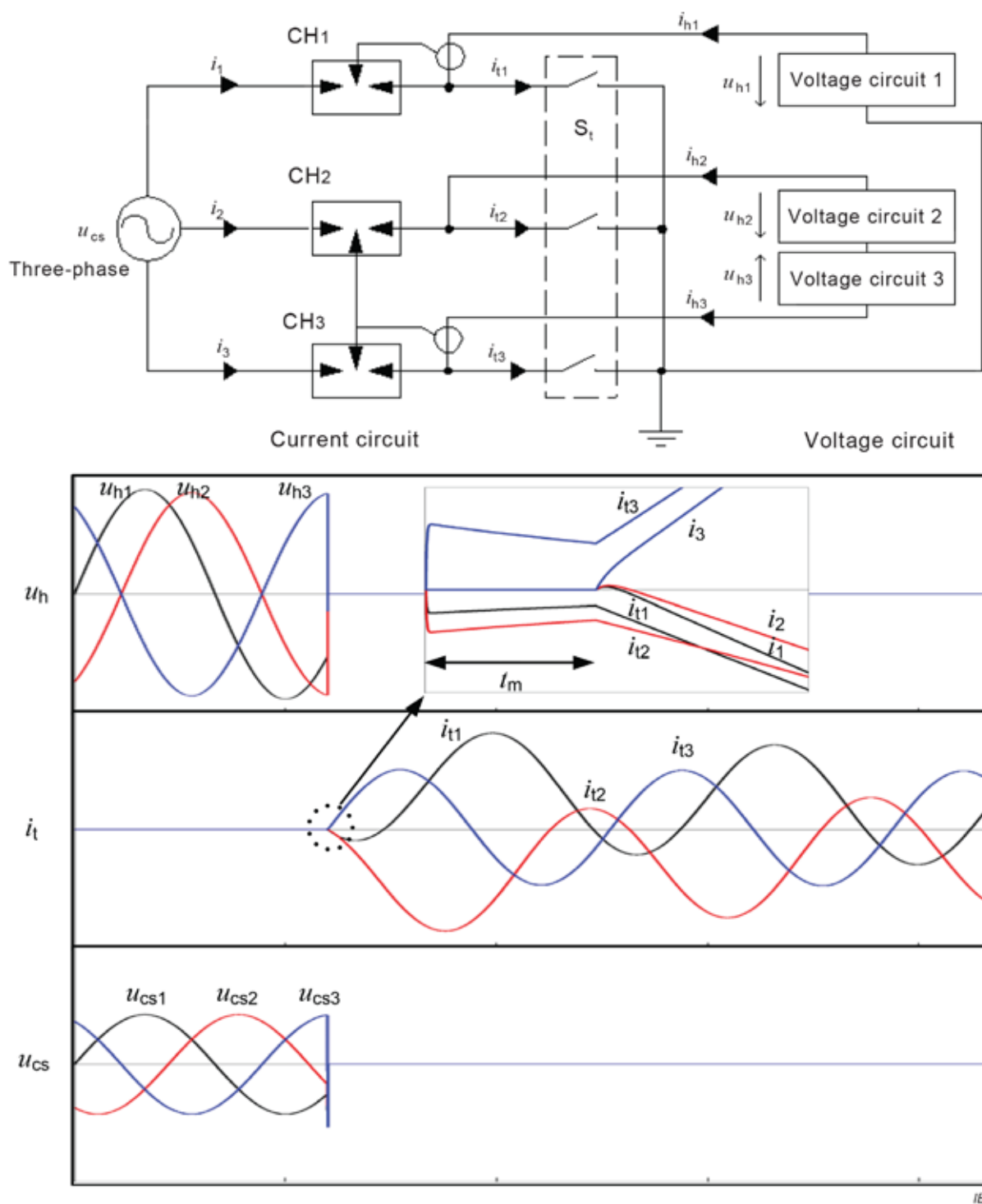
Figure 8 – Example of synthetic making circuit for single-phase tests



Key

u_{cs}	voltage of current circuit	u_{vs}	voltage of voltage circuit
CH	making device (triggered spark gap)	i_h	initial transient making current (ITMC)
i	power-frequency current supplied by current circuit	i_t	current in the test circuit-breaker
S_t	test circuit-breaker	u_t	test voltage across test circuit-breaker
t_m	time delay of making device		

Figure 9 – Example of synthetic making circuit for out-of-phase tests



Key

$u_{cs1}, u_{cs2}, u_{cs3}$	voltage of current circuit	u_{h1}, u_{h2}, u_{h3}	applied voltage
i_1, i_2, i_3	current supplied by the current circuit	CH ₁ , CH ₂ , CH ₃	making device (triggered spark gap)
i_{t1}, i_{t2}, i_{t3}	current through the test object	S_t	test circuit-breaker
i_{h1}, i_{h2}, i_{h3}	initial transient making current (ITMC)	t_m	time delay of making device

Figure 10 – Example of synthetic making circuit for three-phase tests ($k_{pp} = 1,5$)

5.2.3 Alternative test method with reduced voltage

5.2.3.1 General

This alternative test method is permitted only with the consent of the manufacturer.

The test consists of two parts:

- part 1: a test at rated voltage and reduced current to determine the pre-arcing time;
- part 2: a test at reduced voltage and rated making current, with the required pre-arcing time.

5.2.3.2 Part 1: determination of pre-arcing time

5.2.3.2.1 General

The pre-arcing time shall be determined by performing making tests at rated voltage and reduced current. The arrangement of the circuit-breaker shall be as described in 7.105.1 of IEC 62271-100:2021. The current shall be low enough to avoid contact erosion.

5.2.3.2.2 Single-phase tests

In those cases where the circuit-breaker design permits single-pole testing, at least two making tests performed to evaluate the pre-arcing time shall result in a current initiation instant corresponding to an angle of -15° to $+15^\circ$ on the peak of the applied AC voltage wave-shape. The maximum pre-arcing time measured shall be used as pre-arcing time to be applied in part 2 (see 5.2.3.3).

5.2.3.2.3 Three-phase tests

In a three-phase circuit, for each phase, at least one making test performed to evaluate the pre-arcing time shall result in a current initiation instant corresponding to an angle of -15° to $+15^\circ$ on the peak of the applied AC voltage wave-shape. Pre-arcing time shall be measured in all three phases for each test.

The maximum pre-arcing times measured, corresponding to the test giving the longest pre-arcing time in each phase, shall be used as pre-arcing times to be applied in part 2 (see 5.2.3.3).

If a single-phase voltage circuit is used, the pre-arcing time shall be measured in all three-phases, with the assumption that the current initiation would have occur simultaneously in all three phases.

5.2.3.3 Part 2: short-circuit current making test at reduced voltage

During current making test with rated short-circuit making current at reduced voltage, the pre-arcing time shall be at least equal to the pre-arcing time determined in the tests as described in part 1 (see 5.2.3.2).

To obtain the required maximum pre-arcing time, the initiation of current can be achieved by a voltage of any wave form, high enough to initiate the pre-arcing at the correct point on the wave, with the required pre-arcing time determined in part 1.

Conditions required for a correct making operation remain applicable.

7 Type tests

7.102 General

Subclauses 7.102 through 7.112 of IEC 62271-100:2021 are also applicable for synthetic testing. However, in some cases, special techniques are necessary. These cases are outlined in the following paragraphs and subclauses 7.102 to 7.111. The numbering of the subclauses corresponds to that of IEC 62271-100:2021.

Requirements concerning testing of metal enclosed circuit-breakers are given in Annex G.

General requirements for circuit-breakers with opening resistors are given in Annex J of IEC 62271-100:2021. A method available for testing circuit-breakers having opening resistors is reported in Annex J.

The symbols and abbreviated terms given in Table 6 are used to specify the operations to be performed.

Table 6 – Symbols and abbreviated terms used for operation during synthetic tests

Cd	Closing operation in a direct circuit at the voltage of the current circuit which can be less than the voltage specified in 7.105.1 of IEC 62271-100:2021
(Cd)	Closing operation as Cd, which can be carried out under no-load conditions
Cd _{asy}	Closing operation against the rated short-circuit making current according to 7.105.2 of IEC 62271-100:2021 in a direct circuit at conditions described under Cd
Cs	Closing operation with specified parameters in a synthetic circuit
Cs _{sym}	Closing operation against a symmetrical current equal to the rated short-circuit breaking current, carried out at the required applied voltage in a synthetic circuit
Od	Breaking operation at the voltage of the current circuit only and with the specified breaking current
Os	Breaking operation with specified parameters in a synthetic circuit
<i>t</i>	Time interval between operations (0,3 s or 3 min depending on rapid auto-reclosing or auto-reclosing rated operating sequence)
<i>t'</i>	Time interval between operations (3 min)
SP	Single-phase test as defined in 7.108.2 of IEC 62271-100:2021
DEF	Double-earth fault test as defined in 7.108.2 of IEC 62271-100:2021
NOTE Due to the characteristics of synthetic testing, it can be difficult to comply with the specified time intervals of the rated operating sequence. See 7.106.1 of IEC 62271-100:2021.	

In order to comply with all the requirements, it may be necessary to make more operations than specified in the normal test-duty. In such cases the circuit-breaker can be reconditioned, and the test duty repeated.

7.102.4.2 Unit testing

7.102.4.2.1 General

7.102.4.2.1 of IEC 62271-100:2021 is applicable with the following addition.

In the case of metal-enclosed circuit-breakers, Annex G gives details of some examples of test circuits and Annex I of IEC 62271-100:2021 outlines appropriate testing guidelines.

Where the other unit is used as auxiliary circuit-breaker, this other unit is not considered to be a part of the test object. Therefore, a failure of this other unit shall not be considered as a failure of the test object.

7.102.4.2.5 Additional requirements for unit testing

7.102.4.2.5 of IEC 62271-100:2021 is applicable with the following addition.

For verifying insulation performance of metal enclosed circuit-breakers between live parts and enclosures, an additional test shall be performed with:

- the rated short-circuit current interrupted by all units under condition of maximum arcing time;
- the corresponding voltage applied between the incoming terminal and the tank for both duties T100s and T100a.

A single breaking operation is sufficient to demonstrate this performance. The circuit-breaker can be reconditioned before this additional test.

7.102.4.3 Multi-part testing

Opening operations of circuit-breakers with closing resistors require no special testing techniques since the closing resistor will not influence the test circuit.

The closing resistors can only be tested in a direct circuit that provides the correct current and voltage stresses from a single power source.

During the synthetic making tests, it is necessary to remove the closing resistor in order to obtain the correct short-circuit current stresses and pre-arcing conditions in the making and breaking unit.

If all the TRV and/or the recovery voltage requirements cannot be met simultaneously, multi-part testing can be used taking into account 7.102.4.3 of IEC 62271-100:2021.

When multi-part testing is performed to verify only the recovery voltage, it is not necessary to establish the minimum arcing time once again.

7.102.7 Alternative operating mechanisms

In case of a GIS circuit-breaker with three-poles in one enclosure, the tests shall be carried out in a three-phase test circuit with the TRV from synthetic circuits applied on all the three-phases. T100s test-duty, on the alternative operating mechanism, can be demonstrated by using methods defined in Annex D (three-phase currents with one synthetic circuit). The interaction between phases during interruption has already been demonstrated during the T100s on the completely tested circuit-breaker. Test methods as per Annex D adequately verifies the circuit-breaker's capability to perform the test-sequence with currents in all three-phases, correct arcing times and TRVs corresponding to various poles-to-clear.

7.104 Demonstration of arcing times

7.104.1 General

The basic requirements to be met are given in 7.104 of IEC 62271-100:2021.

In order to be able to perform synthetic tests on the same basis as direct tests, normally it will be necessary to apply special re-ignition methods to prolong the arcing of the test circuit-breaker through the necessary number of zeros of the power-frequency current. See Annex H for re-ignition methods to prolong arcing.

The "step-by-step" method described in Annex H is the method used on most synthetic tests. The method is considered to be a sufficiently close approximation of the direct testing procedure.

The arcing is prolonged by means of thermal re-ignitions. As this method makes it possible to force the test circuit-breaker to re-ignite in all conditions, special care shall be taken not to re-ignite the circuit-breaker at the instant of a current zero when the circuit-breaker can clear. For this purpose, it is necessary to determine, for each terminal fault, short-line fault and out-of-phase test duty, the minimum arcing time of the circuit-breaker. At least two breaking tests, one clearance and one re-ignition, are necessary for this determination.

The clearance at the minimum arcing time is the first valid breaking operation. The other test is performed to demonstrate that a re-ignition at an early current zero would take place between the arcing contacts. This re-ignition test shall be performed in addition to the test sequence as described in Table 7 and shall not be the last test in the test-duty.

The extra tests necessary to demonstrate correct behaviour at early current zeros will usually contribute insignificantly to contact wear, etc., due to the short arcing times. Therefore, no re-conditioning should be necessary because of these tests. The re-ignition(s) obtained when determining the minimum arcing time do(es) not indicate a failure of the circuit-breaker. However, it is important to establish that this re-ignition has taken place between the arcing contacts only. When using a current injection method, the interruption of the injected current a few loops after the re-ignition is often a useful means for the judgement. Thorough inspection of screens, arcing and main contacts, etc., should also be made to verify correct behaviour.

The preferred order to verify the correct reignition behaviour is at the beginning of the test sequence when searching for the minimum arcing time. If, for any reason this test is not done at the beginning of a test sequence, it can be accepted, provided that at least one operation has resulted in a clearance after this test. This is to provide evidence that the reignition did not damage any part of the circuit-breaker.

When performing Od-*t*-COs operations, the first opening operation is performed in a direct test circuit. This first opening operation shall represent the minimum arcing time found for single opening operations. In case the arcing time of this first opening operation is longer than required, the test is more severe. For Od operations, a tolerance of ± 2 ms on the arcing time applies.

The minimum clearing time for test-duty T100a is validated by the minimum arcing time of an interruption after a major loop with intermediate asymmetry.

7.104.2 Three-phase tests

Depending on the test circuit used, the test procedures given here may not cover the conditions of the 3rd pole-to-clear for $k_{pp} = 1,3$. For this case the same procedures can be applied, with the manufacturer's consent, by combining the TRV and di/dt parameters for the 2nd pole-to-clear and the arcing time corresponding to the 3rd pole-to-clear. Alternatively, an additional test can be performed with the TRV, di/dt and the maximum arcing time corresponding to the 3rd pole-to-clear.

For alternative testing procedures of multi-enclosure type circuit-breakers with operating mechanism characteristics that require three-phase current, see Annex D.

7.104.2.1 Test-duty T10, T30, T60, T100s, T100s(b)

The test procedure is as follows.

For convenience of testing, the pole in phase A is kept as the first-pole-to-clear.

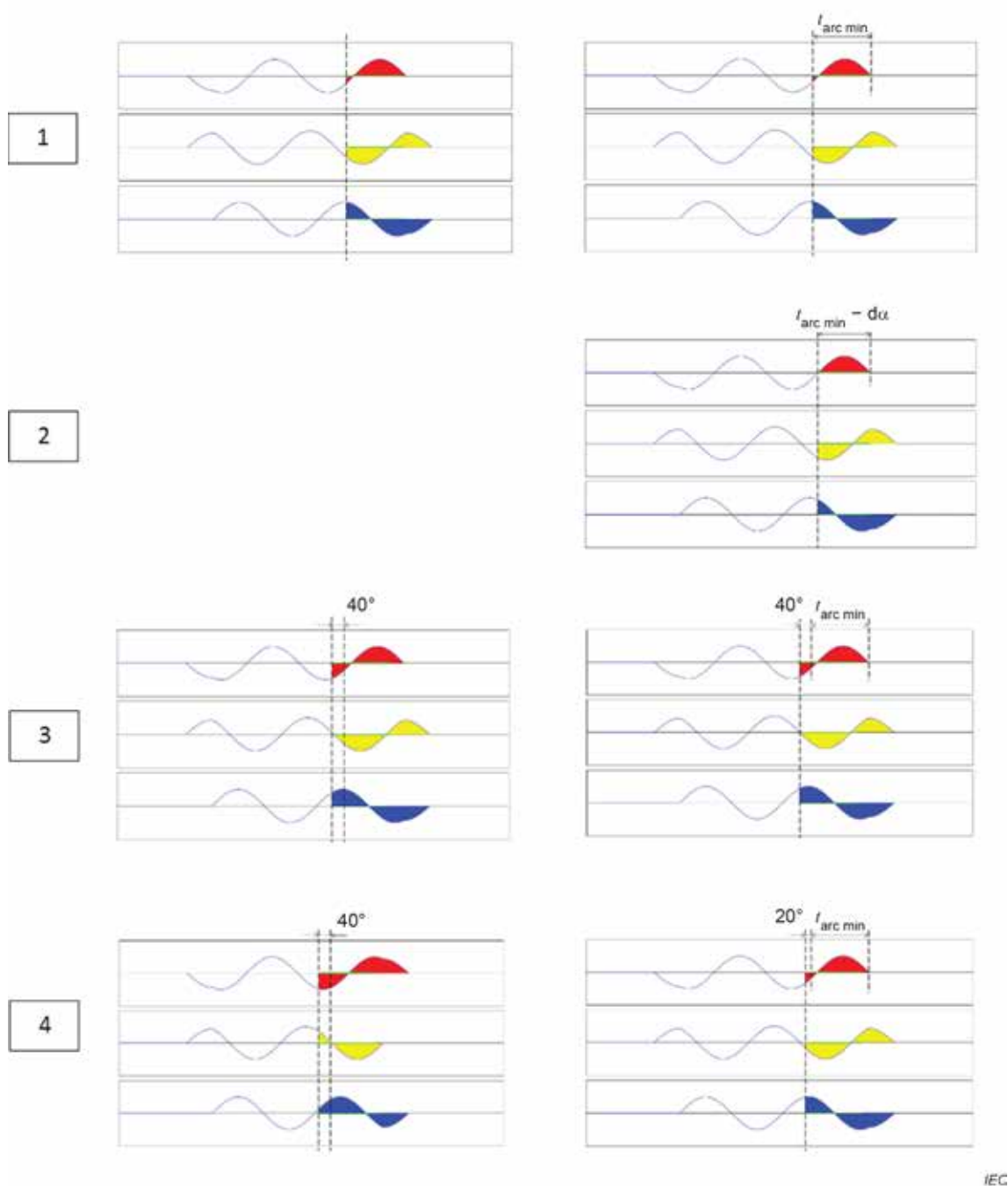
First the minimum arcing time and correct re-ignition behaviour are established. This is done by changing the setting of the tripping command in steps of 18° (possibly this shall be repeated several times). After having done so, the setting of the control of the tripping command shall be advanced by approximately 40° , starting from the shortest arcing time at which the circuit-breaker cleared. For the last test, the setting of the control of the tripping command shall be advanced by approximately 20° , starting from the shortest arcing time at which the circuit-breaker cleared:

- first valid breaking operation: $t_{\text{arc min}}$, minimum arcing time in phase A;
- re-ignition test: $t_{\text{arc reig}} = t_{\text{arc min}} - 18^\circ$, re-ignition in phase A;
- second valid breaking operation: $t_{\text{arc max}} = t_{\text{arc min}} + 40^\circ$, maximum arcing time in phase A;
- third valid breaking operation: $t_{\text{arc med}} = t_{\text{arc min}} + 20^\circ$, medium arcing time in phase A.

The first valid breaking operation and re-ignition test consist of single opening operations. The order of the first valid breaking operation and re-ignition test can be interchanged.

The order of the second and third valid breaking operations can be interchanged and are carried out as part of the rated operating sequence.

For comparison with the arcing time settings used in three-phase direct tests, see Figure 11 and Figure 12.

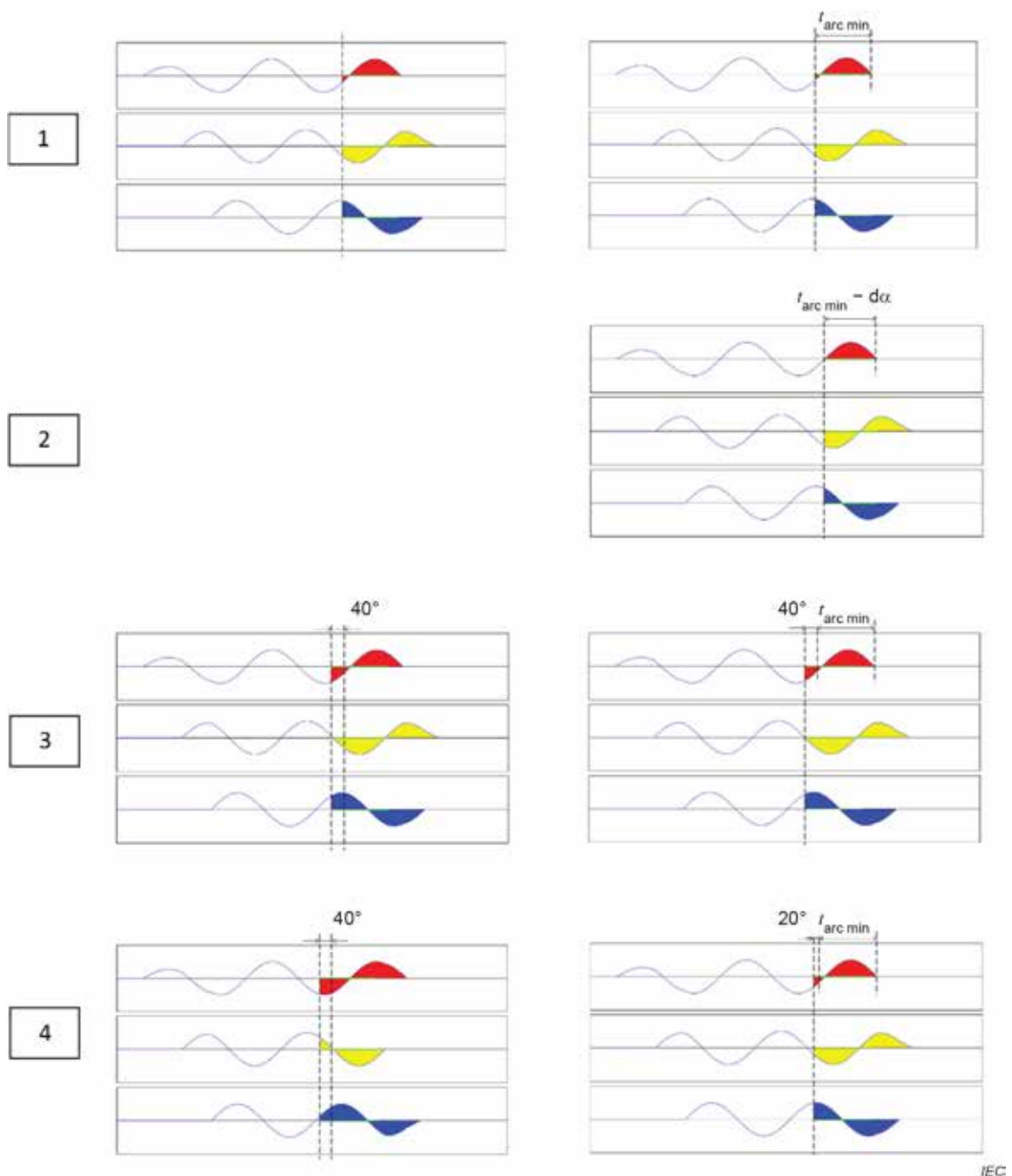


IEC

Key

- | | | |
|---|--|---|
| 1 | first test | first test, $t_{\text{arc min}}$ |
| 2 | | second test, $t_{\text{arc min}} - d\alpha$, resulting in re-ignition |
| 3 | second test, tripping command 40° advanced, related to first test | third test, tripping command 40° advanced, related to first test |
| 4 | third test, tripping command 40° advanced, related to second test | fourth test tripping command 20° advanced, related to first test |

Figure 11 – Comparison of arcing time settings during three-phase direct tests (left) and three-phase synthetic (right) for T100s with $k_{pp} = 1,5$



Key

- | | | |
|---|--|---|
| 1 | first test | first test, $t_{\text{arc min}}$ |
| 2 | | second test, $t_{\text{arc min}} - d\alpha$, resulting in re-ignition |
| 3 | second test, tripping command 40° advanced, related to first test | third test, tripping command 40° advanced, related to first test |
| 4 | third test, tripping command 40° advanced, related to second test | fourth test tripping command 20° advanced, related to first test |

Figure 12 – Comparison of arcing time settings during three-phase direct tests (left) and three-phase synthetic (right) for T100s with $k_{pp} = 1,3$

7.104.2.2 Test-duty T100a

The intention is to demonstrate in a series of breaking tests the requirement a) and b) as defined in 7.104.2.2 of IEC 62271-100:2021:

- condition a) where arc extinction occurs in the first-pole-to-clear at the end of a major loop in the first phase with the required asymmetry criteria and with the longest possible arcing time t_{arc1} ;
- condition b) where arc extinction occurs at the end of a major extended loop in the last-pole-to-clear or in the second-pole-to-clear with the required asymmetry criteria and with the longest possible arcing time, t_{arc2} and t_{arc3} as follows:
 - the longest possible arcing time t_{arc2} applies for the last-pole-to-clear for circuit-breakers rated for $k_{pp} = 1,5$;
 - the longest possible arcing time t_{arc2} applies for the last-pole-to-clear for circuit-breakers rated for $k_{pp} = 1,5$.

The test procedure, for three-phase testing, is as follows.

In order to simplify the test procedure, the pole in phase A is kept as the first-pole-to-clear. As a consequence, the pole in phase C will be subjected to increased electrical wear. In order to obtain similar electrical wear on the poles of phase B and C, the test can be performed by exchanging the poles of phases B and C for the second breaking operation.

First the minimum arcing time $t_{arc\ min}$ (Figure 10 and Figure 11, first test) and re-ignition behaviour (Figure 10 and Figure 11, second test) shall be demonstrated having intermediate asymmetry in phase A (Table E.12 to Table E.17, columns 7, 8 and 9) and with the major extended loop occurring in phase C. This is done by changing the setting of the tripping command in steps of $d\alpha = 18^\circ$ until the minimum arcing time is established.

Before the next operation, initiation of short-circuit current shall be advanced by 60° where the required asymmetry changes to phase A (Figure 10 and Figure 11 third test). Arc extinction shall occur in phase A, the first-pole-to-clear at the end of a major loop with the required asymmetry criteria and with the maximum arcing time demonstrating condition a) mentioned above.

The maximum arcing time t_{arc1} for the first pole-to-clear is achieved when the following condition is met:

$$t_{arc1} = t_{arc\ min} + \Delta t_{a1} - T \times d\alpha/360^\circ$$

In the next operation, the initiation of short-circuit current shall be delayed by 60° . As a result, the required asymmetry changes to phase C. Arc extinction shall occur in phase C at the end of a major extended loop with the required asymmetry criteria and with the maximum arcing time demonstrating condition b) mentioned above:

- the maximum arcing time t_{arc2} for the last-pole-to-clear for circuit-breakers rated for $k_{pp} = 1,5$ (Figure 10 fourth test) is achieved when the following condition is met:

$$t_{arc2} = t_{arc\ min} + \Delta t_{a2} - T \times d\alpha/360^\circ$$

- the maximum arcing time t_{arc3} for the second-pole-to-clear for circuit-breakers rated for $k_{pp} = 1,3$ or $k_{pp} = 1,2$ (Figure 11 fourth test) is achieved when the following condition is met:

$$t_{arc3} = t_{arc\ min} + \Delta t_{a3} - T \times d\alpha/360^\circ$$

where

Δt_{a1} , Δt_{a2} , Δt_{a3} are the relevant time parameters to be selected from Table E.12 to Table E.17.

The order of the last two breaking operations can be interchanged.

Some circuit-breakers will not clear at the end of a major loop after the required arcing time. However, this test is valid if the circuit-breaker clears the subsequent minor loop, that becomes the last-pole-to-clear. The corresponding parameters for the last-pole-to-clear for symmetrical condition shall be applied.

For comparison with the arcing settings used in three-phase direct tests, see Figure 10 and Figure 11.

NOTE The last breaking operation required by 7.104.2.2 of IEC 62271-100:2021 is covered by the tests to demonstrate the minimum arcing time.