

Semiconductor devices —

Part 8: Field-effect transistors

ICS 31.080.01

National foreword

This British Standard is the official English language version of IEC 60747-8:2000 and implements it as the UK national standard. It supersedes BS 6493-1.8:1985 which is withdrawn.

The UK participation in its preparation was entrusted to Technical Committee EPL/ 47, Semiconductors, which has the responsibility to:

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**Partie 8:
Transistors à effet de champ**

Semiconductor devices –

**Part 8:
Field-effect transistors**



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CONTENTS

	Page
FOREWORD	7
INTRODUCTION	9
Clause	
1 Scope	10
2 Normative references.....	10
3 Classification	11
4 Terminology and letter symbols	11
4.1 Types of field-effect transistors	11
4.2 General terms.....	13
4.3 Terms related to ratings and characteristics.....	15
4.4 Letter symbols	16
5 Essential ratings and characteristics	23
5.1 General	23
5.1.1 Device categories	23
5.1.2 Multiple-gate devices	23
5.1.3 Handling precautions	23
5.2 Ratings (limiting values)	23
5.2.1 Temperatures	23
5.2.2 Power dissipation (P_{tot}).....	23
5.2.3 Voltages and currents	24
5.2.4 Mechanical data.....	25
5.3 Characteristics.....	25
5.3.1 Characteristics for low-frequency amplifier applications	25
5.3.2 Characteristics for high-frequency amplifier applications.....	27
5.3.3 Characteristics for switching applications.....	29
5.3.4 Characteristics for chopper applications.....	31
5.3.5 Characteristics for low-level d.c. amplifier applications	34
5.3.6 Characteristics for voltage-controlled resistor applications	35
5.3.7 Specific characteristics of matched-pair field-effect transistors for low-frequency differential applications	37
5.4 Application data.....	38
5.4.1 Intermodulation and AGC.....	38
6 Measuring methods	38
6.1 General	38
6.1.1 Polarity	38
6.1.2 General precautions.....	38
6.1.3 Handling precautions	38
6.1.4 Type categories	38
6.2 Gate cut-off current or gate leakage current.....	38
6.2.1 Gate cut-off current of junction-gate type (type A).....	38
6.2.2 Gate leakage current of insulated-gate type (types B and C).....	39

Clause	Page
6.3 Drain current (types A, B and C) (I_D).....	40
6.3.1 Purpose	40
6.3.2 Circuit diagram	40
6.3.3 Circuit description and requirements	40
6.3.4 Precautions to be observed.....	40
6.3.5 Measurement procedure	41
6.3.6 Specified conditions.....	41
6.4 Drain cut-off current (types A, B and C)	41
6.4.1 Purpose	41
6.4.2 Circuit diagram	41
6.4.3 Precautions to be observed (for types B and C)	41
6.4.4 Measurement procedure	41
6.4.5 Specified conditions.....	41
6.5 Gate-source cut-off voltage (types A and B) ($V_{GS(off)}$).....	41
6.5.1 Purpose	41
6.5.2 Circuit diagram	41
6.5.3 Precautions to be observed.....	41
6.5.4 Measurement procedure	42
6.5.5 Specified conditions.....	42
6.6 Gate-source threshold voltage (type C) ($V_{GS(To)}$)	42
6.6.1 Purpose	42
6.6.2 Circuit diagram	42
6.6.3 Precautions to be observed.....	42
6.6.4 Measurement procedure	42
6.6.5 Specified conditions.....	42
6.7 Small-signal short-circuit input capacitance (types A, B and C) (C_{iss})	42
6.7.1 Purpose	42
6.7.2 Circuit diagram	43
6.7.3 Circuit description and requirements	43
6.7.4 Precautions to be observed.....	44
6.7.5 Measurement procedure	44
6.7.6 Specified conditions.....	44
6.8 Small-signal short-circuit output conductance (type A, B and C) (g_{oss}).....	44
6.8.1 Purpose	44
6.8.2 General.....	44
6.8.3 Null method	44
6.8.4 Two-voltmeter method	45
6.9 Small-signal short-circuit output capacitance (type A, B and C) (C_{oss})	46
6.9.1 Purpose	46
6.9.2 General.....	47
6.9.3 Circuit diagrams.....	47
6.9.4 Circuit description and requirements	47
6.9.5 Precautions to be observed.....	47
6.9.6 Measurement procedure	48
6.9.7 Specified conditions.....	48

Clause	Page
6.10 Small-signal short-circuit forward transconductance (types A, B and C)	48
6.10.1 Purpose	48
6.10.2 General	48
6.10.3 Null method	48
6.10.4 Two-voltmeter method	50
6.11 Small-signal short-circuit feedback capacitance (types A, B and C) (C_{rs})	51
6.11.1 Purpose	51
6.11.2 Circuit diagram	51
6.11.3 Circuit description and requirements	52
6.11.4 Precautions to be observed	52
6.11.5 Measurement procedure	53
6.11.6 Specified conditions	53
6.12 Noise (types A, B and C) (F , V_n)	53
6.12.1 Purpose	53
6.12.2 Equivalent input noise voltage	53
6.12.3 Noise factor	55
6.12.4 Relation between equivalent input noise voltage and noise factor	55
6.13 y -parameters (types A, B and C)	56
6.14 Switching times (types A, B and C) (t_{on} , t_{off})	56
6.14.1 Purpose	56
6.14.2 General	56
6.14.3 Circuit diagram	56
6.14.4 Circuit description and requirements	56
6.14.5 Precautions to be observed	57
6.14.6 Measurement procedure	57
6.14.7 Specified conditions	57
6.15 Static drain-source on-state resistance ($r_{DS(on)}$) or drain-source on-state voltage ($V_{DS(on)}$) and off-state resistance ($r_{DS(off)}$)	58
6.15.1 Purpose	58
6.15.2 General	58
6.15.3 Circuit diagram	58
6.15.4 Circuit description and requirements	58
6.15.5 Precautions to be observed	58
6.15.6 Measurement procedure	59
6.15.7 Specified conditions	59
6.16 On-state drain-source resistance (under small-signal conditions) ($r_{ds(on)}$)	59
6.16.1 Purpose	59
6.16.2 Circuit diagram	59
6.16.3 Circuit description and requirements	59
6.16.4 Precautions to be observed	60
6.16.5 Measurement procedure	60
6.16.6 Specified conditions	60
6.17 Scattering parameters s	60

Clause	Page
6.18 Channel-case transient thermal impedance (Z_{thJC}) and thermal resistance (R_{thJC}) of a power field-effect transistor	60
6.18.1 Purpose	60
6.18.2 Cooling method	60
6.18.3 Heating method	62
6.19 Verification of the forward-bias and reverse-bias safe operating area (FBSOA, RBSOA)	64
6.19.1 Verification of the forward-bias safe operating area (FBSOA)	64
6.19.2 Verification of the reverse-bias safe operation area (RBSOA)	65
7 Acceptance and reliability	67
7.1 Electrical endurance tests	67
7.1.1 General requirements	67
7.1.2 Specific requirements	67
Figures 1 to 3 – Small-signal y parameters in common-source configuration and π equivalent circuit parameters	21
Figure 4 – Switching times	22
Figure 5 – Switching times	32
Figure 6 – Basic circuit for the measurement of gate cut-off current	39
Figure 7 – Basic circuit for the measurement of gate leakage current	39
Figure 8 – Basic circuit for the measurement of drain current	40
Figure 9 – Basic circuit for the measurement of small-signal short-circuit input capacitance	43
Figure 10 – Alternative circuit for measurement of small-signal short-circuit input capacitance	43
Figure 11 – Basic circuit for the measurement of the output conductance g_{oss} (null method)	44
Figure 12 – Basic circuit for the measurement of the output conductance g_{oss} (two-voltmeter method)	45
Figure 13 – Basic circuit for measurement of short-circuit output capacitance	47
Figure 14 – Alternative circuit for measurement of short-circuit output capacitance	47
Figure 15 – Circuit for the measurement of short-circuit forward transconductance g_{fs}	48
Figure 16 – Circuit for the measurement of forward transconductance g_{fs} (two-voltmeter method)	50
Figure 17 – Circuit for measurement of feedback capacitance C_{rs}	51
Figure 18 – Circuit for measurement of feedback capacitance C_{rs} (when the bridge cannot pass d.c.)	52
Figure 19 – Equivalent circuit	52
Figure 20 – Block diagram for the measurement of equivalent input noise voltage	53
Figure 21 – Circuit for the measurement of equivalent input noise voltage	54
Figure 22 – Circuit for measurement of switching times	56

	Page
Figure 23 – Waveforms in the measurement of switching times	57
Figure 24	58
Figure 25 – Circuit of measurement for on-state and off-state resistance	58
Figure 26	59
Figure 27 – Circuit diagram	61
Figure 28 – Circuit diagram	64
Figure 29 – Circuit diagram	65
Figure 30 – Test waveforms	66
Table 1 – Failure-defining characteristics for acceptance after endurance tests	68
Table 2 – Conditions for the endurance tests	68

INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES –

Part 8: Field-effect transistors

FOREWORD

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International Standard IEC 60747-8 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices and integrated circuits.

This second edition of IEC 60747-8 cancels and replaces the first edition published in 1984, amendment 1 (1991) and amendment 2 (1993). This second edition constitutes a technical revision.

The text of this standard is based on the first edition of IEC 60747-8, amendment 1, amendment 2 and on the following documents:

FDIS	Report on voting
47E/149/FDIS	47E/156/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This part 8 should be used in conjunction with IEC 60747-1.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

The committee has decided that the contents of this publication will remain unchanged until 2003. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

INTRODUCTION

This part of IEC 60747 should be read in conjunction with IEC 60747-1. It provides basic information on

- terminology,
- letter symbols,
- essential ratings and characteristics,
- measuring methods,
- acceptance and reliability.

SEMICONDUCTOR DEVICES –

Part 8: Field-effect transistors

1 Scope

This part of IEC 60747 gives standards for the following categories of field-effect transistors:

- type A: junction-gate type;
- type B: insulated-gate depletion type;
- type C: insulated-gate enhancement type.

2 Normative references

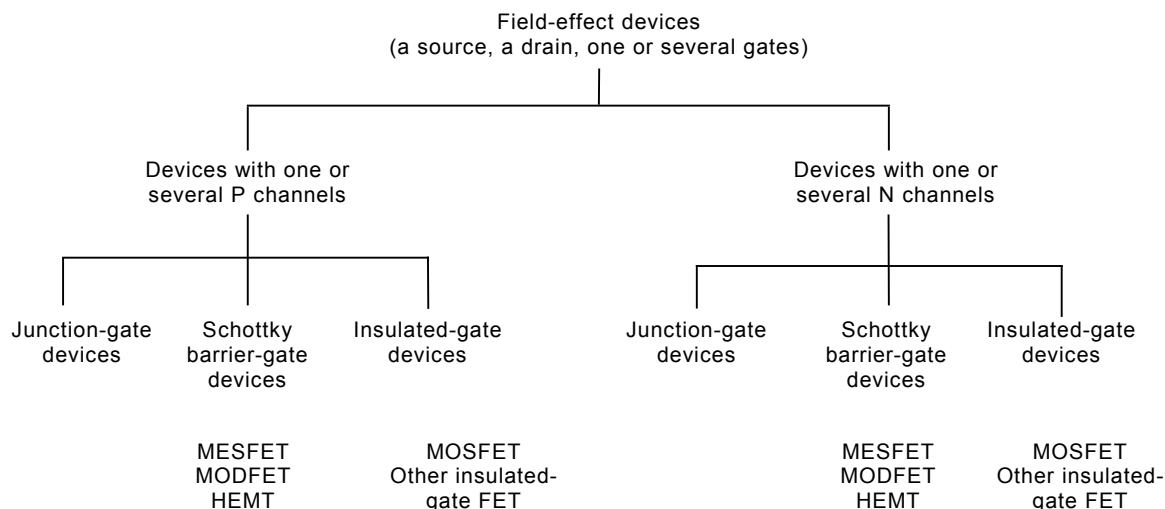
The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 60747. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of IEC 60747 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 60747-1:1983, *Semiconductor devices – Discrete devices and integrated circuits – Part 1: General*

IEC 60747-7:2000, *Semiconductor devices – Part 7: Bipolar transistors*

3 Classification

Since a field-effect transistor may have one or several gates, the following classification results:



NOTE Schottky barrier-gate and insulated gate devices have depletion type devices and enhancement type devices.

4 Terminology and letter symbols

For the purpose of this part of IEC 60747, the following definitions and symbols apply:

4.1 Types of field-effect transistors

4.1.1

N-channel field-effect transistor

a field-effect transistor that has one or more N-type conduction channels

4.1.2

P-channel field-effect transistor

a field-effect transistor that has one or more P-type conduction channels

4.1.3

junction-gate field-effect transistor (JFET)

a field-effect transistor in which:

- the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;
- a gate region adjacent to the channel has the opposite conductivity type, thus forming with source, channel and drain region a PN junction, and
- the gate-source voltage controls the conductivity of the conduction channel in the channel region by controlling the width of the gate space-charge region and hence also the remaining cross-section of the conduction channel

4.1.4**insulated-gate field-effect transistor (IGFET)**

a field-effect transistor in which:

- one or more gate electrodes are electrically insulated from the body;
- the conductivity type of both the source and drain regions is opposite from that of the semiconductor body in which they are located;
- the principal current flows in a channel that is formed by an inversion layer connecting source and drain regions;
- the inversion layer is either already present at zero gate-source voltage or produced within the body at sufficiently high forward gate-source voltage by accumulation of the minority charge carriers of the body material, and
- the conductance of the channel is controlled by the gate-source voltage, which controls the electric field between gate electrode and the body and hence the amount of accumulated minority charge carriers

4.1.5**metal-oxide-semiconductor field-effect transistor (MOSFET)**

an insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material

4.1.6**depletion-type field-effect transistor**

a field-effect transistor in which an inversion layer present at the surface of the active semiconductor region causes an appreciable channel conductance that may be increased (decreased) by applying a forward (reverse) gate-source voltage

4.1.7**enhancement-type field-effect transistor**

a field-effect transistor having substantially zero channel conductance at zero gate-source voltage, and in which a conduction channel may be obtained by applying a sufficiently high forward gate-source voltage, which induces an inversion layer below the gate electrode

4.1.8**single-gate field-effect transistor**

a field-effect transistor having a gate region, a source region, and a drain region

NOTE The term may be abbreviated to "field-effect transistor", if no ambiguity is likely to occur.

4.1.9**dual-gate field-effect transistor**

a field-effect transistor having two independent gate regions, a source region, and a drain region

4.1.10**Schottky-barrier-gate field-effect transistor**

a field-effect transistor in which:

- the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;
- one or more gate electrodes each form a Schottky-barrier with the channel region;
- the gate-source voltage controls the conductance of the conduction channel by varying its cross-section

4.1.11

metal-semiconductor field-effect transistor (MESFET)

a Schottky-barrier-gate field-effect transistor in which the gate electrodes are metal

4.1.12

modulation-doped field-effect transistor (MODFET) or high electron mobility transistor (HEMT)

a metal-semiconductor field-effect transistor in which a doped material forms a heterojunction with an undoped channel; the doped material supplies electrons to the undoped channel whose high electron mobility results in enhanced channel conductance

NOTE MODFET and HEMT may be used interchangeably.

4.2 General terms

4.2.1 Physical region (of a field-effect transistor)

4.2.1.1

source region (of a field-effect transistor)

the physical region that is designed by the manufacturer to contain the supply region under the defined operating conditions to which the specifications refer

4.2.1.2

drain region (of a field-effect transistor)

the physical region that is designed by the manufacturer to contain the collection region under the defined operating conditions to which the specifications refer

4.2.1.3

gate region of an IGFET

the insulating layer between the gate electrode and the surface of the semiconductor body, below which the channel is or may be formed

4.2.1.4

gate region of an JFET

the region below the gate electrode that is of opposite conductivity type from that of the source, channel and drain regions

4.2.1.5

channel region of a depletion-type IGFET

the inversion layer technologically placed below the gate region

4.2.1.6

channel region of a JFET

the region between source region and drain region that has the same conductivity type as these two regions

4.2.1.7

subchannel region of an IGFET

the region between source region and drain region, excluding the channel region of a depletion-type IGFET and all pertinent transition zones

4.2.1.8

substrate (of a JFET or IGFET)

- 1) the part of the original material that remains unchanged when the device elements are formed upon or within the original material

NOTE The original material may be a layer of semiconductor material cut from a single crystal, a layer of semiconductor material deposited on a supporting base, or the supporting base itself.

- 2) the original semiconductor material before being processed

NOTE The intended meaning will become clear from the context in which the term is used. If necessary, distinction could be made between the "original substrate" and the "remaining substrate".

4.2.1.9

substrate (of a thin film field effect transistor)

an insulator that supports the source and drain electrodes, the insulating gate layer, and the thin semiconductor layer

4.2.2 Functional regions

4.2.2.1

functional source region

a supply region that delivers principal-current charge carriers into the channel

4.2.2.2

functional drain region

a collection region that acquires principal-current charge carriers from the channel

4.2.2.3

channel of a IGFET

the functional region through which the principal-current charge carriers pass and in which the carrier concentration is determined by the gate-source voltage, the principal current being the result of the drift field produced by the drain-source voltage

4.2.2.4

channel of a JFET

the functional region through which the principal-current charge carriers pass and whose cross-section is determined by the applied gate-source voltage, the principal current being the result of the drift field produced by the drain-source voltage

4.2.2.5

subchannel space-charge region of an IGFET

the space-charge region associated with the transition regions between the subchannel region on one side, and source region, channel region and drain region on the other side

4.2.2.6

functional subchannel region

the remaining neutral part of the (physical) subchannel region that is confined by the surrounding subchannel space-charge region

4.3 Terms related to ratings and characteristics

NOTE When several distinctive forms of a letter symbol exist, the most commonly used form is given.

4.3.1

"reverse" and "forward" directions

here "reverse" means: the direction in which the channel carriers are decreased (depleted), and "forward" means: the direction in which the channel carriers are increased (enhanced)

4.3.2

threshold voltage (of an enhancement type field-effect transistor) ($V_{GS(TO)}$)

the gate-source voltage at which the magnitude of the drain current reaches a specified low value

4.3.3

cut-off voltage (of a depletion type field-effect transistor) ($V_{GS(off)}$)

the gate-source voltage at which the magnitude of the drain current reaches a specified low value

4.3.4

gate cut-off current (of a junction-gate field-effect transistor)

the current flowing in the gate terminal of a junction field-effect transistor when the gate junction is biased in the reverse direction

4.3.5

gate leakage current (of an insulated-gate field-effect transistor)

the leakage current flowing in the gate terminal of an insulated-gate field-effect transistor

4.3.6 Capacitances

4.3.6.1

(short-circuit) input capacitance C_{iss}

the capacitance between the gate and source terminals with the drain terminal short-circuited to the source terminal for a.c. signals

4.3.6.2

(short-circuit) output capacitance C_{oss}

the capacitance between the drain and source terminals with the gate terminal short-circuited to the source terminal for a.c. signals

4.3.6.3

(short-circuit) reverse transfer capacitance C_{rss}

the capacitance between the drain and gate terminals with the source terminal short-circuited to the gate terminal for a.c. signals

4.3.7

gate-source resistance r_{GS}

the d.c. resistance between gate and source terminals at specified gate-source and drain-source voltages

4.3.8

drain-source on-state resistance $r_{DS(on)}$

the d.c. resistance between the drain and source terminals when the FET is in its on-state

4.3.9 gate charge Q_{gs}
the charge required to raise the gate-source voltage from zero to a specified value

4.4 Letter symbols

4.4.1 General

Clauses 2, 3 and 4, chapter V of IEC 60747-1 apply.

4.4.2 Additional general subscripts

In addition to the list of recommended general subscripts given in 2.2.1, chapter V of IEC 60747-1, the following special subscripts are recommended for field-effect transistors:

- D, d = drain
- G, g = gate
- S, s = source
- B, b; U, u = substrate
- T; th; (TO) = threshold

4.4.3 List of letter symbols

Name and designation	Letter symbol	Remarks
4.4.3.1 Voltage		
Drain-source (d.c.) voltage	V_{DS}	
Gate-source (d.c.) voltage	V_{GS}	
Gate-source cut-off voltage (of a junction field-effect transistor and of a depletion type insulated-gate field-effect transistor)	$V_{GS(OFF)}$; V_{GSoff}	
Gate-source threshold voltage (of an enhancement type insulated-gate field-effect transistor)	V_{GST} ; $V_{GS(th)}$; $V_{GS(TO)}$	
Forward gate-source (d.c.) voltage	V_{GSF}	
Reverse gate-source (d.c.) voltage	V_{GSR}	
Gate-drain (d.c.) voltage	V_{GD}	
Source-substrate (d.c.) voltage	V_{SB} ; V_{SU}	
Drain-substrate (d.c.) voltage	V_{DB} ; V_{DU}	
Gate-substrate (d.c.) voltage	V_{GB} ; V_{GU}	
Gate-gate voltage (for multi-gate devices)	$V_{G1 - G2}$	
Gate-source breakdown voltage with drain short-circuited to source	$V_{(BR)GSS}$	

Name and designation	Letter symbol	Remarks
4.4.3.2 Currents		
Drain (d.c.) current	I_D	
Drain current, at a specified gate-source condition	I_{DSX}	
Drain current, at a specified external gate-source resistance	I_{DSR}	
Drain current, with gate short-circuited to source ($V_{GS} = 0$)	I_{DSS}	
Source (d.c.) current	I_S	
Source current, at a specified gate-drain condition	I_{SDX}	
Source current, with gate short-circuited to drain ($V_{GD} = 0$)	I_{SDS}	
Gate (d.c.) current	I_G	
Forward gate current	I_{GF}	
Gate cut-off current (of a junction field-effect transistor), with source open-circuited	I_{GDO}	
Gate-cut-off current (of a junction field-effect transistor), with drain open-circuited	I_{GSO}	
Gate cut-off current (of a junction field-effect transistor), with drain short-circuited to source	I_{GSS}	
Gate leakage current (of an insulated-gate field-effect transistor), with drain short-circuited to source	I_{GSS}	
Gate cut-off current (of a junction field-effect transistor), with specified drain-source circuit conditions	I_{GSX}	
Substrate current	$I_B; I_U$	
4.4.3.3 Power dissipation		
Drain-source (d.c.) power dissipation	P_{DS}	

Name and designation	Letter symbol	Remarks
4.4.3.4 Resistances (or conductances) and capacitances		
Drain-source resistance Gate-source resistance Gate-drain resistance Gate resistance (with $V_{DS} = 0$ or $v_{ds} = 0$)	$r_{DS}; r_{ds}$ $r_{GS}; r_{gs}$ $r_{GD}; r_{gd}$ $r_{GSS}; r_{gss}$	
Drain-source on-state resistance	$r_{DS(ON)}; r_{ds(on)}; r_{DSon}$	
Drain-source off-state resistance	$r_{DS(OFF)}; r_{ds(off)}; r_{DSoff}$	
Open-circuit gate-source capacitance (drain-source and gate-drain open-circuited to a.c.)	C_{gso}	
Open-circuit gate-drain capacitance (drain-source and gate-source open-circuited to a.c.)	C_{gdo}	
Open-circuit drain-source capacitance (gate-drain and gate-source open-circuited to a.c.)	C_{dso}	
Short-circuit input capacitance in common-source configuration; gate-source capacitance (drain-source short-circuited to a.c.)	$C_{iss}; C_{11ss}$	
Short-circuit output capacitance in common-source configuration; drain-source capacitance (gate-source short-circuited to a.c.)	$C_{oss}; C_{22ss}$	
Short-circuit input conductance in common-source configuration	g_{iss}	
Short-circuit output conductance in common-source configuration	g_{oss}	
Common-source reverse transfer capacitance with input short-circuited to a.c.	$C_{rss}; C_{12ss}$	
Short-circuit output capacitance in common-drain configuration (gate-drain short-circuited to a.c.)	$C_{ods}; C_{22ds}$	

Name and designation	Letter symbol	Remarks
4.4.3.5 Small-signal parameters (see figures 1, 2 and 3)		
Short-circuit input admittance	$y_{is} = \text{Re}_{(y_{is})} + j\omega C_{is}$ $y_{11s} = \text{Re}_{(y_{11s})} + j\omega C_{11s}$	
Short-circuit reverse transfer admittance	$y_{rs} = \text{Re}_{(y_{rs})} + j\omega C_{rs}$ $y_{12s} = \text{Re}_{(y_{12s})} + j\omega C_{12s}$	
Short-circuit forward transfer admittance	$y_{fs} = \text{Re}_{(y_{fs})} + j\text{Im}_{y_{fs}}$ $y_{21s} = \text{Re}_{(y_{21s})} + j\text{Im}_{y_{21s}}$	
Short-circuit output admittance	$y_{os} = \text{Re}_{(y_{os})} + j\omega C_{os}$ $y_{22s} = \text{Re}_{(y_{22s})} + j\omega C_{22s}$	
Modulus of the short-circuit reverse transfer admittance	$ y_{rs} ; y_{12s} $	
Phase of the short-circuit reverse transfer admittance	$\phi_{yrs}; \phi_{y12s}$	
Modulus of the short-circuit forward transfer admittance	$ y_{fs} ; y_{21s} $	
Phase of the short-circuit forward transfer admittance	$\phi_{yfs}; \phi_{y21s}$	
Gate-source conductance (in the π equivalent circuit)	g_{gs}	
Gate-drain conductance (in the π equivalent circuit)	g_{gd}	
Drain-source conductance (in the π equivalent circuit)	g_{ds}	
Forward transconductance (in the π equivalent circuit)	$g_{ms}; g_m$	
Gate-source capacitance (in the π equivalent circuit)	C_{gs}	
Gate-drain capacitance (in the π equivalent circuit)	C_{gd}	
Drain-source capacitance (in the π equivalent circuit)	C_{ds}	

Name and designation	Letter symbol	Remarks
4.4.3.5 Small-signal parameters (continued)		
Input reflection coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	S_{11s} OR S_{is} S_{11g} OR S_{ig} S_{11d} OR S_{id}	
Output reflection coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	S_{22s} OR S_{os} S_{22g} OR S_{og} S_{22d} OR S_{od}	
Forward transmission coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	S_{21s} OR S_{fs} S_{21g} OR S_{fg} S_{21d} OR S_{fd}	
Reverse transmission coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	S_{12s} OR S_{rs} S_{12g} OR S_{rg} S_{12d} OR S_{rd}	
4.4.3.6 Other parameters		
Power gain	G_P ; G_p	
Cut-off frequency (in the common-source configuration)	f_{yfs}	
Noise voltage	V_n	
Noise figure	F	
Temperature coefficient of drain current	α_{ID}	
Temperature coefficient of drain-source resistance	α_{rds}	
Turn-on delay time	$t_{d(on)}$	Switching times (see figure 4) $t_{on} = t_{d(on)} + t_r$ $t_{off} = t_{d(off)} + t_f$
Turn-off delay time	$t_{d(off)}$	
Rise time	t_r	
Fall time	t_f	
Turn-on time	t_{on}	
Turn-off time	t_{off}	
Frequency of unity forward transmission coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	f_{ss} OR f_{iss} f_{sg} OR f_{isg} f_{sd} OR f_{isd}	$f_{ss} = f$ for $ S_{21s} = 1$ $f_{sg} = f$ for $ S_{21g} = 1$ $f_{sd} = f$ for $ S_{21d} = 1$