



BSI Standards Publication

Semiconductor devices — Discrete devices

Part 8: Field-effect transistors

National foreword

This British Standard is the UK implementation of IEC 60747-8:2010, including amendment 1:2021. It supersedes BS IEC 60747-8:2010, which is withdrawn.

The text of IEC amendment 1:2021 has been provided in its entirety at the beginning of this document. BSI's policy of providing consolidated content remains unchanged; however, in the interest of expediency, in this instance BSI have chosen to collate the relevant content at the beginning of this document.

The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors.

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INTERNATIONAL STANDARD

AMENDMENT 1

Semiconductor devices – Discrete devices – Part 8: Field-effect transistors

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COMMISSION

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**SEMICONDUCTOR DEVICES –
DISCRETE DEVICES –****Part 8: Field-effect transistors****AMENDMENT 1****FOREWORD**

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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Amendment 1 to IEC 60747-8:2021 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices.

The text of this Amendment is based on the following documents:

Draft	Report on voting
47E/726/CDV	47E/744/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Amendment is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications/.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

3.4 Conventional used terms

Replace the existing Table 1 title and whole table in this subclause with the following new Table 1:

Table 1 – Terms for MOSFET in this document and the conventional used terms for the inverse diode integrated in the MOSFETs for N-channel

Preferred terms	Letter symbol	Deprecated terms for inverse diode with MOSFET in off-state
Drain-source reverse voltage	V_{SD}	Inverse diode forward voltage
MOSFET forward recovery current	I_{fr}	Inverse diode reverse recovery current
MOSFET peak forward recovery current	I_{frm}	Inverse diode peak reverse recovery current
MOSFET forward recovery time	t_{fr}	Inverse diode reverse recovery time
MOSFET forward recovery charge	Q_f	Inverse diode reverse recovery charge
MOSFET forward recovery energy	E_{fr}	Inverse diode reverse recovery energy
Reverse drain current	I_S	Inverse diode forward current
Repetitive peak reverse drain current	I_{SRM}	Inverse diode repetitive peak forward current

4.3.2 Currents

Delete, in this subclause, the existing third item I_{DRM} .

Replace, in 4.3.2, the existing seventh item with the following new item:

Source (d.c.) current (for P-channel)	I_S	
---------------------------------------	-------	--

Add, after the new item " Source (d.c.) current (for P-channel) I_S ", the following new item:

Peak source current (for P-channel)	I_{SM}	
-------------------------------------	----------	--

Replace, in this subclause, the existing eighth item with the following new item:

Source current, at a specified gate-drain condition (for P-channel)	I_{SDX}	
---	-----------	--

Replace, in this subclause, the existing ninth item with the following new item:

Source current, with gate short-circuited to drain ($V_{GD} = 0$) (for P-channel)	I_{SDS}	
---	-----------	--

Delete, in this subclause, the existing tenth item I_G .

4.3.7 Inverse diodes integrated in MOSFETs

Replace the existing title of 4.3.7 with the following new title.

Replace, in 4.3.7, the existing first, second, third and seventh items with the following new items:

4.3.7 Inverse diodes integrated in MOSFETs for N-channel		
Drain-source reverse voltage	V_{SD}	Forward voltage of the inverse diode
MOSFET forward recovery current	I_{fr}	Reverse recovery current of the inverse diode
MOSFET peak forward recovery current	I_{frm}	Peak reverse recovery current of the inverse diode
Reverse drain current	I_S	Forward current of the inverse diode

Add, in 4.3.7, the following new item:

Repetitive peak reverse drain current	I_{SRM}	Repetitive peak forward current of the inverse diode
---------------------------------------	-----------	--

5.2.4.8 Maximum continuous (d.c.) reverse drain current (I_{DR})

(forward current of the inverse diode)

5.2.4.9 Maximum peak reverse drain current (I_{DRM}) (Maximum peak

forward current of the inverse diode)

Replace the existing Subclauses 5.2.4.8 and 5.2.4.9 with the following new subclauses:

		TYPES		
		A	B	C
5.2.4.8	Maximum continuous (d.c.) reverse drain current (I_S) (forward current of the inverse diode)		+	+
5.2.4.9	Maximum peak reverse drain current (I_{SM}) (Maximum peak forward current of the inverse diode)		+	+

Under specified pulse conditions.

5.3.3.10.1 Drain-source reverse voltage (V_{DSR}) (Forward voltage of the inverse diode)

5.3.3.10.3 Peak forward recovery current (I_{FRM}) (Peak reverse recovery current of the inverse diode)

Replace the existing Subclauses 5.3.3.10.1 and 5.3.3.10.3 with the following new subclauses:

5.3.3.10.1 Drain-source reverse voltage (V_{SD}) (Forward voltage of the inverse diode)

Maximum value at specified reverse drain current (I_S) (forward current of the inverse diode) and at $V_{GS} = 0$.

5.3.3.10.3 Peak forward recovery current (I_{frm}) (Peak reverse recovery current of the inverse diode)

Maximum value under specified conditions.

TYPES		
A	B	C
	+	+
	+	+

5.3.4.9.1 Reverse drain current (I_{DR}) (forward current of the inverse diode)

Replace the existing Subclause 5.3.4.9.1 with the following new subclause:

5.3.4.9.1 Reverse drain current (I_S) (forward current of the inverse diode)

Maximum value at specified Reverse drain current (I_S) and at $V_{GS} = 0$.

TYPES		
A	B	C
	+	+

6.2.1.6 Reverse drain current (I_{DRS}) or (I_{DRX})

Replace the existing title of 6.2.1.6 with the following new title:

6.2.1.6 Reverse drain current (I_{SS}) or (I_{SX})

Replace, in the paragraph "Specified conditions", the existing fourth bullet with the following new condition:

- Reverse drain current I_S

6.2.1.7 Peak reverse drain current (I_{DRM})

Replace the existing title of 6.2.1.7 with the following new title:

6.2.1.7 Peak reverse drain current (I_{SM})

Replace the existing Figure 10 with the following new Figure 10:

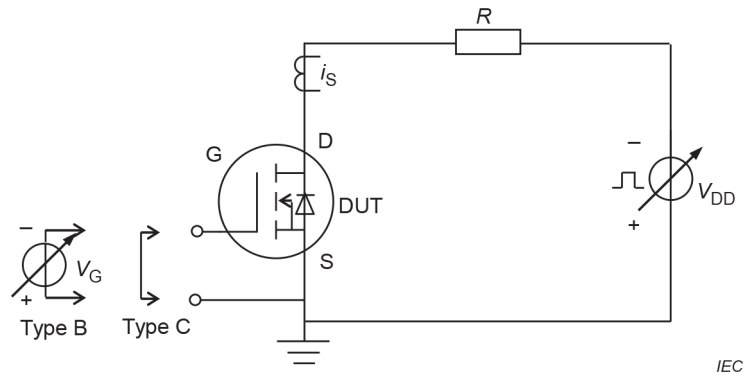


Figure 10 – Basic circuit for the testing of peak reverse drain current of MOSFETs

Replace, under "Specified conditions", the existing fourth bullet with the following new bulleted point:

- Peak reverse drain current I_{SM}

6.2.2.2 Reverse-bias safe operation area (RBSOA)

Replace, in 6.2.2.2, the first paragraph of the existing testing procedure with the following:

DUT is turned off at specified I_D and V_{DS} . I_D and V_{DS} are monitored. The DUT has to turn off I_D and withstand $V_{DS} = V_{DS(clamp)}$.

Figure 34 – Current waveform through MOSFET (Method 1)

Replace the existing Figure 34 with the following new Figure 34:

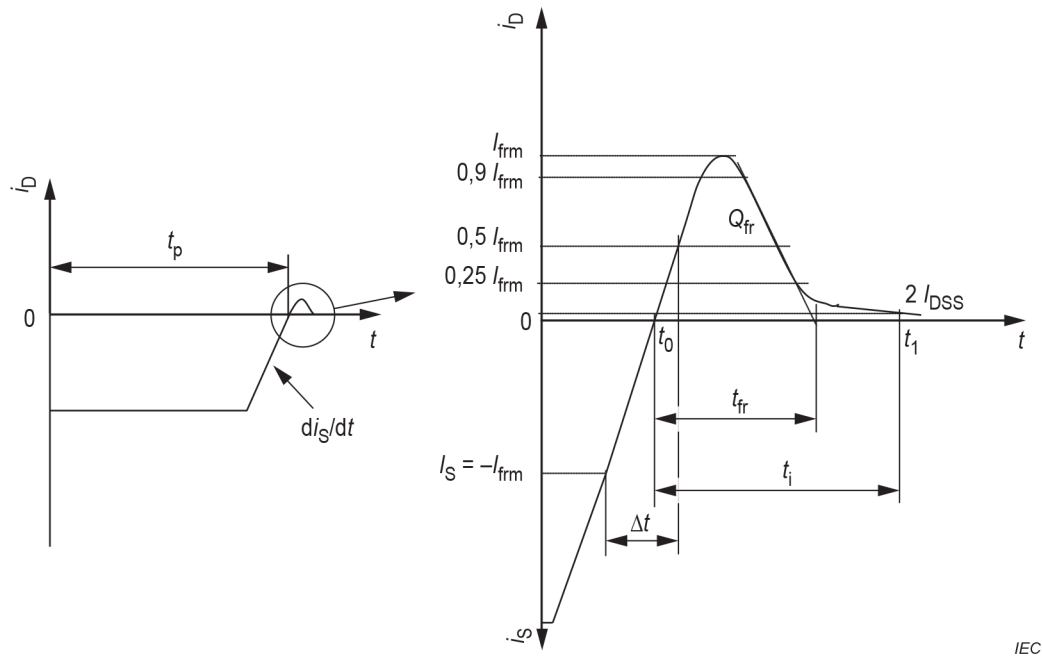


Figure 34 – Current waveform through MOSFET (Method 1)

6.3.14 MOSFET forward recovery time (t_{fr}) and MOSFET forward recovered charge (Q_f)

Replace, in 6.3.14, Method 1, under "– Circuit description and requirements", "MOSFET T" with "MOSFET T" and the letter symbol " di_{DR}/dt " with " di_S/dt ".

Replace, in 6.3.14, Method 1, the existing text under "Measurement procedure" with the following new sentences:

MOSFET T is turned on and turned off twice, and then the second turn-on is observed. Waveforms of the current I_S are monitored. The recovered charge is measured as

$$Q_f = \int_{t_0}^{t_0 + t_i} i_S \cdot dt$$

where

t_0 is the instant when the current passes through zero;

t_i is the integration time.

Integral end time t_1 is the time when forward drain current reaches $2 \times I_{DSS}$, preferably equal to the specified maximum value of t_{fr} . Δt can be adjusted by MOSFET T driving conditions, such as V_G and/or R . The forward recovery time t_{fr} is measured as the interval between the time of t_0 when the drain current passes through zero and the time when, for decreasing values of I_D , a line through the points for $0.9 I_{frm}$ and $0.25 I_{frm}$ crosses the zero current axis.

Replace, in Subclause 6.3.14, Method 1, the existing second and third bullets under "Specified conditions" with the following new bulleted points:

- Peak reverse drain current I_{SM}

- Rate of change of drain current di_S/dt

Figure 36 – Current waveform through MOSFET (Method 2)

Replace the existing Figure 36 with the following new figure:

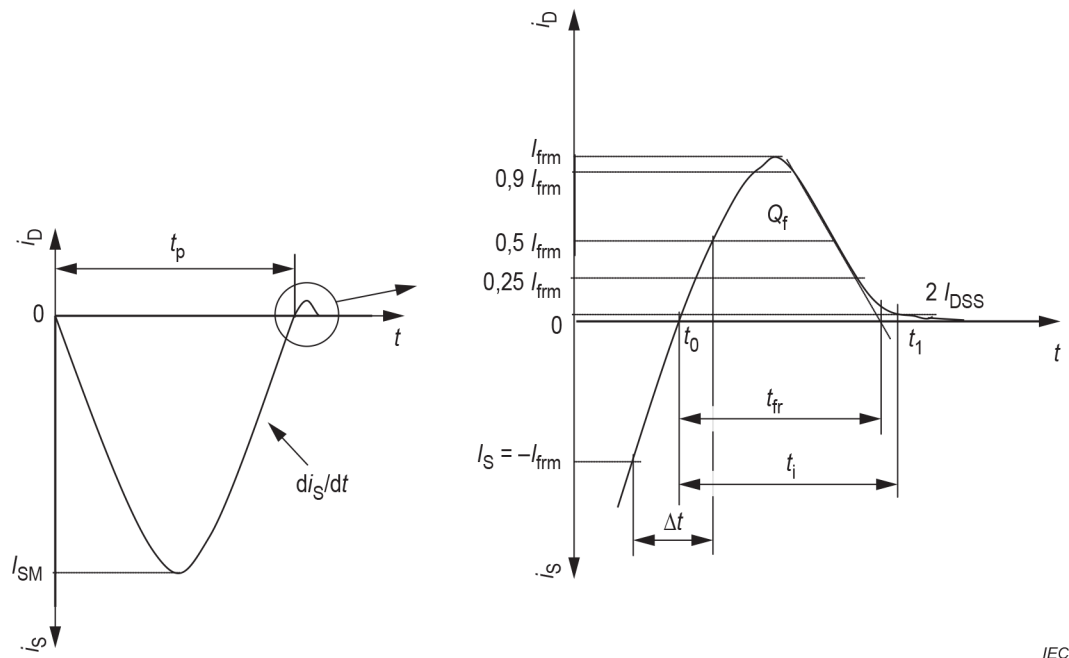


Figure 36 – Current waveform through MOSFET (Method 2)

Replace, in 6.3.14, Method 2, first paragraph of the measurement procedure, the letter symbols " I_{DRM} " with " I_{SM} ", " di_{DR}/dt " with " di_S/dt " and " I_{FRM} " with " I_{frm} ".

Replace, in 6.3.14, Method 2, the existing second and third bullets under "Specified conditions" with the following new bullets:

- Peak drain reverse current I_{frm}
- Rate of change of drain current di_S/dt

Replace, in 6.3.14, Method 2, the existing note with the following new note:

NOTE The rate of change of drain current is measured at zero crossing current, for example over time Δt , between current values of $I_S = -I_{DM}$ and $I_S = 0,5 I_{DM}$.

6.3.15 Drain-source reverse voltage (V_{DSR})

Replace the existing title of 6.3.15 with the following new title:

6.3.15 Drain-source reverse voltage (V_{SD})

Replace the existing sentence of 6.3.15, under "- Purpose" with the following new sentence:

To measure the drain-source reverse voltage V_{SD} under specified conditions.

Replace, in 6.3.15, the existing second bullet under "Specified conditions" with the following new bulleted point:

- Reverse drain current I_S

7.4.2 Routine tests

Replace, in Table 4, the existing cross-references to 6.1.1.6, 6.1.1.7 and 6.2.15 with the following new items:

Subclause		Type test	Routine test
6.1.1.6	Reverse drain current (I_{SS}) or (I_{SX})	X	
6.1.1.7	Peak reverse drain current (I_{SM})	X	X
6.2.15	Drain-source reverse voltage (V_{SD})	X	



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INTERNATIONAL STANDARD

NORME INTERNATIONALE

**Semiconductor devices – Discrete devices –
Part 8: Field-effect transistors**

**Dispositifs à semiconducteurs – Dispositifs discrets –
Partie 8: Transistors à effet de champ**

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**SEMICONDUCTOR DEVICES –
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FOREWORD

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International Standard IEC 60747-8 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This third edition of IEC 60747-8 cancels and replaces the second edition published in 2000. This third edition constitutes a technical revision.

The main changes with respect to the previous edition are listed below.

- a) "Clause 3 Classification" was moved and added to Clause 1.
- b) "Clause 4 Terminology and letter symbols" was divided into "Clause 3 Terms and definitions" and "Clause 4 Letter symbols" was amended with additions and deletions.
- c) Clause 5, 6 and 7 were amended with necessary additions and deletions.

The text of this standard is based on the following documents:

FDIS	Report on voting
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Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

This Part 8 should be used in conjunction with IEC 60747-1:2006.

A list of all the parts in the IEC 60747 series, under the general title *Semiconductor devices – Discrete devices*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

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SEMICONDUCTOR DEVICES – DISCRETE DEVICES –

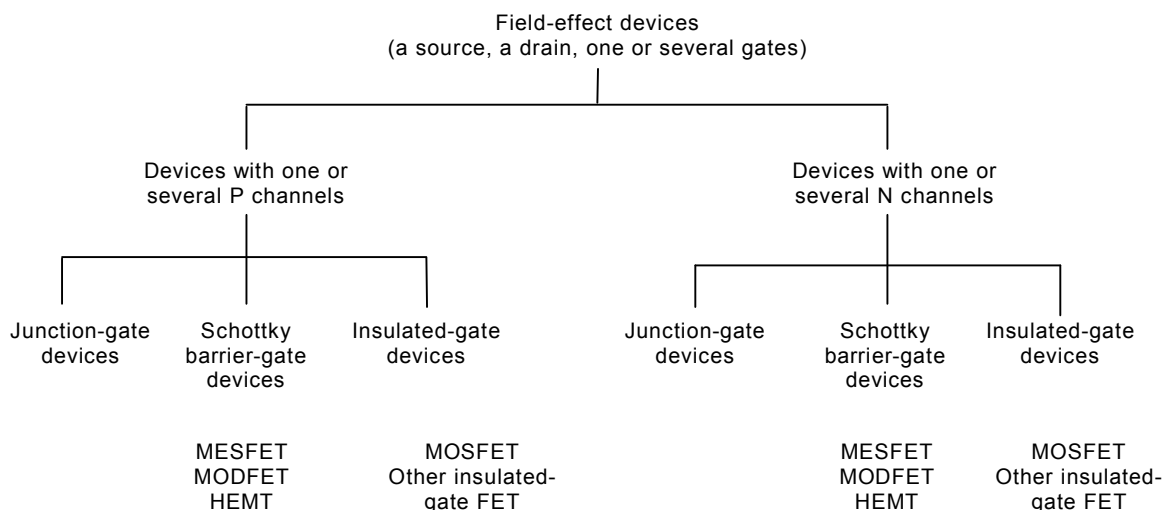
Part 8: Field-effect transistors

1 Scope

This part of IEC 60747 gives standards for the following categories of field-effect transistors:

- type A: junction-gate type;
- type B: insulated-gate depletion (normally on) type;
- type C: insulated-gate enhancement (normally off) type.

Since a field-effect transistor may have one or several gates, the classification shown below results:



NOTE 1 Schottky barrier-gate and insulated gate devices include depletion type devices and enhancement type devices.

NOTE 2 MOSFETs for some applications may not have inverse diode characteristics in the data sheet. Special circuit element structures to eliminate body diode are under development for such applications. MOSFET applications such as motor control equipment need to specify the inverse diode characteristics in the MOSFET to use the inverse diode as a free wheeling diode.

NOTE 3 The graphical symbol only for type C is used in this standard. The standard equally applies for P-channel and for type A and B devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61340 (all parts), *Electrostatics*

IEC 60747-1:2006, *Semiconductor devices – Part 1: General*

IEC 60747-7:2000, *Semiconductor devices – Part 7: Bipolar transistors*

IEC 60749-23:2004, *Semiconductor devices – Mechanical and climatic test methods – Part 23: High temperature operating life*

IEC 60749-34, *Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling*

3 Terms and definitions

For the purpose of this document, the following terms and definitions apply.

3.1 Types of field-effect transistors

3.1.1

N-channel field-effect transistor

field-effect transistor that has one or more N-type conduction channels

3.1.2

P-channel field-effect transistor

field-effect transistor that has one or more P-type conduction channels

3.1.3

junction-gate field-effect transistor

JFET

field-effect transistor in which

- the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;
- a gate region adjacent to the channel has the opposite conductivity type, thus forming with source, channel and drain region a PN junction

NOTE The gate-source voltage controls the conductivity of the conduction channel in the channel region by controlling the width of the gate space-charge region and hence also the remaining cross-section of the conduction channel.

3.1.4

insulated-gate field-effect transistor

IGFET

field-effect transistor in which

- one or more gate electrodes are electrically insulated from the body;
- the conductivity type of both the source and drain regions is opposite from that of the semiconductor body in which they are located;
- the principal current flows in a channel that is formed by an inversion layer connecting source and drain regions

NOTE The inversion layer is either already present at zero gate-source voltage or produced within the body at sufficiently high forward gate-source voltage by accumulation of the minority charge carriers of the body material. The conductance of the channel is controlled by the gate-source voltage, which controls the electric field between gate electrode and the body and hence the amount of accumulated minority charge carriers.

3.1.5

metal-oxide-semiconductor field-effect transistor

MOSFET

insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material

3.1.6

depletion-type (normally on) field-effect transistor

field-effect transistor in which an inversion layer present at the surface of the active semiconductor region causes an appreciable channel conductance that may be increased (decreased) by applying a forward (reverse) gate-source voltage

3.1.7

enhancement-type (normally off) field-effect transistor

field-effect transistor having substantially zero channel conductance at zero gate-source voltage, and in which a conduction channel may be obtained by applying a sufficiently high forward gate-source voltage, which induces an inversion layer below the gate electrode

3.1.8

single-gate field-effect transistor

field-effect transistor having a gate region, a source region, and a drain region

NOTE The term may be abbreviated to "field-effect transistor", if no ambiguity is likely to occur.

3.1.9

dual-gate field-effect transistor

field-effect transistor having two independent gate regions, a source region, and a drain region

3.1.10

schottky-barrier-gate field-effect transistor

field-effect transistor in which

- the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;
- one or more gate electrodes each form a Schottky-barrier with the channel region;

the gate-source voltage controls the conductance of the conduction channel by varying its cross-section

3.1.11

metal-semiconductor field-effect transistor

MESFET

Schottky-barrier-gate field-effect transistor in which the gate electrodes are metal

3.1.12

modulation-doped field-effect transistor or high electron mobility transistor MODFET or HEMT

metal-semiconductor field-effect transistor in which a doped material forms a heterojunction with an undoped channel; the doped material supplies electrons to the undoped channel whose high electron mobility results in enhanced channel conductance

NOTE MODFET and HEMT should be used interchangeably.

3.2 General terms

3.2.1 Physical regions (of a field-effect transistor)

3.2.1.1

source (of a field-effect transistor)

physical region that is designed by the manufacturer to contain the supply region under the defined operating conditions to which the specifications refer

3.2.1.2**drain (of a field-effect transistor)**

physical region that is designed by the manufacturer to contain the collection region under the defined operating conditions to which the specifications refer

3.2.1.3**gate (of an IGFET)**

insulating layer between the gate electrode and the surface of the semiconductor body, below which the channel is or may be formed

3.2.1.4**gate (of an JFET)**

region below the gate electrode that is of opposite conductivity type from that of the source, channel and drain regions

3.2.1.5**channel (of a depletion-type IGFET)**

inversion layer technologically placed below the gate region

3.2.1.6**channel (of a JFET)**

region between source region and drain region that has the same conductivity type as these two regions

3.2.1.7**subchannel (of an IGFET)**

region between source region and drain region, excluding the channel region of a depletion-type IGFET and all pertinent transition zones

3.2.1.8**substrate (of a JFET or IGFET)**

part of the original material that remains unchanged when the device elements are formed upon or within the original material

NOTE The original material may be a layer of semiconductor material cut from a single crystal, a layer of semiconductor material deposited on a supporting base, or the supporting base itself.

3.2.1.9**substrate (of a JFET or IGFET)**

original semiconductor material before being processed

NOTE The intended meaning will become clear from the context in which the term is used. If necessary, distinction could be made between the "original substrate" and the "remaining substrate".

3.2.1.10**substrate (of a thin-film field-effect transistor)**

insulator that supports the source and drain electrodes, the insulating gate layer, and the thin semiconductor layer

3.2.2 Functional regions**3.2.2.1****functional source region**

supply region that delivers principal-current charge carriers into the channel

3.2.2.2**functional drain region**

collection region that acquires principal-current charge carriers from the channel

3.2.2.3

channel (of a IGFET)

functional region through which the principal-current charge carriers pass and in which the carrier concentration is determined by the gate-source voltage, the principal current being the result of the drift field produced by the drain-source voltage

3.2.2.4

channel (of a JFET)

functional region through which the principal-current charge carriers pass and whose cross-section is determined by the applied gate-source voltage, the principal current being the result of the drift field produced by the drain-source voltage

3.2.2.5

subchannel space-charge region (of an IGFET)

space-charge region associated with the transition regions between the subchannel region on one side, and source region, channel region and drain region on the other side

3.2.2.6

functional subchannel region

remaining neutral part of the (physical) subchannel region that is confined by the surrounding subchannel space-charge region

3.3 Terms related to ratings and characteristics

3.3.1

gate cut-off current (of a junction-gate field-effect transistor)

current flowing in the gate terminal of a junction field-effect transistor when the pn junction is biased in the reverse direction

3.3.2

gate leakage current (of an insulated-gate field-effect transistor)

leakage current through the insulated-gate of an insulated-gate field-effect transistor

3.3.3

capacitances

3.3.3.1

(short-circuit) input capacitance

capacitance between the gate and source terminals with the drain terminal short-circuited to the source terminal for a.c. signals

3.3.3.2

(short-circuit) output capacitance

capacitance between the drain and source terminals with the gate terminal short-circuited to the source terminal for a.c. signals

3.3.3.3

reverse transfer capacitance

capacitance between the drain and gate terminals excluding parallel capacitances between drain and source, and gate and source

3.3.4

gate-source resistance

d.c. resistance between gate and source terminals at specified gate-source and drain-source voltages

3.3.5

drain-source on-state resistance

d.c. resistance between the drain and source terminals when the FET is in its on-state

3.3.6**gate charge**

charge required to raise the gate-source voltage from zero to a specified value

3.3.6.1**total gate charge**

charge that is required to raise the gate-source voltage from zero to a specified value and calculated by the equation below (see Figure 1)

$$Q_G = \int_{t_0}^{t_4} i_{GG}(t) dt$$

3.3.6.2**threshold gate charge**

charge required to raise gate-source from zero to $V_{GS(th)}$ and calculated by the equation below (see Figure 1)

$$Q_{GS(th)} = \int_{t_0}^{t_1} i_{GG}(t) dt$$

3.3.6.3**plateau gate charge**

charge required to raise gate-source voltage from zero to plateau voltage $V_{GS(pl)}$ and calculated by the equation below (see Figure 1)

$$Q_{GS(pl)} = \int_{t_0}^{t_2} i_{GG}(t) dt$$

3.3.6.4**gate drain charge**

charge difference between beginning and end of plateau region, required to charge up C_{GD} and calculated by the equation below (see Figure 1)

$$Q_{GD} = \int_{t_2}^{t_3} i_{GG}(t) dt$$

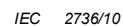


Figure 1 – Basic waveforms to specify the gate charges

ratio of the output power to the sum of the input signal power and the d.c. input power

ratio of the output power to the d.c. drain power

ratio of the difference between the output power and the input signal power to the d.c. input power

$$\eta_{\text{add}} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{d(d.c.)}}}$$

3.3.10**rate of rise of off-state voltage**

rate of rise of drain-source off-state voltage induced during reverse recovery period of the inverse diode

3.3.11**reverse-bias safe operating area**

drain current versus drain-source voltage region in which the MOSFET is able to turned-off repetitively with clamped inductive load without failure

3.3.12**short circuit safe operating area**

drain current versus drain voltage region in which the MOSFET is able to turn on and off non repetitively without failure

3.3.13**avalanche energy (for avalanche devices)**

avalanche energy capability during turn-off period

3.3.14**repetitive avalanche energy (for avalanche devices)**

repetitive avalanche energy capability during turn-off period

3.3.15**non-repetitive avalanche energy (for avalanche devices)**

non-repetitive avalanche capability during turn-off period (single pulse)

3.3.16**drain leakage current**

drain current in the off-state

3.3.17**breakdown voltage, drain to source**

drain-source breakdown voltage in the off-state

3.3.18**internal gate resistance**

short-circuit internal gate resistance (see Figure 32)

3.3.19**switching times**

input wave form is the gate to source voltage, and output waveform is the drain current (see IEC 60747-1:2006)

3.3.20**turn-on energy**

value of the integral of the product of drain-source voltage V_{DS} and drain current I_{D} during turn-on described in the following equation: $E_{\text{on}} = \int_0^{t_1} i_{\text{D}} \times v_{\text{DS}} \times dt$ (see Figure 2)