

Discrete semiconductor devices —

Part 8-4: Metal-oxide-semiconductor field-effect transistors (MOSFETs) for power switching applications)

ICS 31.080.30

National foreword

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Summary of pages

This document comprises a front cover, an inside front cover, the IEC title page, pages 2 to 61 and a back cover.

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Amendments issued since publication

Amd. No.	Date	Comments

This British Standard was published under the authority of the Standards Policy and Strategy Committee on 9 November 2004

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**NORME
INTERNATIONALE
INTERNATIONAL
STANDARD**

**CEI
IEC**

60747-8-4

Première édition
First edition
2004-09

Dispositifs discrets à semiconducteurs –

Partie 8-4:

**Transistors à semiconducteurs à oxyde métallique
à effet de champ (MOSFET) pour les applications
de commutation de puissance**

Discrete semiconductor devices –

Part 8-4:

**Metal-oxide-semiconductor field-effect
transistors (MOSFETs) for power
switching applications**



Numéro de référence
Reference number
CEI/IEC 60747-8-4:2004

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

DISCRETE SEMICONDUCTOR DEVICES –

**Part 8-4: Metal-oxide-semiconductor field-effect transistors (MOSFETs)
for power switching applications**

FOREWORD

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International Standard IEC 60747-8-4 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47E/259/FDIS	47E/266/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

This standard is to be read in conjunction with IEC 60747-1 where the user will find all basic information on

- terminology (Chapter II);
- letter symbols (Chapter II);
- essential ratings and characteristics (Chapter III);
- measuring methods (including verification of ratings) (Chapter IV);
- acceptance and reliability (Chapter V).

IEC 60747 consists of the following parts, under the general title *Discrete semiconductor devices*:

Part 1: General

Part 2: Rectifier diodes

Part 3: Signal (including switching) and regulator diodes

Part 4: Microwave devices

Part 5: Optoelectronic devices

Part 6: Thyristors

Part 7: Bipolar transistors

Part 8: Field-effect transistors

Part 9: Insulated-gate bipolar transistors (IGBTs)

Part 10: Generic specification for discrete devices and integrated circuits

Part 11: Sectional specification for discrete devices

Part 12: Sectional specification for optoelectronic devices

Part 13: —

Part 14: Semiconductor sensors

Part 15: Isolated power semiconductor devices

Part 16: Microwave integrated devices.

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- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

DISCRETE SEMICONDUCTOR DEVICES –

Part 8-4: Metal-oxide-semiconductor field-effect transistors (MOSFETs) for power switching applications

1 Scope

This part of IEC 60747 gives details for the following categories of metal-oxide semiconductor field-effect transistors (MOSFETs) with inverse diodes.

- Type B depletion (normally on) type.
- Type C enhancement (normally off) type.

NOTE 1 MOSFETs for some applications may not have inverse diode characteristics in the data sheet. Special circuit element structures to eliminate body diode are under development for such applications. MOSFET applications such as motor control equipment need to specify the inverse diode characteristics in the MOSFET to use the inverse diode as a free wheeling diode.

NOTE 2 MOSFET is classified as a kind of insulated gate field-effect transistor (IGFET) in IEC 60747-8.

NOTE 3 The graphical symbol only for type C is used in this standard. It equally applies for the measurement of type B devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60747-1:1983, *Semiconductor devices – Discrete devices and integrated circuits – Part 1: General*

IEC 60747-2:2000, *Semiconductor devices – Discrete devices and integrated circuits – Part 2: Rectifier diodes*

IEC 60747-8:2000, *Semiconductor devices – Part 8: Field-effect transistors.*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1 General terms

General terms for MOSFETs are defined in 4.2 of IEC 60747-8.

3.2 Equivalent circuit

MOSFETs generally (see NOTE 1 in Clause 1) contain an intrinsic inverse or body diode in parallel with the MOSFET itself. Figure 1 shows the equivalent circuit of an N-channel device. Polarities are reversed for P-channel devices. The diode is not shown in the normal graphical symbol.

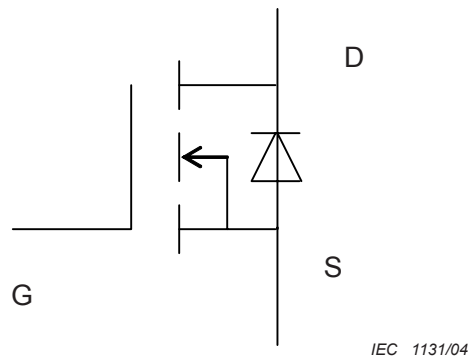


Figure 1 – Equivalent circuit of MOSFET with inverse diode

3.3 Terms related to ratings and characteristics

3.3.1

rate of rise of off-state voltage

dv/dt

rate of rise of drain-source off-state voltage induced during reverse recovery period of the inverse diode

3.3.2

reverse-bias safe operating area

RBSOA

drain current versus drain-source voltage region in which the MOSFET is able to turned-off repetitively with clamped inductive load without failure

3.3.3

short-circuit safe operating area

SCSOA

drain current versus drain voltage region in which the MOSFET is able to turn on and off non repetitively without failure

3.3.4

avalanche energy (for avalanche devices)

E_A

avalanche energy capability during turn-off period

3.3.5

repetitive avalanche energy (for avalanche devices)

E_{AR}

repetitive avalanche energy capability during turn-off period

3.3.6

non-repetitive avalanche energy (for avalanche devices)

E_{AS}

non-repetitive avalanche capability during turn-off period (single pulse)

3.3.7

drain leakage current

I_{DS}

drain current in the off-state

3.3.8**breakdown voltage, drain to source** $V_{(BR)DS}$

drain-source breakdown voltage in the off-state

3.3.9**(short-circuit) input capacitance** C_{iss}

see 4.3.6.1 in IEC 60747-8

3.3.10**(short-circuit) output capacitance** C_{oss}

see 4.3.6.2 in IEC 60747-8

3.3.11**(short-circuit) reverse transfer capacitance** C_{rss}

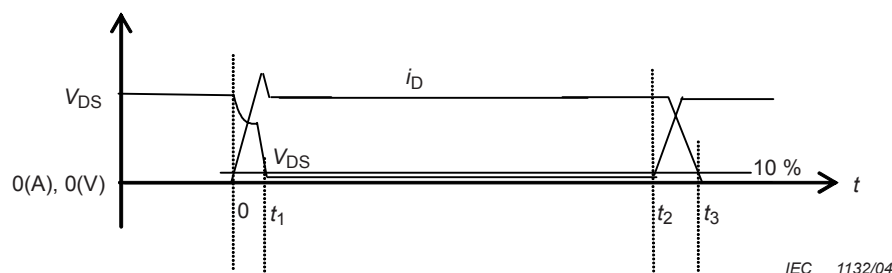
see 4.3.6.3 in IEC 60747-8

3.3.12**internal gate resistance** r_g

short-circuit internal gate resistance (see Figure 37)

3.3.13**switching times** $t_{d(on)}$, t_r , $t_{d(off)}$, and t_f

input waveform is the gate to source voltage, and output waveform is the drain current (see IEC 60747-1)

3.3.14**turn-on energy** E_{on} value of the integral of the product of drain-source voltage V_{DS} and drain current I_D during turn-on described as the equation of $E_{on} = \int_0^{t_1} I_D \times V_{DS} \times dt$ (see Figure 2)**3.3.15****turn-off energy** E_{off} value of the integral of drain-source voltage V_{DS} multiplied by drain current I_D during turn-off described as the equation of $E_{off} = \int_{t_2}^{t_3} I_D \times V_{DS} \times dt$ (see Figure 2)Figure 2 – Integral times for the turn-on energy E_{on} and turn-off energy E_{off}

3.3.16
gate charges

3.3.16.1
total gate charge

Q_G

charge that is required to raise the gate-source voltage from zero to a specified value and calculated by the following equation (see Figure 3)

$$Q_G = \int_{t_0}^{t_4} i_{GG}(t) dt$$

3.3.16.2
threshold gate charge

$Q_{GS(th)}$

charge required to raise gate-source from zero to $V_{GS(th)}$ and calculated by the following equation (see Figure 3)

$$Q_{GS(th)} = \int_{t_0}^{t_1} i_{GG}(t) dt$$

3.3.16.3
plateau gate charge

$Q_{GS(pl)}$

charge required to raise gate-source voltage from zero to plateau voltage $V_{GS(pl)}$ and calculated by the following equation (see Figure 3)

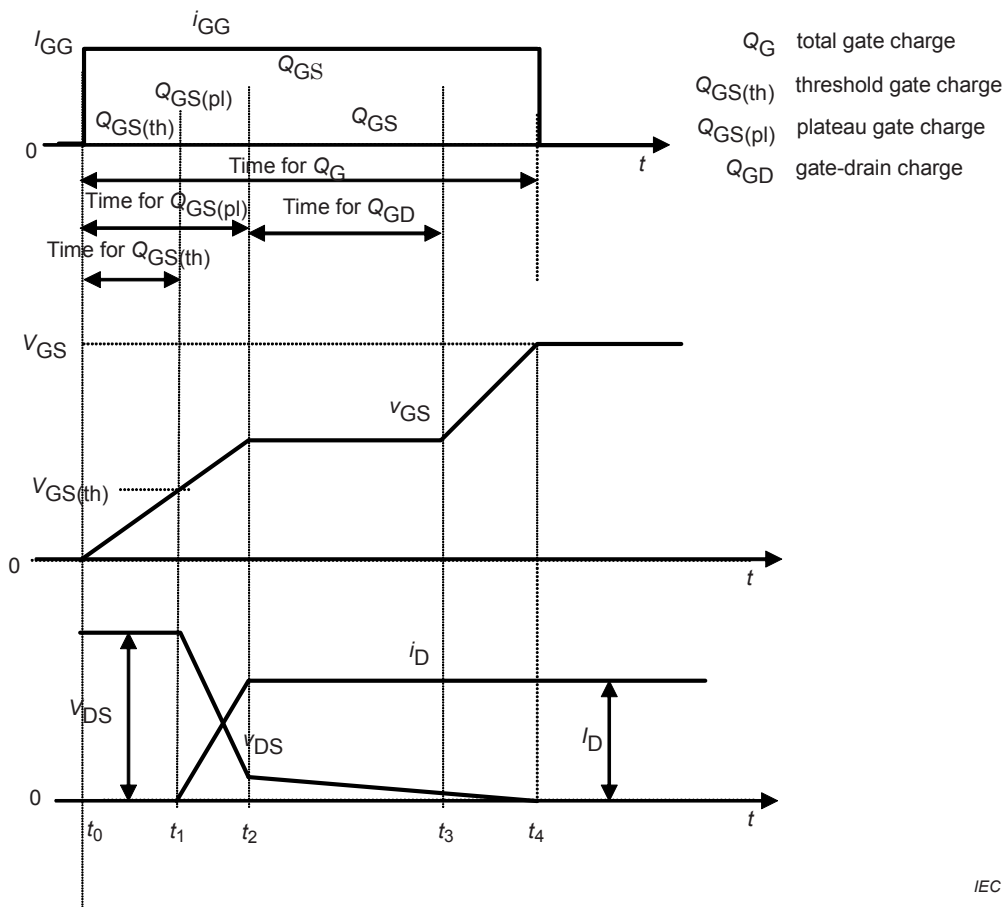
$$Q_{GS(pl)} = \int_{t_0}^{t_2} i_{GG}(t) dt$$

3.3.16.4
gate drain charge

Q_{GD}

charge difference between beginning and end of plateau region, required to charge up C_{GD} and calculated by the following equation (see Figure 3)

$$Q_{GD} = \int_{t_2}^{t_3} i_{GG}(t) dt$$



IEC 1133/04

NOTE Time intervals indicated by arrow end lines are integral intervals to calculate the gate charges.

Figure 3 – Basic waveforms to specify the gate charges

3.3.17

output capacitance charge

Q_{OSS}

charge required to change the voltage at output capacitance C_{OSS} during turn-on and turn-off

3.3.18

gate-source plateau voltage

$V_{GS(pl)}$

voltage during turn-on, where V_{GS} is relatively constant (Miller-Plateau) and during which C_{GD} is charged

NOTE See Figure 3.

3.3.19

drain-source reverse voltage

V_{DSR}

voltage across the MOSFET which results from the flow of current in the reverse direction

3.3.20

MOSFET forward recovery current

I_{FR}

recovery current of the MOSFET which results from the flow of current in the reverse direction

3.3.21**MOSFET forward recovery time** t_{fr}

recovery time of the MOSFET which results from the flow of current in the reverse direction

3.3.22**MOSFET forward recovery charge** Q_f

recovery charge of the MOSFET which results from the flow of current in the reverse direction

3.4 Conventional used terms**Table 1 – Terms for MOSFET in this standard and the conventional used terms for the inverse diode integrated in the MOSFET**

Standard terms	Letter symbol	Conventionally used terms for inverse diode with MOSFET in off-state	Letter symbol
Drain-source reverse voltage	V_{DSR}	Inverse diode forward voltage	V_F
MOSFET forward recovery current	I_{FR}	Inverse diode reverse recovery current	I_{RR}
MOSFET peak forward recovery current	I_{FRM}	Inverse diode peak reverse recovery current	I_{RM}
MOSFET forward recovery time	t_{fr}	Inverse diode reverse recovery time	t_{rr}
MOSFET forward recovered charge	Q_f	Inverse diode reverse recovered charge	Q_r
Reverse drain current	I_{DR}	Inverse diode forward current	I_F
Peak reverse drain current	I_{DRM}	Inverse diode peak forward current	I_{FM}

4 Letter symbols

General letter symbols for MOSFETs are defined in Clauses 2, 3 and 4, Chapter V of IEC 60747-1 and in 4.4.3 of IEC 60747-8. Special letter symbols related to inverse diodes are given in 4.3 of IEC 60747-2.

4.1 Additional general subscripts

In addition to the list of recommended general subscripts given in 2.2.1, Chapter V of IEC 60747-1, the following subscripts are newly introduced in this standard:

- O termination with a open circuit
- S termination with a short circuit
- R termination with a resistor
- X termination with specified gate source voltage
- pl plateau
- th threshold.

NOTE X is defined in 4.1.2 of IEC 60747-7.

4.2 List of additional letter symbols

Name and designation	Letter symbol	Remarks
4.2.1 Voltages		
Breakdown voltage, drain-source (for type B)	$V_{(BR)DSX}$	
Breakdown voltage, drain-source (for type C)	$V_{(BR)DSS}$	
Gate-source on-state voltage (for type C)	$V_{GS(on)}$	
Drain-source on-state voltage	$V_{DS(on)}$	
Drain-source reverse voltage	V_{DR}	
Gate-source plateau voltage	$V_{GS(pl)}$	
4.2.2 Currents		
Peak drain current	I_{DM}	
Reverse drain current	I_{DR}	
Peak reverse drain current	I_{DRM}	
4.2.3 Switching energy		
Turn-on energy	E_{on}	
Turn-off energy	E_{off}	
4.2.4 Avalanche energy (for avalanche types)		
Repetitive avalanche energy	E_{AR}	
Non-repetitive single pulse avalanche energy	E_{AS}	
4.2.5 Resistance		
Internal gate resistance	r_g	
4.2.6 Gate charges (see Figure 3)		
Total gate charge	Q_G	
Plateau gate charge	$Q_{GS(pl)}$	
Gate-drain charge	Q_{GD}	
Threshold gate charge	$Q_{GS(th)}$	
4.2.7 MOSFETs recoveries (inverse diode recoveries)		
Peak forward recovery current	I_{FRM}	
Forward recovery time	t_{fr}	
Forward recovered charge	Q_f	

5 Essential ratings and characteristics

5.1 General

For multiple-gate devices, required gate ratings and characteristics shall be given for each gate separately, except where otherwise stated.

5.2 Ratings (limiting values)

Ratings shall be valid for the whole range of operating conditions as stated for the particular device, with reference to a curve where appropriate.

5.2.1 Temperatures

5.2.1.1 Minimum and maximum ambient, case or virtual junction temperatures (T_a or T_C or T_{vj})

5.2.1.2 Where appropriate, minimum and maximum storage temperature (T_{stg})

5.2.2 Power dissipation (P_{tot})

Maximum total power dissipation, any special requirements for ventilation and/or mounting shall be stated, where appropriate, a de-rating curve versus temperature.

5.2.3 Voltages and currents

5.2.3.1 Maximum off-state drain current (I_{D0})

5.2.3.2 Maximum gate-source voltages ($\pm V_{GS}$)

5.2.3.3 Maximum gate-gate voltage (for multiple-gate devices) (V_{G1-G2})

5.2.3.4 Maximum rate of rise of off-state voltage (dv/dt)

5.2.3.5 Maximum on-state drain current (I_D)

5.2.3.6 Maximum peak on-state drain current (I_{DM})

Under specified pulse conditions.

5.2.3.7 Maximum reverse drain current (I_{DR})

5.2.3.8 Maximum peak reverse drain current (I_{DRM})

Under specified pulse conditions.

5.2.4 Safe operating area (SOA), where appropriate

5.2.4.1 Maximum RBSOA

Under specified pulse conditions.

5.2.4.2 Maximum SCSOA (if applicable)

Under specified short-circuit conditions. Alternatively the time for which the device can be turned-on non repetitively across a specified drain-source voltage and with specified gate conditions may be specified.

5.2.5 Avalanche energy (for avalanche devices)

5.2.5.1 Maximum repetitive avalanche energy (E_{AR})

Under specified conditions in an unclamped inductive switching circuit.

5.2.5.2 Maximum non-repetitive avalanche energy (E_{AS})

Under specified conditions in an unclamped inductive switching circuit.

5.2.6 Mechanical data

See IEC 60747-1.

5.3 Characteristics

Characteristics shall be given at 25 °C and at one specified higher operating temperature taken except where otherwise stated.

5.3.1 Gate leakage current (I_{GSS})

Maximum value at maximum gate-source voltage V_{GS} with drain shorted to source.

5.3.2 Drain leakage current (I_{DSX}) (for type B)

Maximum value at specified high drain-source voltage and gate-source voltage.

5.3.3 Drain leakage current (I_{DSS}) (for type C)

Maximum value at specified high drain-source voltage and gate-source shorted.

5.3.4 Breakdown voltage, drain to source ($V_{(BR)DSX}$) (for type B)

Minimum value, at maximum off-state drain current I_{D0} and specified gate-source voltage.

5.3.5 Breakdown voltage, drain to source ($V_{(BR)DSS}$) (for type C)

Minimum value, at maximum off-state drain current I_{D0} and gate-source shorted.

5.3.6 Gate-source cut-off voltage ($V_{GS(off)}$) (for type B)

Minimum and maximum values at specified high value of drain-source voltage and low value of drain current.

5.3.7 Gate-source threshold voltage ($V_{GS(th)}$) (for type C)

Minimum and maximum values, at specified high value of drain-source voltage and at a low value of drain current.

5.3.8 Gate-source on-state voltage ($V_{GSM(on)}$) (for type C)

Maximum value in the on-state.

5.3.9 Drain-source on-state resistance ($r_{DS(on)}$)

Maximum value at specified gate voltage, temperature and with negligible internal dissipation (see Figure 28).

5.3.10 Drain-source reverse voltage (V_{DR})

Maximum value at specified high reverse current (I_{DR}) and at $V_{GS} = 0$.

5.3.11 Short-circuit input capacitance (C_{iss})

Maximum value, under specified drain-source voltage, at specified frequency and with the drain source short-circuited to a.c.

5.3.12 Short-circuit output capacitance (C_{oss})

Maximum value, under specified drain-source voltage, at specified frequency and with gate source short-circuited to a.c.

5.3.13 Short-circuit reverse transfer capacitance (C_{rss})

Maximum value, under specified drain-source voltage, at specified frequency and with gate source short-circuited to a.c.

5.3.14 Internal gate resistance (r_g), where appropriate

Maximum and/or typical value, under the electrical conditions specified and at specified frequency

5.3.15 Switching times ($t_{d(on)}$, t_r , $t_{d(off)}$, and t_f)

Typical values under specified conditions:

- drain current;
- gate-source voltage for turn-on and off;
- load resistance;
- resistance in the gate-source circuit;
- case or ambient temperature or virtual junction temperature.

NOTE Where $t_{d(off)}$ is only a small fraction of the total turn-off time (t_{off}), a maximum value for t_{off} alone is adequate. The value of $t_{d(on)}$ is from 10 % of V_{GS} to 10 % of rising I_D . The value of t_r is from 10 % to 90 % of the rising I_D . The value of t_f is using the linear part of decline only to cover the (di/dt) of falling I_D (see IEC 60747-1).

5.3.16 Turn-on energy (per pulse) (E_{on}), where appropriate

Maximum value under specified conditions:

- drain-source voltage before turn-on;
- drain peak current after turn-on;
- gate-source voltage;
- resistance in the gate-source circuit;
- case or ambient temperature or virtual junction temperature.

5.3.17 Turn-off energy (per pulse) (E_{off}), where appropriate

Maximum value under specified conditions:

- drain peak current before turn-off;
- drain-source voltage after turn-off;
- gate-source voltage;
- resistance in the gate-source circuit;
- case or ambient temperature or virtual junction temperature.

5.3.18 Gate charges (Q_G , Q_{GD} , $Q_{GD(th)}$, $Q_{GS(pl)}$)

Typical values at specified drain current (I_D), drain-source voltage (V_{DS}) and gate current (I_{GG}) (see Figure 3).

5.3.19 Forward recovery time (t_{fr})

Maximum value under specified conditions.

5.3.20 Peak forward recovery current (I_{FRM})

Maximum value under specified conditions.

6 Measuring methods**6.1 General**

The polarities of the power supplies, shown in the circuits in this standard, are applicable to N-channel type devices. However, the circuits can be adapted for P-channel type devices by changing the polarities of the meters and the power supplies.

The general precautions listed in Clause 2, Section One of Chapter VII of IEC 60747-1 apply. In addition, special care should be taken to use low-ripple d.c. supplies and to decouple adequately all bias supply voltages at the frequency of measurement. For four-terminal devices, the fourth terminal should be connected as specified.

When handling these devices, the handling precautions given in Clause 1, Chapter IX, of IEC 60747-1 shall be observed. The entire circuit in the following subclauses should be placed inside an electrostatic screen.

6.2 Verification of ratings (limiting values)

Table 2 – Failure defining characteristics and failure criteria

Failure defining characteristics	Failure criteria
I_{GSS}	$I_{GSS} > USL$
I_{DS*}	$I_{DS*} > USL$
$V_{GS(th)}$ (or $V_{GS(off)}$)	$V_{GS(th)} > USL$ or $V_{GS(th)} < LSL$
$r_{DS(on)}$	$r_{DS(on)} > USL$
USL: upper specified limit LSL: lower specified limit	

6.2.1 Voltages and currents

6.2.1.1 Drain-source voltage (d.c.) (V_{DS^*})

NOTE * = O, R, S or X

6.2.1.1.1 Purpose

To verify the drain-source voltage (d.c.) V_{DS^*} under specified conditions.

6.2.1.1.2 Circuit diagram

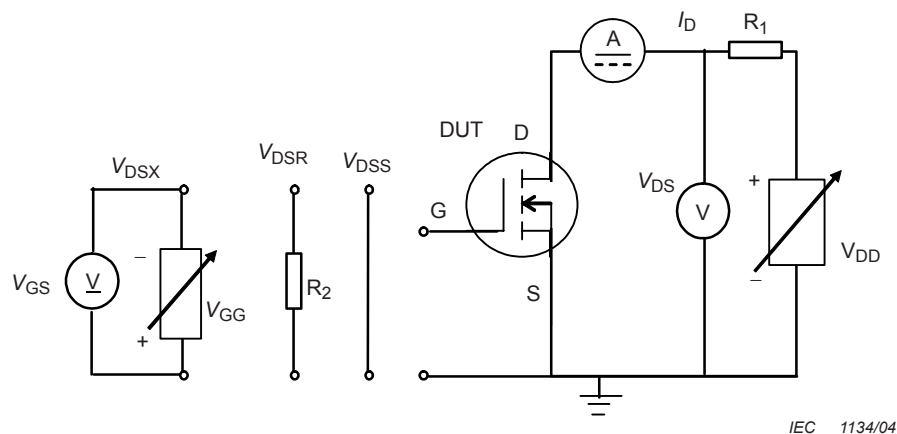


Figure 4 – Circuit diagram for testing of drain-source voltage

6.2.1.1.3 Circuit description and requirements

V_{DD} and V_{GG} are the d.c. voltage supply. R_1 is a circuit protection resistor.

6.2.1.1.4 Testing procedure

The gate-source is set to specified conditions. V_{DD} is increased until the drain-source voltage measured on voltmeter V_{DS} reaches the specified drain-source voltage (d.c.) V_{DS^*} . After the above test, confirm the failure-defining characteristics of DUT being normal by the criteria of Table 2.

6.2.1.1.5 Specified conditions

- Ambient or case or junction temperature (T_a or T_c or T_{vj})
- Gate-source bias conditions
- Drain-source voltage: rated drain-source voltage.

6.2.1.2 Gate-source (d.c.) voltage (V_{GS^*})

6.2.1.2.1 Purpose

To verify the gate-source (d.c.) voltage for both polarities, under specified conditions.