

Semiconductor devices — Integrated circuits

Part 2. Digital integrated circuits

ICS 31.200

National foreword

This British Standard reproduces verbatim IEC 60748-2 : 1997 and implements it as the UK national standard. It supersedes BS 6493-2-2 : 1986 which is withdrawn.

The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors, which has the responsibility to:

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- monitor related international and European developments and promulgate them in the UK.

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Summary of pages

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**Semiconductor devices –
Integrated circuits –**

**Part 2:
Digital integrated circuits**



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CONTENTS

Clause		Page
CHAPTER I: GENERAL		
1	Scope	11
2	Normative references.....	11
CHAPTER II: TERMINOLOGY AND LETTER SYMBOLS		
1	Terminology for combinatorial and sequential integrated circuits.....	12
1.1	General terms.....	12
1.2	Terms related to functions	12
1.3	Types of circuits	15
1.4	Terms related to ratings and characteristics	18
1.5	Latch-up concept.....	20
2	Examples	20
3	Terminology for integrated circuit memories	35
3.1	General terms.....	35
3.2	General terms relating to memory function and organization.....	36
3.3	Types of memories	37
3.4	Terms related to ratings and characteristics	39
3.5	Typical waveforms for static read/write memories	40
3.6	Terms and descriptions for test patterns for memory testing.....	45
4	Terminology for integrated circuit microprocessors.....	51
5	Terminology for charge-transfer devices	51
6	Letter symbols for combinatorial and sequential circuits	55
7	Letter symbols for the dynamic parameters of sequential integrated circuits, including memories	55
8	Additional terms and definitions for digital integrated circuits	68
9	Classification of programmable logic devices (PLDs).....	68
CHAPTER III: ESSENTIAL RATINGS AND CHARACTERISTICS		
SECTION ONE — DIGITAL INTEGRATED CIRCUITS, GENERAL		
1	Circuit identification and description	69
1.1	Designation and type	69
1.2	Technology.....	69
1.3	Package identification.....	69
2	Functional specifications	69
2.1	Block diagram.....	69
2.2	Functional description.....	70
2.3	Complex structures.....	70

3	Ratings (limiting values)	70
3.1	Continuous voltages and currents	71
3.2	Non-continuous voltages and currents	71
3.3	Temperatures	71
3.4	Capability of sustaining a short circuit	71
4	Recommended operating conditions (within the specified operating temperature range) ..	71
5	Static electrical characteristics for bipolar integrated circuits	72
5.1	Essential characteristics of the digital voltage signals	72
5.2	Input clamping voltage (where appropriate)	73
5.3	Essential characteristics for input and output currents	73
5.4	Applied conditions for worst case	76
5.5	Latch-up characteristics	76
6	Static and quasi-static electrical characteristics for MOS integrated circuits	77
6.1	Essential characteristics of the digital voltage signals	77
6.2	Essential characteristics for currents	77
6.3	Latch-up characteristics	78
7	Dynamic electrical characteristics	78
7.1	Introduction	79
7.2	Times characterizing the response of the circuit	79
7.3	Requirements at the inputs to ensure correct sequential operation	80
7.4	Input and output impedances	81
8	Total power or currents provided from the supplies	83
9	Total current drawn from the power supplies (dynamic operation)	83
10	Command pulse information (where appropriate)	84
11	Insulation resistance	84
12	Mechanical ratings, characteristics and other data	84
13	Supplementary information	84
13.1	Output loading capability	84
13.2	Noise margins	84
13.3	Interconnections of digital integrated circuits	84
14	Handling precautions	84

APPENDIX TO SECTION ONE — Specification of characteristics

SECTION TWO — INTEGRATED CIRCUIT MEMORIES

A. Static and dynamic read/write memories and read-only memories

1	Circuit identification and description	86
2	Functional specifications	86
2.1	Block diagram	86
2.2	Functional description	86
3	Ratings (limiting values)	86
4	Recommended operating conditions (within the specified operating temperature range)	87
5	Static electrical characteristics for bipolar memories	87
6	Static electrical characteristics for MOS memories	87

7	Dynamic electrical characteristics	87
7.1	Times characterizing the response of the circuit.....	87
7.2	Requirements at the inputs to ensure correct sequential operation	88
7.3	Input and output capacitances	92
8	Power or current drawn from each supply (static operation).....	93
9	Power or current drawn from each supply (dynamic operation)	93
10	Mechanical ratings, characteristics and other data	93
11	Supplementary information	93
11.1	Output loading capability.....	93
11.2	Noise margins	93
11.3	Interconnections of similar units.....	93
11.4	Type of output circuit	93
11.5	Interconnections to other types of circuits	93
12	Handling precautions	93

B. Field-programmable read-only memories

1	Circuit identification and description	94
2	Functional specifications.....	94
2.1	Block diagram.....	94
2.2	Identification of terminals.....	94
2.3	Functional description.....	95
3	Ratings (limiting values).....	95
4	Read mode.....	95
4.1	Recommended operating conditions (within the specified operating temperature range)	95
4.2	Static electrical characteristics.....	95
4.3	Dynamic electrical characteristics	96
4.4	Timing requirements	96
5	Programming mode	96
5.1	Programming procedure	96
5.2	Recommended programming conditions.....	96
5.3	Timing requirements	97
6	Erasing mode (if applicable).....	97
6.1	Electrically erasable memories.....	97
6.2	Ultraviolet erasable memories.....	98
7	Number of programming-erasing cycles	98
8	Data retention information.....	99
9	Power or current drawn from each supply (static operation).....	99
10	Power or current drawn from each supply (dynamic operation)	99
11	Mechanical ratings, characteristics and other data	99
12	Supplementary information	99
12.1	Output loading capability.....	99
12.2	Electrical noise margins.....	99
12.3	Interconnections of similar units.....	99
12.4	Type of output circuit	100
12.5	Interconnections to other types of circuits	100
13	Handling precautions	100

C. Content addressable memories (CAM)

1	Circuit identification and description	101
2	Functional specifications	101
2.1	Block diagram	101
2.2	Functional description	101
2.3	Instruction set	101
2.4	Operation mode	102
3	The provisions of clauses 3 to 6 of Section Two A apply	102
4	The provisions of clauses 7 and 7.1 of Section Two A apply with the exception of 7.1.1 which is replaced by the following	102
5	The provisions of 7.2 and 7.3 of Section Two A apply	102
6	The provisions of clauses 8 to 12 of Section Two A apply	102

SECTION THREE — INTEGRATED CIRCUIT MICROPROCESSORS

1	Circuit identification and description	103
1.4	Electrical compatibility	103
2	Functional specifications	103
2.1	Block diagram	103
2.2	Functional description	103
2.3	Instruction set	104
2.4	Configuration of instructions	104
2.5	Input and output signals	104
3	Ratings (limiting values)	105
3.1	Electrical limiting values	105
3.2	Temperatures	106
3.3	Power dissipation	106
4	Recommended operating conditions (within the specified operating temperature range) ..	106
4.1	Power supply voltage(s)	106
4.2	Clock inputs	106
4.3	Input voltages (excluding clock inputs)	106
4.4	Output currents	106
4.5	External elements (where appropriate)	106
4.6	Set-up and hold times	106
4.7	Timing diagrams for control sequences	107
5	Electrical characteristics	107
5.1	Static characteristics	107
5.2	Dynamic characteristics	108
6	Mechanical ratings, characteristics and other data	109
7	Supplementary information	109
7.1	Output loading capability	109
7.2	Noise margins	109
7.3	Application data	109
7.4	Other information	110
8	Handling precautions	110

SECTION FOUR — PROGRAMMABLE LOGIC DEVICES (PLDs)

1	Circuit identification and types.....	111
1.1	Designation of types	111
1.2	General function description	111
1.3	Manufacturing technology	111
1.4	Package identification.....	111
2	Application related description	111
2.1	Main application and features	111
2.2	Overall block diagram	111
2.3	Main features available by programming	111
2.4	Reference data	112
2.5	Electrical compatibility	112
2.6	Associated devices	112
3	Specification of the function	112
3.1	Detailed block diagram - functional blocks	112
3.2	Identification and function of terminals	112
3.3	Functional description.....	113
3.4	Family related characteristics.....	114
4	Limiting values (absolute maximum rating system)	114
4.1	Electrical limiting values.....	114
4.2	Temperatures	115
5	Recommended operating conditions (within the specified operating temperature range) ..	115
5.1	Power supplies – positive and/or negative values	115
5.2	Initialization sequences.....	115
5.3	Clock input(s) (where appropriate)	115
5.4	Input voltage(s).....	115
5.5	Output current(s)	116
5.6	Voltage and/or current of other terminal(s)	116
5.7	External elements (where appropriate).....	116
5.8	Operating temperature range	116
5.9	Timing requirements	116
6	Electrical characteristics	116
6.1	Static characteristics	116
6.2	Dynamic characteristics	117
6.3	Timing diagram.....	118
6.4	Capacitances.....	118
7	Programming	119
7.1	Programming mode	119
7.2	Erasing mode (if applicable).....	120
7.3	Number of programming-erasing cycles (where appropriate)	121
7.4	Data retention information.....	121
8	Design aspects	121
8.1	Computer aided engineering (CAE) design hardware.....	121
8.2	CAE design software	121

9	Mechanical and environment rating, characteristics and data.....	121
10	Additional information	121
10.1	Equivalent input and output circuit	121
10.2	Internal protection	122
10.3	Thermal resistance.....	122
10.4	Noise margin.....	122
10.5	Output loading capability	122
10.6	Interconnections of digital circuits.....	122
10.7	Interconnections to other types of circuit.....	122
10.8	Effects of externally connected component(s).....	122
10.9	Recommendations for any associated device(s).....	122
10.10	Handling precautions.....	122
10.11	Application data.....	122
10.12	Other application information.....	122
10.13	Date of issue of data sheet.....	122

CHAPTER IV: MEASURING METHODS

SECTION ONE — GENERAL

1	Basic requirements	123
2	Specific requirements	123
2.1	General requirements for static and dynamic measurements.....	123
2.2	Specified conditions for static characteristics	123
2.3	Specified conditions for dynamic characteristics.....	124
3	Application matrix for the measuring methods	124

SECTION TWO — MEASURING METHODS OF STATIC CHARACTERISTICS

1	High-level and low-level output voltages (V_{OH} and V_{OL}) [37]	126
2	High-level and low-level input currents (I_{IH} and I_{IL}) [38].....	127
3	Short-circuit output current (I_{OS}) [40].....	128
4	Power supply current under static conditions [41].....	129
5	(Input) threshold voltages and hysteresis voltage [48].....	129
6	Input clamping voltage (V_{IK}) [94]	132
7	Off-state output current (I_{OZ}) [95].....	133
8	Latch-up characteristics [96].....	133
8.1	Positive latch-up input or output voltage or current	133
8.2	Negative latch-up input or output voltage or current.....	136
8.3	Latch-up supply voltage or current	138
8.4	Latch-up state (supply) voltage or current	141
8.5	Precautions	142
8.6	Post-test measurement.....	142

SECTION THREE — DYNAMIC MEASUREMENTS

1	Total current drawn from the power supplies under dynamic conditions [1]	143
2	Power supplied through the clock line [2]	144
3	Input and output impedances [6], [11]	145
3.1	Current measurement: input and output capacitances for large-signal operation [6]	145
3.2	Voltage measurement: equivalent input and output capacitances, equivalent input and output resistances [11]	147
4	Times characterizing the circuit	152
4.1	Propagation times [3], [7]	152
4.2	Delay and transition times [4], [5]	155
4.3	Set-up time [8] and hold time [9]	158
4.4	Resolution time [36]	161
4.5	Output enable and disable times (for three-state outputs) [49]	163
4.6	Specific times for memories [50] to [54]	165
5	Switching frequency of a sequential circuit [10]	169
6	Method of verification of the function of a digital integrated circuit [97]	171

CHAPTER V: ACCEPTANCE AND RELIABILITY

SECTION ONE — ELECTRICAL ENDURANCE TESTS

1	General requirements	173
2	Specific requirements	173
2.1	List of endurance tests	173
2.2	Conditions for the endurance tests	173
2.3	Failure criteria for the failure-defining characteristics for acceptance tests	173
2.4	Failure criteria and failure-defining characteristics for reliability tests	173
2.5	Procedure in case of a testing error	173
TABLE 7		174

INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –

Part 2: Digital integrated circuits

FOREWORD

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International Standard IEC 60748-2 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

This second edition cancels and replaces the first edition published in 1985, amendment 1 (1991) and amendment 2 (1993).

The text of this standard is a compilation of the first edition, its amendments 1 and 2 and the following documents:

FDIS	Report on voting
47A/502/FDIS	47A/506/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This standard shall be used in conjunction with IEC 60747-1 and IEC 60748-1. In these publications, the user will find all basic information on terminology, letter symbols, essential ratings and characteristics, measuring methods, acceptance and reliability.

Although not conform to Part 3 of ISO/IEC Directives, the numbering of the clauses of this standard remains the same as that of the first edition. The next technical revision will conform to Part 3 of the Directives.

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –

Part 2: Digital integrated circuits

CHAPTER I: GENERAL

1 Scope

This part of IEC 60748 is applicable for the following categories or subcategories of devices:

- combinatorial and sequential digital circuits;
- integrated circuit memories;
- integrated circuit microprocessors;
- charge-transfer devices.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this International Standard. At the time of publication, the editions indicated were valid. All normative documents are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 60747-1: 1983, *Semiconductor devices – Discrete devices – Part 1: General*

IEC 60748-1: 1984, *Semiconductor devices – Integrated circuits – Part 1: General*

IEC 60748-3: 1986, *Semiconductor devices – Integrated circuits – Part 3: Analogue integrated circuits*

IEC 60748-4: 1987, *Semiconductor devices – Integrated circuits – Part 4: Interface integrated circuits*

CHAPTER II: TERMINOLOGY AND LETTER SYMBOLS

1 Terminology for combinatorial and sequential integrated circuits

1.1 General terms

NOTE – A signal is a physical representation of information. A digital signal is the time-dependent behaviour or variation of a physical quantity with a finite number of non-overlapping ranges of values. A digital signal can be used for transmission of information or for information processing. Taking into account common practice, simplified definitions have been chosen below. Referring to digital circuits, this will generally produce no ambiguity or misunderstanding.

1.1.1 Digital signal

The variation with time of a physical quantity, having a finite number of non-overlapping ranges of values, that is used for transmission or the processing of information.

NOTE 1 – The physical quantity may include voltage, current, impedance, etc.

NOTE 2 – For convenience, each range of values can be represented by a single value, e.g. the nominal value.

1.1.2 Binary signal

A digital signal with only two possible ranges of values.

1.1.3 Low range (of a binary signal)

The range of least positive (most negative) levels of a binary signal.

NOTE – This range is often denoted by "L-range" and any level in the range by "L-level".

1.1.4 High range (of a binary signal)

The range of most positive (least negative) levels of a binary signal.

NOTE – This range is often denoted by "H-range" and any level in the range by "H-level".

1.1.5 Input terminal

A terminal by means of which an applied signal may modify the output configuration (output pattern) of the circuit:

- either directly;
- or indirectly by modifying the ways in which the circuit reacts to signals at other terminals.

1.1.6 Three-state output

An output of a binary circuit that is a relatively low-impedance source or sink at the high and low levels and, in addition, under appropriate input conditions, provides a high-impedance state approaching an open-circuit.

NOTE – In function tables and function (sequential) matrices, the abbreviation Z should be used for the high-impedance state.

1.2 Terms related to functions

1.2.1 Input configuration (input pattern) (of a binary circuit)

A combination of the L-levels and H-levels at the input terminals at a given instant.

1.2.2 Output configuration (output pattern) (of a binary circuit)

A combination of the L-levels and H-levels at the output terminals at a given instant.

NOTE – When there is no possibility of ambiguity, the output configuration (output pattern) may be represented by the level (expressed as L-level and H-level) of the signal at a stated terminal of the circuit (the reference output terminal).

1.2.3 Function table

A representation of the necessary or possible relations between the values of the digital signals at the inputs and the outputs of a digital circuit, these values of the digital signals being indicated either by using electrical values directly or by stating the electrical significance of the symbols (e.g. L and H for binary circuits).

Generally:

- every column indicates the values of the digital signals at an input or at an output of the digital circuit;
- every line indicates the combination of values of the digital signals at the input(s) and the resulting values of the digital signals at the output(s);
- whenever the value of the digital signal at an output is not determined, it should be indicated by a question mark;
- whenever the value of a digital signal at an input has no influence, it should be indicated by the symbol L/H or X.

1.2.4 Truth table (for a relation between digital variables)

A representation of the logic relationship between one or more independent digital variables and one or more dependent digital variables, by means of a table which, for each possible combination of the values of the independent variables, gives the appropriate values of the dependent variables:

NOTE – The distinction between "function table" and "truth table" is fundamentally necessary, because the same digital circuit may fulfil several different logic operations, according to the arbitrary choice of the assignment of the values of the digital variables to the values of the digital electrical quantities.

1.2.5 Excitation

An input configuration (input pattern), or change in input configuration (input pattern), that can:

- cause the circuit to change its output configuration (output pattern), either directly, or in conjunction with an already existing state of preparedness;
- or put the circuit in a state of preparedness;
- or either cancel or modify an already existing state of preparedness.

NOTE 1 – The repetition, or reiteration, of a given excitation will not necessarily produce the same effect.

NOTE 2 – In some cases, an excitation can also maintain an output configuration (output pattern) which it could have produced.

1.2.6 Active level (of a digital signal to a sequential circuit)

A level of a digital input signal which can produce excitation.

1.2.7 Active transition (of a digital signal to a sequential circuit)

A transition from one level of a digital input signal to another level, which can produce excitation.

NOTE – An active transition may also be subject to limitations arising from the slope of the signal.

1.2.8 Stable output configuration (output pattern) (of a sequential circuit)

An output configuration (output pattern), in which the circuit will remain after the excitation that produced it, or any other that could have maintained it, has been replaced by an input configuration (input pattern) which is not an excitation,

or:

an output configuration (output pattern) which the circuit takes up in the absence of excitation.

NOTE – Any short persistence of the output configuration (output pattern) due to undesired effects such as capacitance, storage and propagation times, etc., is ignored.

1.2.9 Pseudo-stable output configuration (output pattern) (of a sequential circuit)

An output configuration (output pattern) which does not persist after the excitation that produced it, or other excitations that have maintained it, have been replaced by an input configuration (input pattern) which is not an excitation.

NOTE – Any short persistence of the output configuration (output pattern) due to undesired effects such as capacitance, storage and propagation times, etc., is ignored.

1.2.10 Meta-stable output configuration (output pattern) (of a sequential circuit)

An output configuration (output pattern) which persists, for a limited duration only, after the appropriate excitation has been applied.

NOTE 1 – The duration of the meta-stable output configuration (output pattern) will depend on the design of the circuit, may depend on the duration of the excitation that produced it and may be affected by further excitation.

NOTE 2 – Any short persistence of the output configuration (output pattern) due to undesired effects such as capacitance, storage and propagation times, etc., is ignored.

1.2.11 Function (sequential) matrix

A table having several inputs which gives the possible output configurations for each input configuration(s) and from which the output configuration(s) resulting from a transition from each individual input configuration to any other input configuration can be read directly.

NOTE – Where appropriate, a function (sequential) matrix may be completed by additional data or details concerning time conditions (e.g. transition times for the input levels, delay time, duration of the input configuration to produce a desired new output configuration).

1.2.12 Preparatory input terminal

An input terminal through which an applied digital signal can modify the manner in which the circuit reacts to signals at other input terminals, without directly causing a change of the output configuration (output pattern) of the circuit.

1.2.13 Enable input

An input that when active permits one or more specific operations to be commenced.

NOTE 1 – An "enable" signal may either:

- a) permit one or more operations to be performed while the signal is maintained at a specified level, or
- b) operate a latch that will allow an operation to continue even after the "enable" signal has been removed.

NOTE 2 – "Enable" is a generic term. It may be qualified by suitable descriptive adjectives as required.

1.2.14 Chip-enable input

An enable input that when inactive causes the integrated circuit to be in a reduced-power stand-by mode.

1.2.15 Chip-select input

An enable input that when inactive prevents both input and output of data to and from the integrated circuit.

1.2.16 Output enable input

An enable input that when inactive prevents the output of data from the integrated circuit.

NOTE – When not enabled, the outputs will assume a low level, a high level, or a floating (high-impedance) state, depending on the design of the particular circuit.

1.2.17 Write-enable input

An input that, when active, permits data to be entered into a memory for storage.

1.2.18 Disable input; inhibit input

An input that when active prevents one or more specific operations from being performed.

NOTE 1 – These are alternative names for an enable input emphasizing the complementary or negative aspect.

NOTE 2 – When inactive, an enable input disables or prevents the operations that it would permit if active. Conversely, when inactive, a disable input permits the operation(s) to be performed that it would prevent if active.

1.2.19 Level-operated input

An input that continues to be active (to cause excitation) as long as it remains at an active level.

1.2.20 Transition-operated input

An input that is active (causes excitation) only on one of the two directions of transition or an input that causes excitation only if the rate of change from one level to another is sufficiently large.

1.2.21 Set

- 1) (ISO) To cause a counter to take the state corresponding to a specified number.
- 2) (ISO) To place a storage device into a specified state, usually other than that denoting zero.

NOTE – Contrast with "reset".

1.2.22 Resets

- 1) (ISO) To cause a counter to take the state corresponding to a specified initial number.
- 2) (ISO) To restore a storage device to a prescribed initial state, not necessarily that denoting zero.

NOTE – Contrast with "set".

1.3 Types of circuits**1.3.1 Digital circuit**

A circuit which is designed to operate by means of digital signals at the input(s) and at the output(s).

NOTE 1 – In this definition, it is understood that "inputs" and "outputs" exclude static power supplies.

NOTE 2 – In some digital circuits, e.g. certain types of astable circuits, the input(s) need not exist.

1.3.2 Binary circuit

A digital circuit designed to operate with binary signals.

NOTE – The pairs of ranges of values of the binary signals may be different at different terminals.

1.3.3 Combinational (digital) circuit

A digital circuit in which there exists one, and only one, combination of the digital signals at the outputs for each possible combination of digital signals at the inputs.

1.3.4 Sequential (digital) circuit

A digital circuit in which there exists at least one combination of the digital signals at the inputs for which there is more than one corresponding combination of the digital signals at the outputs.

NOTE – These combinations at the outputs are determined by previous history (as a result of internal memory, delay, etc.)

1.3.5 Elementary combinational circuit

A binary combinational (digital) circuit which has only one output terminal; and in which the output signal accepts the value occurring only once in the function if, and only if, the signals applied to all the input terminals are either all in the H-range or all in the L-range.

NOTE 1 – Because the output signal value (occurring only once in the function table) can lie either in the H-range or in the L-range, there are four types of elementary combinational circuits. According to the assignment of the signal values L and H to the binary values 0 and 1 of Boolean algebra, the following logic operations can be realized by means of the four types of elementary combinational circuits: AND, OR, NAND, NOR.

NOTE 2 – Non-elementary combinational circuits can be formed by combining elementary combinational circuits or by combining elementary combinational circuits with inverters.

1.3.6 Bistable circuit

A sequential circuit which has two, and only two, stable output configurations (output patterns).

NOTE 1 – This broad classification can be divided into sub-classes according to the numbers and kinds of pseudo-stable and meta-stable output configurations (output patterns) available and the number of applications of appropriate excitations required to change from one stable output configuration (output pattern) to the other.

NOTE 2 – A stable output configuration (output pattern) of a bistable circuit can be expressed by the L-level or the H-level of the reference output terminal.

NOTE 3 – The term "bistable circuit" is used as a generic term to cover the whole range of sequential circuits with two, and only two, stable output configurations. It may be used itself for any kind or class of bistable circuits, when such use does not result in ambiguity or misunderstanding. In particular, the abbreviated term "bistable circuit" is often used for the single excitation bistable circuits.

1.3.6.1 Edge-triggered (transition-operated) bistable circuit

A bistable circuit having one or more transition-operated inputs.

1.3.6.2 Pulse-triggered bistable circuit

A bistable circuit requiring that a signal at a preparatory input be set up with respect to a first transition of a signal at a triggering input and be held with respect to a second transition occurring at the same triggering input and possibly causing the outputs to change state.

NOTE – This definition does not preclude the possibilities that minimum set-up and/or hold times may be negative.

1.3.6.3 Data-lock-out bistable circuit

A bistable circuit requiring that the signals at the preparatory inputs be set up and held with respect to that transition of the triggering-input signal that does not cause the outputs to change state.

1.3.7 Monostable circuit

A sequential circuit which has only one stable output configuration (output pattern).

NOTE 1 – The definition above is given in its most general form. In present usage, the term "monostable circuit" implies that there is at least one meta-stable output configuration (output pattern) in addition to the stable output configuration (output pattern).

NOTE 2 – In general, such circuits may have one or more meta-stable and/or pseudo-stable output configurations (output patterns).

1.3.8 Expander circuit

An auxiliary circuit which can be used to expand the number of inputs of equal influence of an associated circuit without modifying the function of the associated circuit.

1.3.9 Binary inverter

Binary circuit which has only one input terminal and one output terminal, and in which a signal value L (H) at the input produces a signal value H (L) at the output.

1.3.10 Master-slave arrangement

An arrangement of two bistable circuits such that one of them, called the "slave", reproduces the output configuration of the other circuit, called the "master". The transfer of information from the master to the slave is produced by means of an appropriate signal.

1.3.11 Register

An arrangement of bistable circuits by means of which information may be accepted, stored, and retrieved.

NOTE – The register may form part of another memory and is of a specified capacity.

1.3.12 Shift register

A register that, by means of an appropriate control signal, can transfer information between consecutive bistable circuits with the sequence being preserved.

1.3.13 Counter

A sequential circuit for storing numbers that permits such numbers to be incremented or decremented by a defined constant, including unity.

1.3.14 Digital decoder (integrated circuit)

An arrangement of logic elements (or the equivalent) that selects one or more output channels according to the combination of input signals present.

1.3.15 Programmable logic device (PLD)

An integrated circuit that consists of logic elements with an interconnection pattern parts of which are user programmable.

1.3.16 Programmable logic array (PLA)

A programmable logic device in which the logic elements consist mainly of arrays of AND gates and arrays of OR gates.

1.3.17 Programmable gate array (PGA)

A programmable logic device in which the logic elements include switches and memory elements that behave as groups of gates.

1.4 Terms related to ratings and characteristics

1.4.1 (Input) threshold voltage

The input voltage level that, when crossed, enables an output to change its logic state.

NOTE – The term hysteresis, often used in data sheets, denotes the difference between the positive-going and negative-going threshold voltages.

$$V_{\text{hys}} = V_{\text{IT+}} - V_{\text{IT-}}$$

or: $V_{\text{hys}} = V_{\text{ITP}} - V_{\text{ITN}}$

1.4.1.1 Positive-going (input) threshold voltage $V_{\text{IT+}}$, V_{ITP}

The input threshold voltage when the input voltage is rising.

NOTE – See note to 1.4.1.

1.4.1.2 Negative-going (input) threshold voltage $V_{\text{IT-}}$, V_{ITN}

The input threshold voltage when the input voltage is falling.

NOTE – See note to 1.4.1.

1.4.2 Input loading factor (of a binary digital circuit)

A factor which indicates the ratio of the input current of a specified input terminal of a digital circuit to the input current of a particular circuit which is chosen as a reference load.

NOTE – The reference load should preferably be chosen in such a way that the input loading factor becomes an integer.

1.4.3 Output loading capability (of a binary digital circuit)

A factor which indicates the ratio of the maximum output current of a specified output terminal of a digital circuit to the input current of a particular circuit which is chosen as a reference load.

NOTE – The reference load should preferably be chosen in such a way that the output loading capability becomes an integer.

1.4.4 Set-up time

The time interval between application of a signal that is maintained at a specific input terminal and a specified subsequent active transition at another input terminal.

NOTE 1 – The set-up time is measured between the instants at which the magnitudes of the two signals pass through specified values within the transition of the signal levels.

NOTE 2 – The set-up time is the actual time between two signals and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

NOTE 3 – The set-up time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which interval correct operation of the digital circuit is guaranteed.

1.4.5 Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTE 1 – The hold time is measured between the instants at which the magnitudes of the two signals pass through specified values within the transition of the signal levels.

NOTE 2 – The hold time is the actual time between two signals and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

NOTE 3 – The hold time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which interval correct operation of the digital circuit is guaranteed.

1.4.6 Resolution time

The time interval between the cessation of one input pulse and the commencement of the next input pulse applied to the same input terminal.

NOTE 1 – The resolution time is measured between the instants at which the magnitude of the input signal passes through specified values within the transition of the signal levels.

NOTE 2 – The resolution time is the actual time between two pulses and may be insufficient to ensure that both pulses are recognized. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

1.4.7 High-level to low-level (low-level to high-level) propagation time

The time interval between specified reference points on the input and on the output pulses, when the output is going to the low-(high-)level and when the device is driven and loaded by typical devices of stated types.

NOTE 1 – In some circumstances, the driving and the loading circuits may be replaced for test purposes by equivalent networks which must be specified.

NOTE 2 – The mean value between the upper limit of the input low range and the lower limit of the input high range is generally used as the specified reference level.

1.4.8 High-level to low-level (low-level to high-level) transition time

The time interval between specified reference points on the edge of the output pulse when the output is going to the low-(high-)level and when a specified input signal is applied through a specified network and the output is loaded by another specified network.

1.4.9 Enable time

The time interval from a specified point on the transition of the enabling signal to a specified point on an output waveform that represents the commencement of the intended operation.

1.4.10 Disable time

The time interval from a specified point on the transition of the disabling signal to a specified point on an output waveform that represents the cessation of the affected operation.

1.4.11 Output enable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

1.4.12 Output disable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

1.4.13 Pulse duration (width)

The time interval between the specified reference points on the two transitions of the pulse waveform.

1.4.14 Valid time

The time interval during which an output signal is valid or during which an input signal must be valid.

1.4.15 Output data-valid time

The time interval during which output data continues to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

1.4.16 Equivalent input (output) capacitance (of a binary circuit)

The capacitance of a discrete capacitor that causes the same effect on the waveform of a digital signal as the capacitive component of the input (output) impedance of a binary circuit.

1.5 Latch-up concept**1.5.1 Latch-up state**

A state in which a low-impedance path has resulted from and persists following the current resulting from an input, output or supply overvoltage that triggers a parasitic four-layer bipolar structure.

NOTE – In the latch-up state, the device becomes inoperable.

1.5.2 Latch-up effect

A process that results in a latch-up state.

1.5.3 Latch-up on-state voltage ($V_{CC(L)}$, $V_{DD(L)}$)

The voltage between the supply voltage terminals of an integrated circuit at a specified current when the integrated circuit is in the latch-up state.

1.5.4 Latch-up current (I_{latch})

The lowest current that flows into or out of a specified terminal of an integrated circuit at the onset of latch-up.

2 Examples**2.1 Elementary combinatorial circuits****2.1.1 Types of elementary combinatorial circuits and their function tables**

a) L-AND, H-OR circuit

Inputs	Output
A B C	Q
L L L . . . L	L
All combinations with H	H

b) L-NAND, H-NOR circuit

Inputs	Output
A B C	Q
L L L . . . L	H
All combinations with H	L

c) H-AND, L-OR circuit

Inputs	Output
A B C	Q
H H H . . . H	H
All combinations with L	L

d) H-NAND, L-NOR circuit

Inputs	Output
A B C	Q
H H H . . . H	L
All combinations with L	H

e) Binary inverter

Input	Output
L	H
H	L

2.1.2 Realization of logic operations by means of elementary combinatorial circuits

(for two possible assignments of the signal values L and H to the binary values 0 and 1 of Boolean algebra)

Circuit		Assignment	
Type	Name	L $\equiv$ 1 H $\equiv$ 0	L $\equiv$ 0 H $\equiv$ 1
a	L-AND, H-OR	AND	OR
b	L-NAND, H-NOR	NAND	NOR
c	L-NOR, H-AND	OR	AND
d	L-NOR, H-NAND	NOR	NAND

2.2 Principles of characterizing bistable circuits and related sequential digital circuits, shown by examples using letter designations

Two different ways of presenting the (sequential) function matrices are quoted.

2.2.1 Preamble

2.2.1.1 If the signal applied to the input terminal concerned is:

- active when it is at the H-level,
- or active during the transition from the L-level to the H-level,

then the letter which represents the input is used without a bar.

Examples: R, S, J ...

If the signal applied to the input terminal concerned is:

- active when it is at the L-level (i.e. NOT AT THE H-LEVEL),
- or active during the transition from the H-level to the L-level (i.e. NOT DURING THE TRANSITION FROM THE L-LEVEL TO THE H-LEVEL),

then the letter which represents the input is used with a bar.

Examples: $\bar{R}$, $\bar{S}$, $\bar{J}$...

In cases of level/transition-operated circuits where the above gives rise to contrary indications, priority is given to the transition.

2.2.1.2 The output terminals of a bistable circuit are denoted by Q and Q^* , where Q is the reference-output terminal.

2.2.1.3 Normally, in the two stable output configurations (output patterns) of a bistable circuit, the levels at the terminals Q and Q^* are complementary.

The pseudo-stable output configuration (output pattern) is stated by the letters H or L or combinations thereof, to be put in brackets following the letters RS , when it occurs.

If, in the pseudo-stable output configuration (output pattern), the levels at Q and Q^* are complementary, both the letters H and L are used, the first letter designating the level at Q .

If, in the pseudo-stable output configuration (output pattern), the levels at Q and Q^* are the same, only one letter is used to designate these levels.

Examples: $RS(H)$, $RS(L)$, $RS(HL)$, $RS(LH)$.

If not required, the brackets and letters between them can be omitted.

2.2.1.4 All other types of RS , $R_G S_G$, JK , $J_T K_T$ circuits, etc., can be described in a manner analogue to the examples that follow.

2.2.2 Circuits

2.2.2.1 $RS (L)$ circuit

A circuit having two level-operated input terminals R and S . Either input signal can be active in the H -level only.

The input configuration (input pattern) $(R, S) = (L, H)$ produces the output configuration (output pattern) $(Q, Q^*) = (H, L)$. The return of the input signal at the S terminal to the L -level produces no action.

The input configuration (input pattern) $(R, S) = (H, L)$ produces the output configuration (output pattern) $(Q, Q^*) = (L, H)$. The return of the input signal at the R terminal to the L -level produces no action.

The input configuration (input pattern) $(R, S) = (H, H)$ produces the pseudo-stable output configuration (output pattern) $(Q, Q^*) = (L, L)$. The simultaneous return of both input signals from the H -level to the L -level produces a non-foreseeable stable output configuration (output pattern).

NOTE – In some cases, the input configuration (input pattern) $(R, S) = (H, H)$ may not be permitted due to technical reasons.

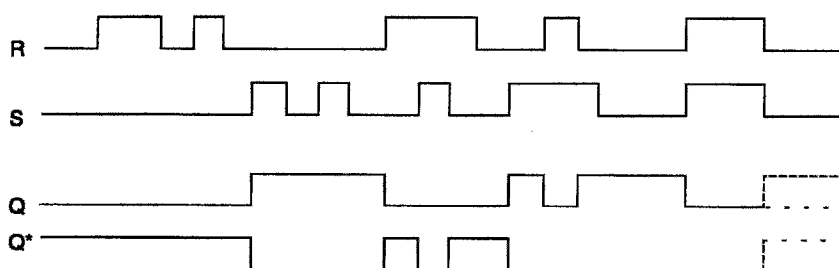
Function (sequential) matrices:

R	L		H			
S	L		H	L	Q	Q*
	①	①	3	2	H	L
	②	1	3	②	L	H
	?	1	③	2	L	L

R	L		H			
S	L		H	L	Q	Q*
					H	L
					L	H
	?				L	L

IEC 1659/97

Timing diagram:



IEC 1660/97

Figure 1

2.2.2.2 $\overline{R}\overline{S}$ (H) circuit

A circuit having two level-operated input terminals $\overline{R}$ and $\overline{S}$. Either input signal can be active in the L-level only.

The input configuration (input pattern) $(\overline{R}, \overline{S}) = (H, L)$ produces the output configuration (output pattern) $(Q, Q^*) = (H, L)$. The return of the input signal at the S terminal to the H-level produces no action.

The input configuration (input pattern) $(\overline{R}, \overline{S}) = (L, H)$ produces the output configuration (output pattern) $(Q, Q^*) = (L, H)$. The return of the input signal at the R terminal to the H-level produces no action.

The input configuration (input pattern) $(\overline{R}, \overline{S}) = (L, L)$ produces the pseudo-stable output configuration (output pattern) $(Q, Q^*) = (H, H)$. The simultaneous return of both input signals from the L-level to the H-level produces a non-foreseeable stable output configuration (output pattern).

NOTE – In some cases, the input configuration (input pattern) $(\overline{R}, \overline{S}) = (L, L)$ may not be permitted due to technical reasons.

Timing diagram:

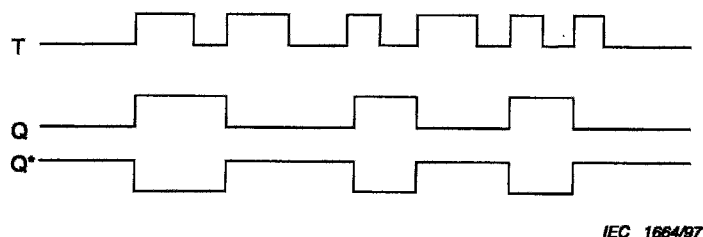


Figure 3

2.2.2.4 $\bar{T}$ circuit

A circuit having one input terminal, $\bar{T}$, which is transition-operated.

When the signal applied to the input terminal $\bar{T}$ changes from the H-level to the L-level, it produces change-over of the output configuration (output pattern).

The return of the input signal from the L-level to the H-level produces no action.

Function (sequential) matrices:

$\bar{T}$	L	H	Q	Q*
	2	①	L	H
	②	3	H	L
	4	③	H	L
	④	1	L	H

$\bar{T}$	L	H	Q	Q*
	•		L	H
		•	H	L
	•		H	L
		•	L	H

IEC 1665/97

Timing diagram:

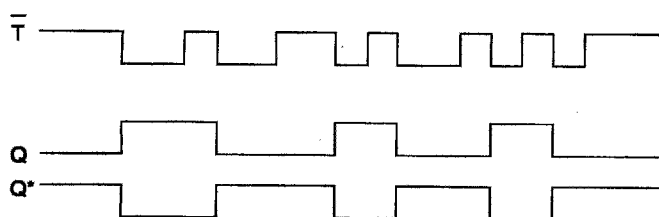


Figure 4

2.2.2.5 General T_G circuit

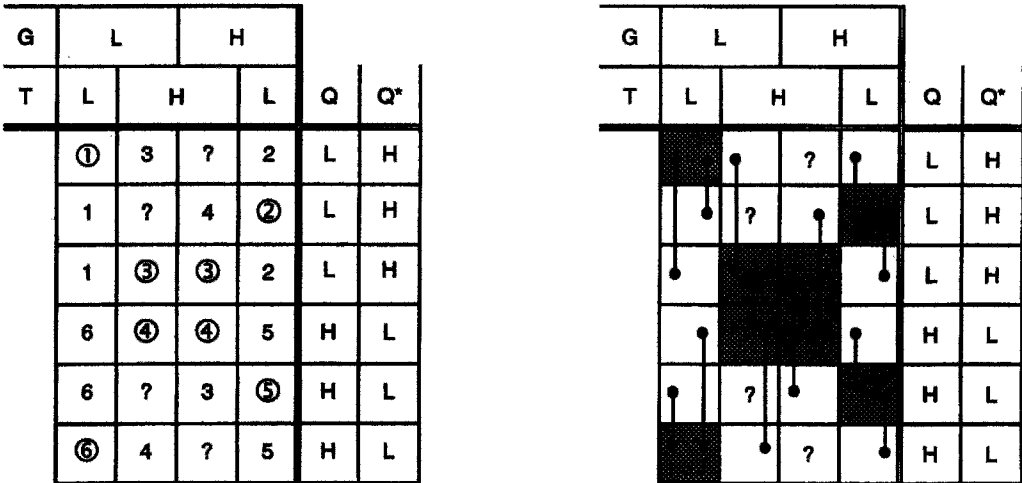
A circuit having one transition-operated input terminal, T, and one level-operated input terminal, G.

While the G input signal has the H-level, the circuit functions like a T circuit.

While the G input signal has the L-level, the T input signal has no effect on the output configuration (output pattern).

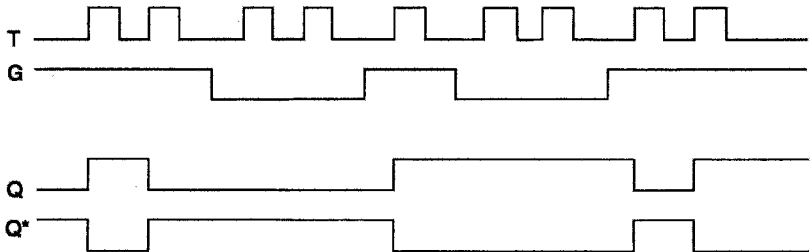
The simultaneous change of both input signals produces a non-foreseeable output configuration (output pattern) if the T input signal changes from the L-level to the H-level and the G input signal changes, either from the L-level to the H-level, or from the H-level to the L-level.

Function (sequential) matrices:



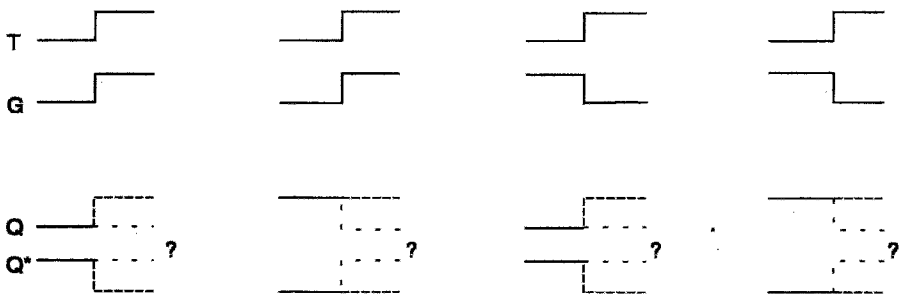
IEC 1687/97

Timing diagram:



IEC 1688/97

Timing diagram of general T_G circuit (continued):



IEC 1689/97

Figure 5

Function (sequential) matrices of the T_G circuit with T delayed with respect to G :

G	L	H	L/H		
T	H		L	Q	Q*
	2	3	①	L	H
	②	②	1	L	H
	③	③	4	H	L
	3	2	④	H	L

G	L	H	L/H		
T	H		L	Q	Q*
	•	•		L	H
			•	L	H
			•	H	L
	•			H	L

IEC 1670/97

Function (sequential) matrices of the T_G circuit with G delayed with respect to T :

G	L	L/H	H		
T	L	H	L	Q	Q*
	①	①	2	L	H
	1	3	②	L	H
	③	③	4	H	L
	3	1	④	H	L

G	L	L/H	H		
T	L	H	L	Q	Q*
			•	L	H
	•	•		L	H
			•	H	L
	•	•		H	L

IEC 1671/97

Figure 6

2.2.2.6 (Transition-operated) JK circuit

A circuit having two transition-operated input terminals, J and K, for which the input signals are active during the change from the L-level to the H-level.

When the signal applied to the J input terminal changes from the L-level to the H-level, it produces the output configuration (output pattern) $(Q, Q^*) = (H, L)$. The return to the input signal at the J terminal to the L-level produces no action.

When the signal applied to the K input terminal changes from the L-level to the H-level, it produces the output configuration (output pattern) $(Q, Q^*) = (L, H)$. The return of the input signal at the K terminal to the L-level produces no action.

The simultaneous change of both input signals from the L-level to the H-level produces change-over of the output configuration (output pattern).

The return of either, or both, input signals to the L-level produces no action.

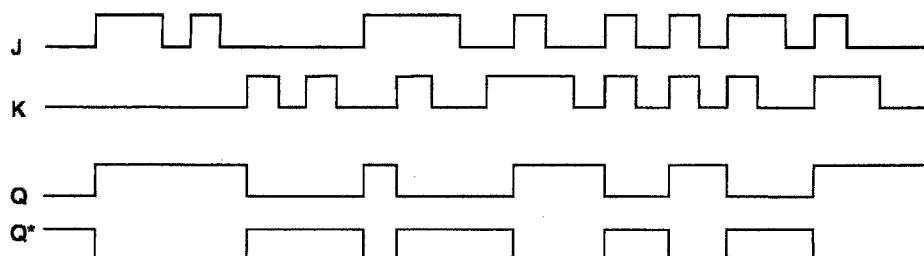
Function (sequential) matrices:

K	L		H			
J	L	H	L	H	Q	Q*
	①	4	3	①	L	H
	1	②	②	1	L	H
	4	4	③	③	H	L
	④	④	2	1	H	L

K	L		H			
J	L	H	L	H	Q	Q*
					L	H
					L	H
					H	L
					H	L

IEC 1672/97

Timing diagram:



IEC 1673/97

Figure 7

2.2.2.7 (Transition-operated) $\bar{J}$, $\bar{K}$ circuit

Description analogous to 2.2.2.6, but where the input signals are active during the change from H-level to L-level.

2.2.2.8 D_G circuit

A circuit having two level-operated input terminals D and G.

While the G input signal has the H-level, the level at the reference output terminal Q is the same as the level of the D input signal.

When the G input signal changes from the H-level to the L-level, the output configuration (output pattern) is maintained.

While the G input signal has the L-level, the D input signal has no effect.

The simultaneous change of both input signals produces a non-foreseeable output configuration (output pattern) if the G input signal changes from the H-level to the L-level and the D input signal changes either from the L-level to the H-level, or from the H-level to the L-level.

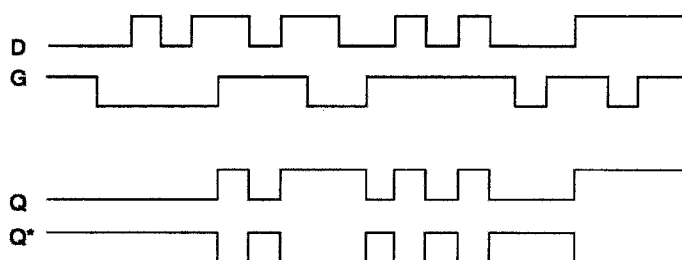
Function (sequential) matrices (these matrices apply only for the case where D is delayed with respect to G):

G	L	H			
D	L/H	H	L	Q	Q*
①	2	①	L	H	
②	②	1	H	L	

G	L	H			
D	L/H	H	L	Q	Q*
				L	H
				H	L

IEC 1674/97

Timing diagram:



IEC 1675/97

Figure 8

2.2.2.9 $D_{\overline{G}}$ circuit

A circuit having two level-operated input terminals, D and $\overline{G}$.

While the $\overline{G}$ input signal has the L-level, the level at the reference output terminal Q is the same as the level of the D input signal.

When the $\overline{G}$ input signal changes from the L-level to the H-level, the output configuration (output pattern) is maintained.

While the $\overline{G}$ input signal has the H-level, the D input signal has no effect.

The simultaneous change of both input signals produces a non-foreseeable output configuration (output pattern) if the $\overline{G}$ input signal changes from the L-level to the H-level and the D input signal changes either from the L-level to the H-level, or from the H-level to the L-level.

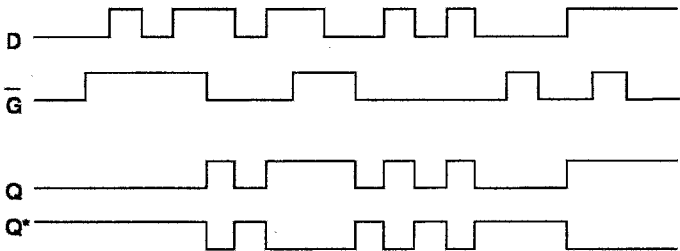
Function (sequential) matrices (these matrices apply only for the case where D is delayed with respect to $\overline{G}$):

$\overline{G}$	L		H		
D	L	H	L/H	Q	Q*
	①	2	①	L	H
	1	②	②	H	L

$\overline{G}$	L		H		
D	L	H	L/H	Q	Q*
				L	H
				H	L

IEC 1678/97

Timing diagram:



IEC 1677/97

Figure 9

2.2.2.10 D_T circuit

A circuit having one level-operated input terminal, D, and one transition-operated input terminal, T.

The change of the T input signal from the L-level to the H-level produces at the reference output terminal Q a level which is the same as the level of the D input signal.

When the T input signal changes from the H-level to the L-level, the output configuration (output pattern) is maintained.

While the T input signal has either the L-level or the H-level, the D input signal has no effect.

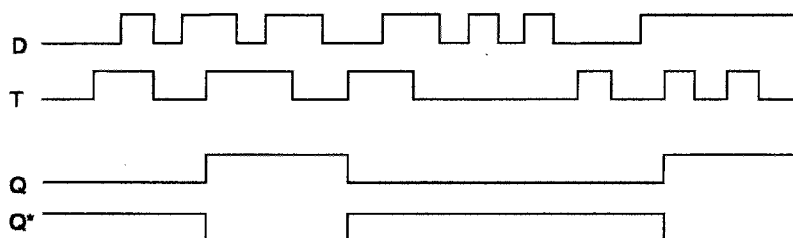
Function (sequential) matrices (these matrices apply only for the case where D is delayed with respect to T):

T	L		H		
D	L	H	L/H	Q	Q*
	①	2	①	L	H
	1	②	3	L	H
	4	③	③	H	L
	④	3	1	H	L

T	L		H		
D	L	H	L/H	Q	Q*
				L	H
				L	H
				H	L
				H	L

IEC 1679/97

Timing diagram:



IEC 1679/97

Figure 10

2.2.2.11 $D_{\bar{T}}$ circuit

A circuit having one level-operated input terminal, D, and one transition-operated input terminal, $\bar{T}$.

The change of the $\bar{T}$ input signal from the H-level to the L-level produces at the reference output terminal Q a level which is the same as the level of the D input signal.

When the $\bar{T}$ input signal changes from the L-level to the H-level, the output configuration (output pattern) is maintained.

While the $\bar{T}$ input signal has either the H-level or the L-level, the D input signal has no effect.

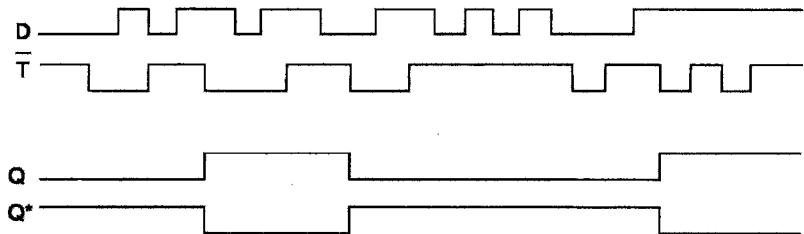
Function (sequential) matrices (these matrices apply only for the case where D is delayed with respect to $\bar{T}$):

$\bar{T}$	L		H			
D	L/H	H	L	Q	Q*	
	①	2	①	L	H	
	3	②	1	L	H	
	③	③	4	H	L	
	1	3	④	H	L	

$\bar{T}$	L		H			
D	L/H	H	L	Q	Q*	
				L	H	
				L	H	
				H	L	
				H	L	

IEC 1680/97

Timing diagram:



IEC 1681/97

Figure 11

2.2.2.12 $R_G S_G (L)$ circuit

A circuit having three level-operated input terminals, R, S and G for which H is the active level.

While the G input signal has the H-level, the circuit functions as a RS (L) circuit.

When the G input signal changes from the H-level to the L-level, the output configuration (output pattern) is maintained, provided that it is not pseudo-stable.

When the output configuration (output pattern) is pseudo-stable, i.e. $(Q, Q^*) = (L, L)$, the change of the G input signal from the H-level to the L-level produces a non-foreseeable output configuration (output pattern).

While the G input signal has the L-level, the R and S input signals have no effect.

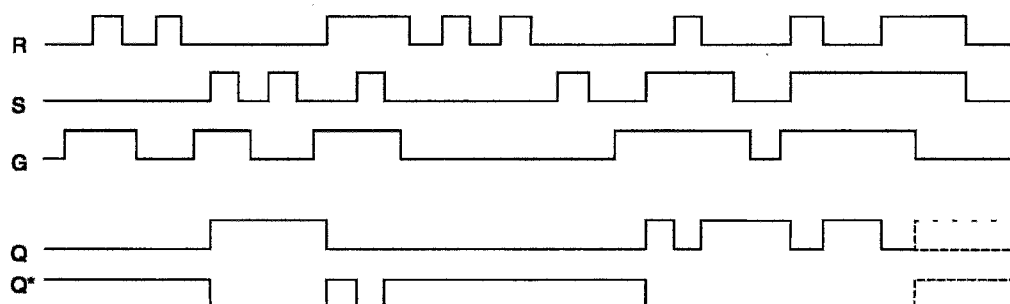
Function (sequential) matrices:

G	L				H				Q	Q*
R	L		H				L			
S	L	H		L		H		L		
	①	2	2	①	①	5	4	①	L	H
	1	②	②	1	1	5	4	?	L	H
	4	4	③	③	1	5	4	?	H	L
	④	④	3	3	1	5	④	④	H	L
	?	?	?	?	1	⑤	4	?	L	L

G	L				H				Q	Q*
R	L		H				L			
S	L	H		L	H		L			
									L	H
									L	H
									H	L
									H	L
									L	L

IEC 1682/97

Timing diagram:



IEC 1683/97

Figure 12

2.2.2.13 $R_{\overline{G}}S_{\overline{G}}$ (L), $\overline{R}_G\overline{S}_G$ (H) and $\overline{R}_{\overline{G}}\overline{S}_{\overline{G}}$ (H) circuits

Description analogous to 2.2.2.12.

2.2.2.14 J_TK_T circuit

A circuit having two level-operated input terminals, J and K, and one transition-operated input terminal, T.

When the T input signal changes from the L-level to the H-level, an input configuration (output pattern) corresponding to the levels of the J and K input signals is produced as follows:

For the input configuration (input pattern) (J, K) = (L, H),
the output configuration (output pattern) (Q, Q*) = (L, H).

For the input configuration (input pattern) (J, K) = (H, L),
the output configuration (output pattern) (Q, Q*) = (H, L).

For the input configuration (input pattern) (J, K) = (H, H),
change of the output configuration (output pattern).

For the input configuration (input pattern) (J, K) = (L, L),
the output configuration is maintained.

The return for the T input signal from the H-level to the L-level has no effect. When the T input signal has either the H-level or the L-level, the J and K input signals have no effect.

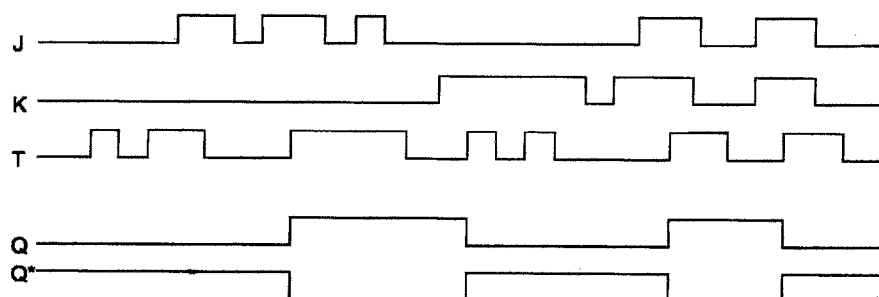
Function (sequential) matrices (the following matrices apply only for the case where J and K are delayed with respect to T):

T	L				H		
K	L		H		L/H		
J	L	H		L	L/H	Q	Q*
	①	2	2	①	①	L	H
	1	②	②	1	4	L	H
	4	4	③	③	1	H	L
	④	④	3	3	④	H	L

T	L				H		
K	L		H		L/H		
J	L	H		L	L/H	Q	Q*
						L	H
						L	H
						H	L
						H	L

IEC 1684/87

Timing diagram:



IEC 1685/97

NOTE – Definitions for the other classes of $J_T K_T$ circuits are still under consideration.

Figure 13

2.2.2.15 $J_T K_T$, $\bar{J}_T \bar{K}_T$ and $\bar{J}_T \bar{K}_T$ circuits

Descriptions analogous to 2.2.2.14.

2.2.2.16 $\bar{R} \bar{S}$ (H), $\bar{J}_T \bar{K}_T$ circuit

Function (sequential) matrices:

	$\bar{R}\bar{S}$		JK				T		
$\bar{S}$	L	H	H				H		
$\bar{R}$	L	H	L	H				H	
T	X		H				L		
J	X		H		L		X		
K	X		L	H	L	X		Q	Q*
	3	4	①	2	2	①	①	L	H
	3	4	1	②	②	1	1	4	L
	③	4	1	?	?	?	?	H	H
	3	④	1	④	5	5	④	H	L
	3	4	1	4	⑤	⑤	4	1	H

	$\bar{R}\bar{S}$		JK				T		
$\bar{S}$	L	H	H				H		
$\bar{R}$	L	H	L	H				H	
T	X		H				L		
J	X		H		L		X		
K	X		L	H	L	X		Q	Q*
	•	•	•	•	•	•	•	L	H
	•	•	•	•	•	•	•	L	H
	•	•	•	•	•	•	•	H	H
	•	•	•	•	•	•	•	H	L
	•	•	•	•	•	•	•	H	L

IEC 1686/97

3 Terminology for integrated circuit memories

3.1 General terms

3.1.1 Memory cell (or memory element)

The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

3.1.2 Integrated circuit memory

An integrated circuit consisting of memory cells (elements) and usually including associated circuits such as those for address selection, amplifiers, etc.

3.1.3 Storage zone of data

A subdivision of the memory, including one or several memory cells, that is the smallest part of the memory that can be selected.

NOTE – The content of a storage zone of data is usually called a "word".

3.1.4 Address

A group of bits that identifies a particular storage zone of data

or:

the appropriate electrical signals applied to the inputs to access this storage zone.

3.1.5 Destructive readout

A reading process that causes the loss of stored information from the storage zone that has been read.

3.1.6 Block

A continuous range of memory addresses.

NOTE – The number of addresses in the range is frequently equal to 2^n .

3.1.7 Erase

To remove information from a memory.

3.2 General terms relating to memory function and organization

3.2.1 Organization of information storage

3.2.1.1 Bit-oriented organization

An arrangement in which the storage zones each consist of one memory cell.

3.2.1.2 Word-oriented organization

An arrangement in which the storage zones each consist of a defined number of memory cells that form a word.

3.2.1.3 Block-oriented organization

An arrangement in which the storage zones form a block.

NOTE – The storage zones in a block may each contain a different number of memory cells.

3.2.2 Presentation of information

3.2.2.1 Parallel presentation of information

The simultaneous transmission of several bits of data on separate channels or bus lines.

3.2.2.2 Serial presentation of information

The transmission of several bits of data in succession on a single channel or bus line.

3.2.3 Mode of addressing

3.2.3.1 Parallel addressing

The selection of a storage zone by the simultaneous presentation of each bit of the address.

3.2.3.2 Serial addressing

The selection of a storage zone by the presentation in succession of each bit of the address.

3.2.3.3 Multiplexed addressing, serial-parallel addressing

The selection of a storage zone by the presentation of several groups of bits that together constitute the address, the bits of each group being presented in parallel and the groups themselves being presented in series.

3.3 Types of memories

3.3.1 Read-only memory (ROM)

A memory in which the contents are intended to be read only and not to be altered during normal operation.

NOTE – Unless otherwise qualified, the term "read-only memory" implies that the data content is determined by its structure and is unalterable.

3.3.1.1 Fixed-programmed read-only memory

A read-only memory in which the data content of each cell (element) is determined during manufacture, and is thereafter unalterable.

a) Mask-programmed read-only memory

A fixed-programmed read-only memory in which the data content of each cell (element) is determined during manufacture by the use of a mask.

3.3.1.2 Field-programmable read-only memory

A read-only memory that, after being manufactured, can have the data content of each memory cell (element) altered.

a) Programmable read-only memory (PROM)

A field-programmable read-only memory that can have the data content of each memory cell (element) altered once only.

b) Reprogrammable read-only memory

A field-programmable read-only memory that can have the data content of each memory cell (element) altered more than once.

3.3.2 Read/write memory

A memory in which each cell (element) may be selected by applying appropriate electrical input signals, and in which the stored data may be either:

- a) sensed at appropriate output terminals, or
- b) changed in response to other appropriate electrical input signals.

3.3.3 Random-access memory (RAM)

A memory that permits access to any of its address locations in any desired sequence.

NOTE – By common usage, this term usually denotes a "read/write" memory; but it could also apply to a "read-only" memory.

3.3.4 Static read/write memory

A memory in which the data content is retained in the absence of control signals.

NOTE 1 – The words "read/write" may be omitted from the term when no misunderstanding may occur.

NOTE 2 – A static memory may use dynamic addressing and/or sensing circuits.

3.3.5 Dynamic read/write memory

A memory in which the cells (elements) require the repetitive application of control signals in order to retain the data stored.

NOTE 1 – The words "read/write" may be omitted from the term when no misunderstanding may occur.

NOTE 2 – Such repetitive application of the control signals is normally called a refresh operation.

NOTE 3 – A dynamic memory may use static addressing and/or sensing circuits.

NOTE 4 – This definition applies whether or not the control signals are generated inside or outside the memory.

3.3.6 Volatile memory

A memory in which the data content is lost when power is no longer supplied to it.

3.3.7 Serial access memory

A memory in which storage zones can only be accessed in a predetermined sequence.

3.3.8 Content addressable memory (CAM) (associative memory)

A memory that responds with all the data in a storage zone if a portion of that data matches the data used for addressing the memory.

NOTE – If a match could occur in more than one storage zone, then usually the data read out will be that contained in the storage zone having the lowest address value.

3.4 Terms related to ratings and characteristics

3.4.1 Cycle

A sequence of operations necessary to perform one of the functions of the memory.

In general, four possible cycles can be identified, i.e.:

- a) Read.
- b) Write.
- c) Read-write.
- d) Write-read.

3.4.2 Cycle time (see notes 1, 2 and 3)

The time interval necessary to perform one cycle, i.e. the time interval between the start of a cycle and the end of that cycle.

a) Read cycle time

The time interval between the start and the end of a read cycle.

b) Write cycle time

The time interval between the start and the end of a write cycle.

c) Read-write cycle time

The time interval between the start of a cycle in which the memory is read and new data are entered, and the end of that cycle.

NOTE – The term "read-modify-write cycle" is sometimes used as an alternative title for "read-write cycle"; however, this usage is deprecated because "read-modify-write" is also used in another context to indicate that data are extracted, processed, and then re-entered into the memory.

d) Write-read cycle time

The time interval between the start of a cycle in which data are entered and the memory is then read, and the end of that cycle.

NOTE 1 – These times are the actual time intervals between two pulses, and may be insufficient for the completion of operations within the memory. In each case, a minimum value is specified that is the shortest time in which the memory will perform its corresponding function(s) correctly.

NOTE 2 – The "end of a cycle" is to be understood as the earliest instant at which any subsequent cycle can start with correct functioning of the memory.

NOTE 3 – A cycle is always performed for a constant address.

3.4.3 Write recovery time (see note 1 to 3.4.2)

The time interval between the termination of a write pulse and the initiation of a new cycle, this time interval being provided for the memory to recover from a write operation and operate correctly.

3.4.4 Sense recovery time

The time interval needed to switch a memory from a write mode to a read mode, and to obtain valid data signals at the output.

3.4.5 Access time

The time interval between the application of a specific input pulse, other necessary inputs being already present, and the availability of valid data signals at an output.

The access time can only be defined with reference to an output signal (read operation).

NOTE – Examples of various access times are:

Address access time: time between address input and data output.

Enable access time: time between enable input and data output.

Read access time: time between input and data output.

In general, there are two values for each access time, depending on whether the output goes to the high level or to the low level.

3.4.6 Refresh time interval

The time interval between the beginning of successive signals that are intended to restore the level in a dynamic memory cell to its original level.

NOTE – The refresh time interval is the actual time between two refresh operations and may be insufficient to protect the stored data. A maximum value is specified that is the longest interval for which correct operation is guaranteed.

3.4.7 Precharge time (of a dynamic memory)

The time interval between specified transitions at one or more inputs that allows the internal nodes of the circuit to be charged or discharged to predetermined voltage levels prior to the start of a new cycle.

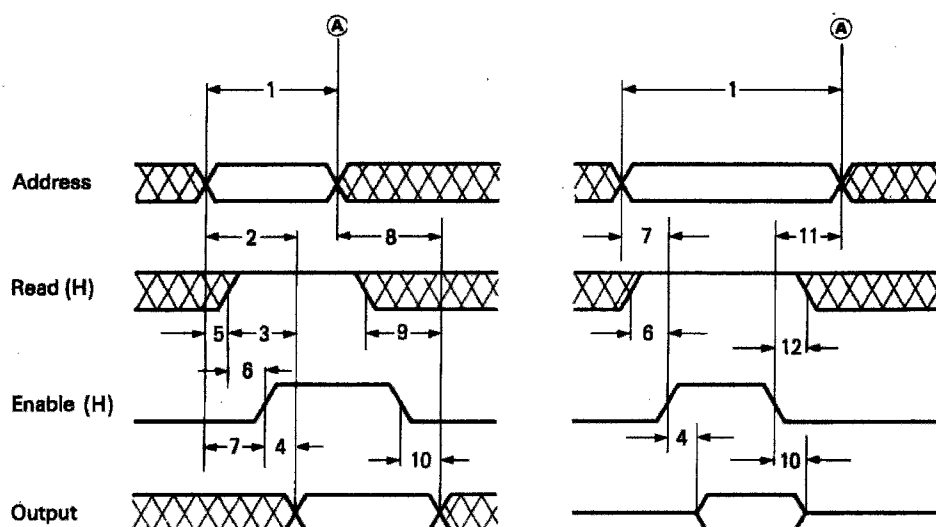
NOTE – This defines the actual precharge time interval, which is determined by the system in which the device is to operate. A minimum value is specified that is the shortest interval for which correct operation of the device is guaranteed.

3.5 Typical waveforms for static read/write memories

NOTE – Four waveform diagrams are shown to illustrate the definitions of "cycle times" (given in 3.4.2) for four modes of operation. These diagrams are examples only; they are for static memories, and do not necessarily represent any particular memory device.

They are not intended to indicate the precise points on the waveforms between which the various times are measured. These points shall be part of the specification for a particular integrated circuit.

The diagram also include some additional terms to assist understanding, though no formal titles or definitions exist for those additional terms at present.



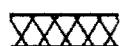
IEC 1687/97

Typical waveforms

- 1 = read cycle time
- 2 = address access time
- 3 = read access time
- 4 = enable access time
- 5 = address set-up time before read
- 6 = read set-up time before enable
- 7 = address set-up time before enable
- 8 = output valid time after address
- 9 = output valid time after read
- 10 = output valid time after enable
- 11 = address hold time after enable
- 12 = read hold time after enable

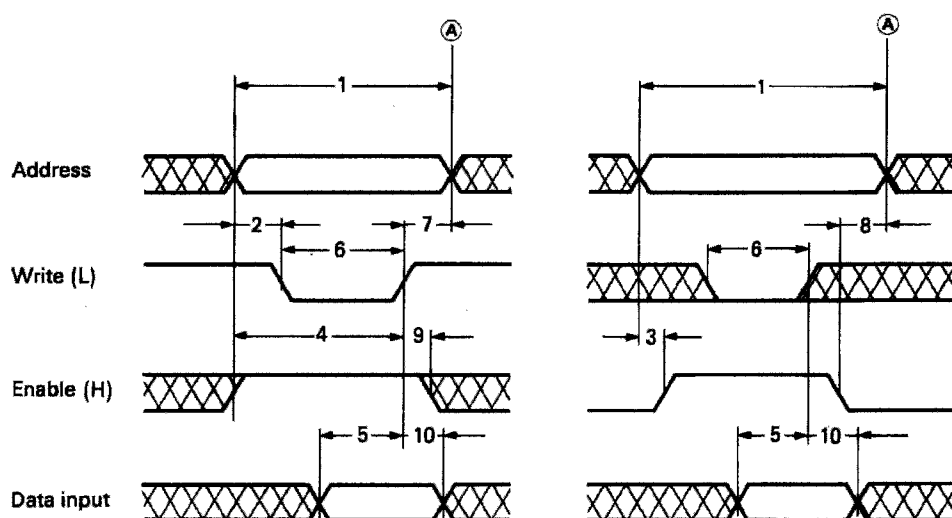
Point A is the earliest instant at which a subsequent cycle can start.

The active levels for the read and enable inputs are indicated by the letters in parentheses (H or L).



input : irrelevant
output : unknown or changing

Figure 14 – Read cycle



IEC 1688/97

Typical waveforms

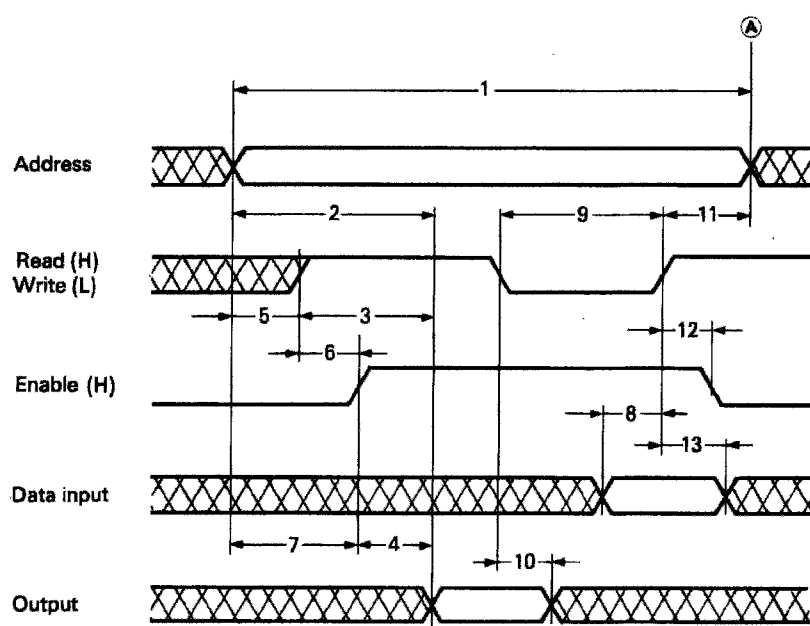
- 1 = write cycle time
- 2 = address set-up time before write
- 3 = address set-up time before enable
- 4 = enable set-up time before (end of) write
- 5 = data-in set-up time before (end of) write
- 6 = write pulse duration
- 7 = address hold time after write
- 8 = address hold time after enable
- 9 = enable hold time after write
- 10 = data-in hold time after write

Point **A** is the earliest instant at which a subsequent cycle can start.

The active levels for the write and enable inputs are indicated by the letters in parentheses (H or L).

 input : irrelevant
 output : unknown or changing

Figure 15 – Write cycle



IEC 1689/97

Typical waveforms

- 1 = read-write cycle time
- 2 = address access time
- 3 = read access time
- 4 = enable access time
- 5 = address set-up time before read
- 6 = read set-up time before enable
- 7 = address set-up time before enable
- 8 = data-in set-up time before (end of) write
- 9 = write pulse duration
- 10 = output valid time after read
- 11 = address hold time after write
- 12 = enable hold time after write
- 13 = data-in hold time after write

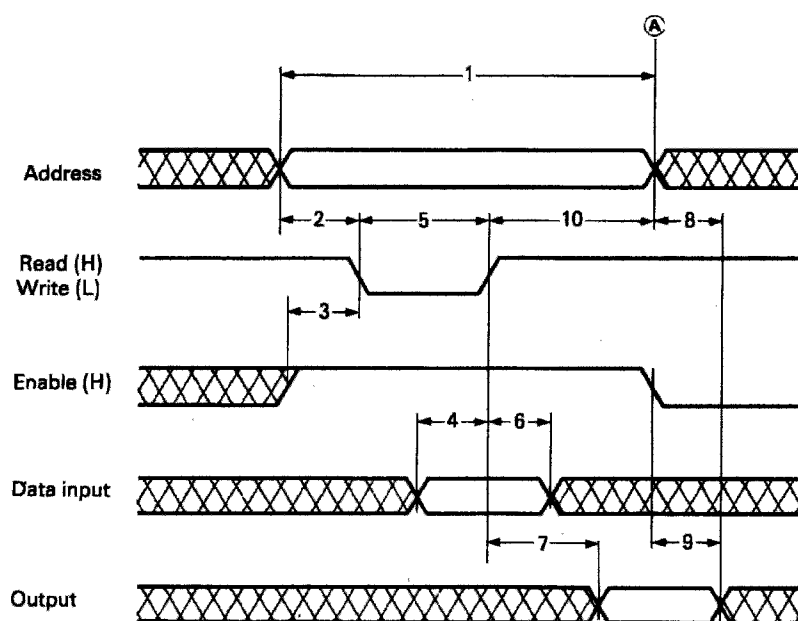
Point A is the earliest instant at which a subsequent cycle can start.

The active levels for the read/write and enable inputs are indicated by the letters in parentheses (H or L).



input : irrelevant
output : unknown or changing

Figure 16 – Read-write cycle



IEC 1690/97

Typical waveforms

- 1 = write-read cycle time
- 2 = address set-up time before write
- 3 = enable set-up time before write
- 4 = data-in set-up time before (end of) write
- 5 = write pulse duration
- 6 = data-in hold time after write
- 7 = sense recovery time
- 8 = output valid time after address
- 9 = output valid time after enable
- 10 = write recovery time

Point **A** is the earliest instant at which a subsequent cycle can start.

The active levels for the write-read and enable inputs are indicated by the letters in parentheses (H or L).



input : irrelevant
output : unknown or changing

Figure 17 – Write-read cycle

3.6 Terms and descriptions for test patterns for memory testing

3.6.1 Introduction

3.6.1.1 Working definitions for principal terms

3.6.1.1.1 Data pattern

An array of logic ZEROs (0's) and logic ONEs (1's) within a field of memory cells.

NOTE – A field is usually subdivided into "rows" and "columns".

3.6.1.1.2 Address sequence

A specified sequence of addresses.

3.6.1.1.3 Test pattern

A specified address sequence with the operations specified for each address so as to create a specified data pattern.

3.6.1.2 General

The enumeration given in 3.6.2 to 3.6.4.2 is not exhaustive and is limited to descriptions only.

No considerations are made regarding elapsed test times or failure modes and related test patterns. All test patterns described in subclause 3.6.4 are intended to perform tests on a specified data pattern. For each description, an assumption is made on the allocation of the memory addresses to the topological location of the memory cells. On this basis, the address sequence is chosen.

In practice, a different allocation may be chosen by the manufacturer, for example, in a 4 k RAM, cell number 4095 may be located in the upper left corner of the field of memory cells, adjacent to cell number 0. Then the address sequence corresponding to the specified data pattern shall be changed accordingly.

In all specifications, the address sequence corresponding to the specified data pattern shall be stated by the manufacturer. Examples given are based on a square field where the numbers of "rows" and "columns" are equal.

To the extent that much of the information given relates to data patterns within the memory, the logic symbols "0" and "1" have been used (instead of L and H).

NOTE – N means the number of memory cells. The addresses run from 0 to N-1.

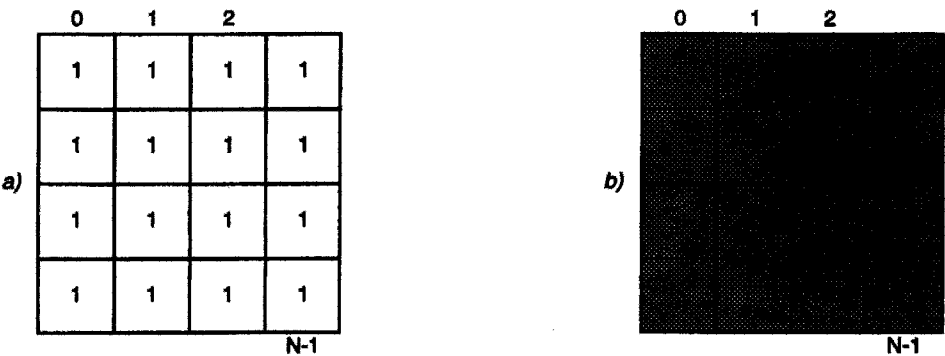
3.6.2 Data patterns

In the figures representing data patterns, the number of memory cells is represented by the sequence 0 to N-1, where N is the total number of cells. The numbering used is row-by-row and from left to right.

NOTE – Representations may be in either logical or graphical form as shown in the a) or b) versions of the figures given.

3.6.2.1 All ONE (all ZERO)

A data pattern consisting of all 1s (all 0s) (see figure 18 for all 1s).

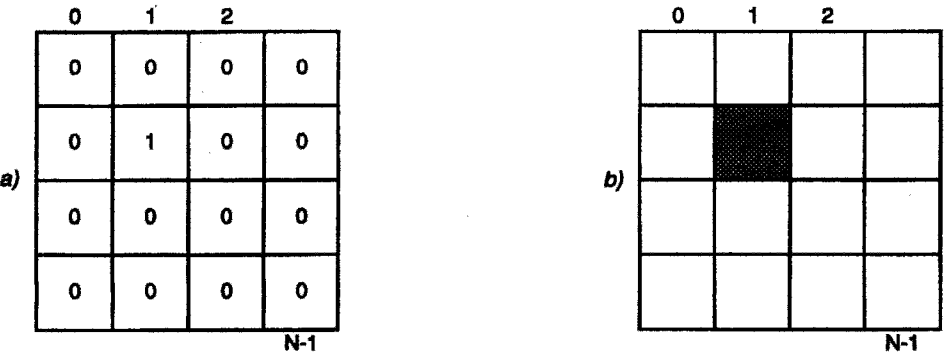


IEC 1691/97

Figure 18

3.6.2.2 Single ONE (single ZERO)

A data pattern consisting of a single 1 (single 0) on a background of all 0s (all 1s) (see figure 19 for a single 1).

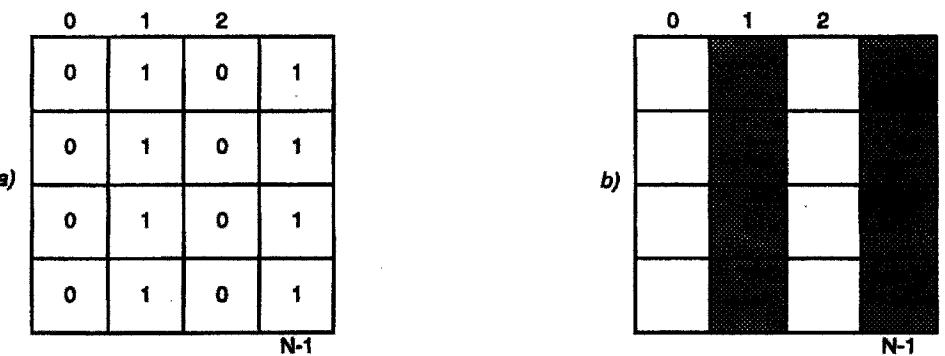


IEC 1692/97

Figure 19

3.6.2.3 Column bars

A data pattern of alternating columns of 0s and 1s (see figure 20).

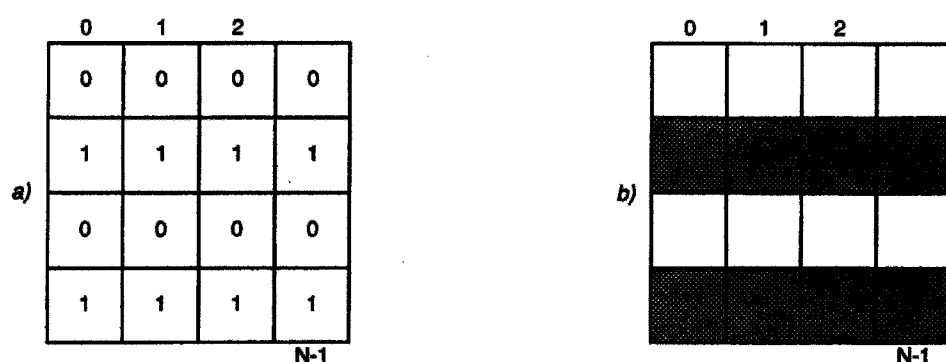


IEC 1693/97

Figure 20

3.6.2.4 Row bars

A data pattern of alternating rows of 0s and 1s (see figure 21).



IEC 1694/97

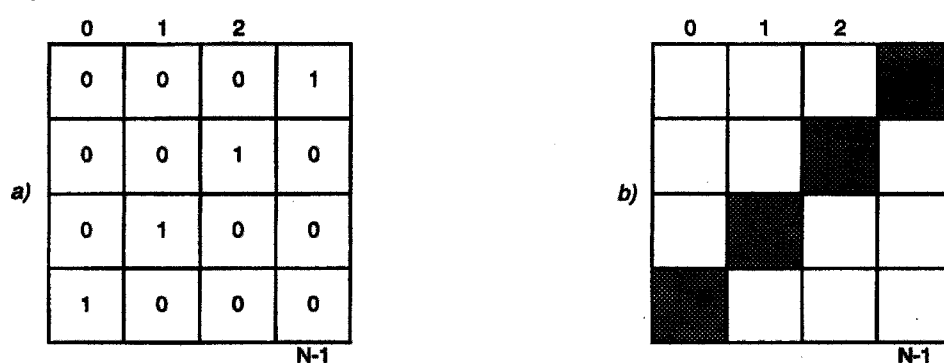
Figure 21

3.6.2.5 Diagonal

A data pattern of diagonal 1s or 0s on the background of complementary data.

NOTE – In a square array of memory cells, "diagonal" denotes a configuration in which all cells are located either on a main diagonal (see figure 22) or on two parallel diagonals such that only one memory cell is located in each row and each column (see figure 23).

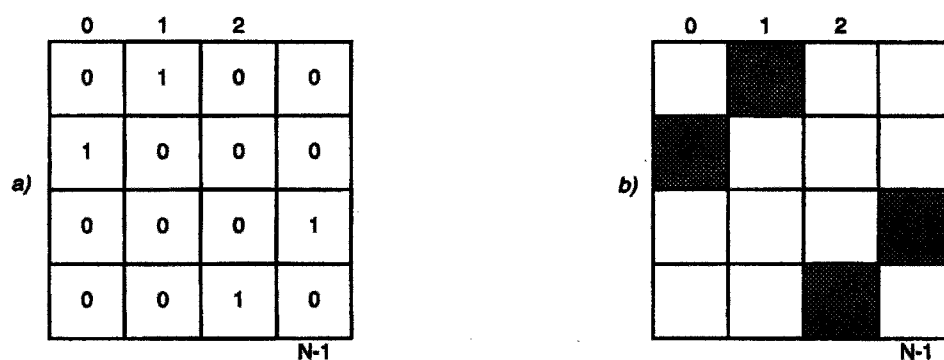
Example 1:



IEC 1695/97

Figure 22

Example 2:

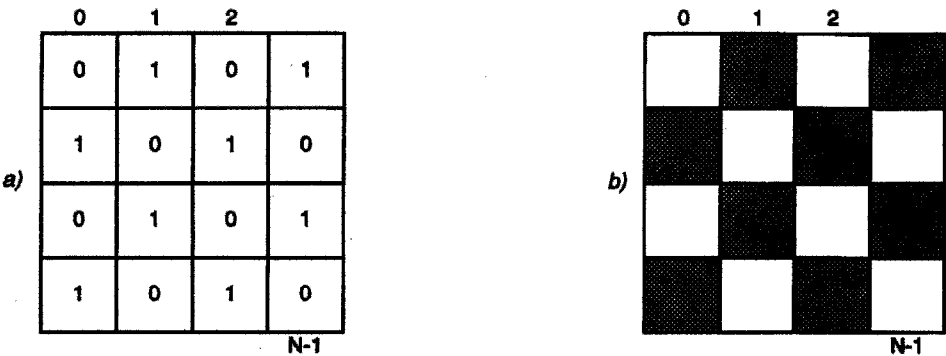


IEC 1696/97

Figure 23

3.6.2.6 Checkerboard

A data pattern of alternating 0s and 1s in both directions (that is, columns and rows) (see figure 24).



IEC 1697/97

Figure 24

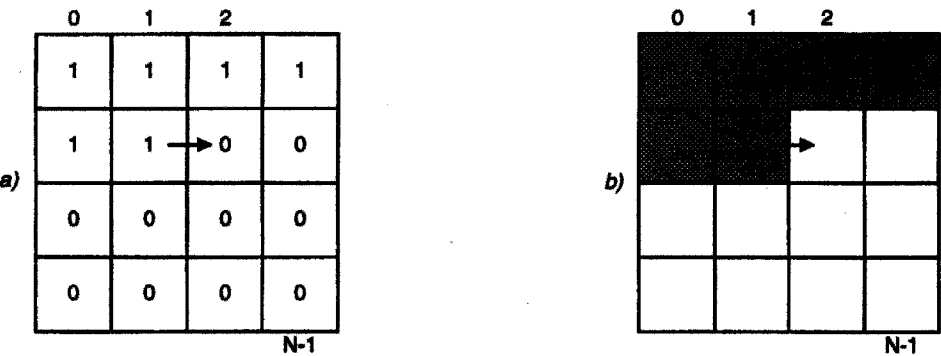
3.6.3 Address sequences

NOTE – By means of suitable address sequences, data patterns can be shifted, complemented or extended within memory fields.

3.6.3.1 Marching

An address sequence by means of which all cells are sequentially read and rewritten with complementary data.

NOTE – Background data and rewritten data are complementary to each other (see figure 25).



IEC 1698/97

Figure 25

3.6.3.2 Walking

An address sequence by means of which a specified pattern in one or more consecutive cells is shifted through the whole memory, all cells except those written with the shifted pattern being read after each shifting (see figure 26).