

Semiconductor devices — Integrated circuits —

Part 4: Interface integrated circuits

ICS 31.200

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Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, the IEC title page, pages ii to vi, pages 1 to 134 and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

This British Standard, having been prepared under the direction of the Electrotechnical Sector Board, was published under the authority of the Standards Board and comes into effect on 15 September 1997

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ISBN 0 580 28094 2

Amendments issued since publication

Amd. No.	Date	Comments

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**NORME
INTERNATIONALE
INTERNATIONAL
STANDARD**

**CEI
IEC**

60748-4

QC 790300

Deuxième édition
Second edition
1997-04

**Dispositifs à semiconducteurs –
Circuits intégrés –**

**Partie 4:
Circuits intégrés d'interface**

**Semiconductor devices –
Integrated circuits –**

**Partie 4:
Interface integrated circuits**



Numéro de référence
Reference number
CEI/IEC 60748-4: 1997

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Chapter I. General

1 Scope

This part of IEC 60748 gives requirements for the following categories or subcategories of interface integrated circuits.

Category I:

- subcategory A: line circuits (transmitters and receivers);
- subcategory B: sense amplifiers;
- subcategory C: peripheral drivers (including memory drivers) and level shifters;
- subcategory D: voltage comparators.

Category II:

- linear and non-linear analogue-to-digital and digital-to-analogue converters.

Category III:

- control circuits for switch-mode power supplies.

Category IV:

- companding PCM coder-decoders (CODEC).

Category V:

- digital interface integrated circuits (UBF).

Category VI:

- integrated service digital network (ISDN).

As stated in the foreword, this standard is to be used in conjunction with IEC 60747-1 and IEC 60748-1. In these standards, the user will find all basic information on:

- terminology;
- letter symbols;
- essential ratings and characteristics;
- measuring methods.

The sequence of the different chapters is in accordance with IEC 60747-1, **2.1**, chapter III.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 60748. At the time of publication, the editions indicated were valid. All normative documents are subject to revision, and parties to agreements based on this part of IEC 60748 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 60134:1961, *Rating systems for electronic tubes and valves and analogous semiconductor devices*.

IEC 60617-12:1996, *Graphical symbols for diagrams — Part 12: Binary logic elements*.

IEC 60747, *Semiconductor devices — Discrete devices*.

IEC 60747-1:1983, *Semiconductor devices — Discrete devices and integrated circuits — Part 1: General*.

IEC 60748, *Semiconductor devices — Integrated circuits*.

IEC 60748-1:1984, *Semiconductor devices — Integrated circuits — Part 1: General*.

IEC 60748-2:1985, *Semiconductor devices — Integrated circuits — Part 2: Digital integrated circuits*.

IEC 60748-3:1986, *Semiconductor devices — Integrated circuits — Part 3: Analogue integrated circuits*.

ITU-T Recommendation G 712:1993, *Transmission performance characteristics of pulse code modulation*.

ITU-T Recommendation | 430:1994, *Basic user-network interface — Layer 1 specification*.

Chapter II. Terminology and letter symbols

1 Category I (line circuits, sense amplifiers, peripheral drivers [including memory drivers] and level shifters, voltage comparators)

1.1 General terms

1.1.1

line transmitter

an integrated circuit operating as a transmitter, the transmitter being coupled to a receiver by a transmission line or similar electrical connection. The transmitter operates with single-ended digital voltage input and provides either single-ended or differential output signals that may be either voltage or current

a strobe facility may also be included

1.1.2

line receiver

an integrated circuit operating as a receiver, the receiver being coupled to a transmitter by a transmission line or similar electrical connection. The receiver accepts either voltage or current signals at the input in either single-ended or differential form, and provides a digital voltage output

a strobe facility may also be included

1.1.3

sense amplifier

an integrated circuit that responds to a signal within a known input voltage range (window) and that will provide a digital output voltage

it usually has a differential input and a single-ended output. Sense amplifiers may have input(s) intended to adjust the input voltage range

a strobe facility may also be included

1.1.4

peripheral driver (including memory driver)

an integral circuit that responds to a digital input voltage and gives a digital output, either voltage or current. The input and output levels may not be compatible. The circuit may have single or multiple outputs

a control facility may be included

1.1.5

level shifter

an integrated circuit that responds to a digital input voltage and gives a digital output, either voltage or current. The input and output levels are not compatible. The circuit may have single or multiple outputs

a control facility may be included

1.1.6

voltage comparator

an integrated circuit that responds to a differential input voltage. It gives a digital output (normally voltage) and may include a strobe facility

1.2 Ratings and characteristics

1.2.1 Input characteristics

1.2.1.1

input impedance (Z_i) [2.1.10, chapter II, IEC 60748-3]

- a) **single-ended (Z_{is})**: The impedance from each input to the electrical reference point.
- b) **differential (-mode) (Z_{id})**: The impedance between two inputs.
- c) **common mode (Z_{ic})**: The impedance between inputs in parallel and the electrical reference point.

1.2.1.2

high-level input voltage (V_{IH})

an input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variable

1.2.1.3**low-level input voltage (V_{IL})**

an input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variable

1.2.1.4**high-level input current (I_{IH})**

the current through an input terminal when a high-level voltage is applied to that input

1.2.1.5**low-level input current (I_{IL})**

the current through an input terminal when a low-level voltage is applied to that input

1.2.1.6**input offset voltage (V_{IO})**

the d.c. voltage that must be applied between the differential input terminals to cause the d.c. output voltage to reach a specified value

NOTE This term is not applicable to circuits with hysteresis transfer characteristics.

1.2.1.7**input offset current (I_{IO})**

the difference between the d.c. currents through two differential input terminals that causes the d.c. output voltage to reach a specified value

NOTE This term is not applicable to circuits with hysteresis transfer characteristics.

1.2.1.8**differential-input voltage range (V_{ID})**

the range of the differential input voltage for which the device functions in accordance with its specification

1.2.1.9**differential-input threshold voltage (V_{IDT})**

the value of the d.c. differential input voltage that causes the digital output variable (for example, voltage, current) of the circuit to just reach the high level when changing from a low level, or vice versa

NOTE The values for the two directions of transition will usually be different.

1.2.1.10**average (mean) bias current (of an interface circuit) (I_{IB})**

the arithmetical average of the currents into specified differential input terminals when the device is in a quiescent state

1.2.1.11**common-mode input voltage (V_{IC})**

the average of the two input voltages [2.1.30, Chapter II, IEC 60748-3]

1.2.1.12**common-mode input triggering voltage (V_{ICT})**

the value of common-mode input voltage at which the output just changes state, for a fixed differential input voltage

1.2.1.13**common-mode rejection ratio (k_{CMR})**

the ratio of the differential-mode voltage amplification to the common-mode voltage amplification, under the same specified conditions [2.1.3, chapter II, IEC 60748-3]

NOTE The abbreviations CMR and CMRR are in common use for this quantity.

1.2.1.14**input (output) clamping voltage ($V_{\text{IK}}, V_{\text{OK}}$)**

an input (output) voltage in a region of relatively low differential resistance that serves to limit the input (output) voltage swing

1.2.1.15**supply voltage rejection ratio (k_{SVR})**

the absolute value of the ratio of the change in one power-supply voltage to the resulting change in input offset voltage, with all remaining power-supply voltages held constant [2.1.25, chapter II, IEC 60748-3]

1.2.2 Output characteristics**1.2.2.1****high-level output voltage (V_{OH})**

the voltage at an output terminal with input conditions applied that will establish a high level at the output

1.2.2.2**low-level output voltage (V_{OL})**

the voltage at an output terminal with input conditions applied that will establish a low level at the output

1.2.2.3**high-level output current (I_{OH})**

the current through an output terminal with input conditions applied that will establish a high level at the output

1.2.2.4**low-level output current (I_{OL})**

the current through an output terminal with input conditions applied that will establish a low level at the output

1.2.2.5**short-circuit output current (I_{OS})**

the current through an output terminal when that terminal is short-circuited to earth (ground) (or other specified potential)

NOTE Normally, the input conditions specified are those that would establish the largest potential difference between the output and earth (ground) (or other specified terminal).

1.2.2.6**off-state (high-impedance state) output current ($I_{o(off)}$, I_{OZ})**

the current through an output terminal with input conditions applied that will cause the output to be in the off-state (high-impedance state)

NOTE Generally the input conditions specified are those that would establish an output potential, if the output enabled this, farthest from the potential applied to the output.

1.2.3 Transfer characteristics**1.2.3.1****differential-mode voltage amplification (A_{VD} , A_{vd})**

the ratio of the change in the magnitude of the output voltage to the change in the magnitude of the differential input voltage under specified conditions [2.1.1, chapter II, IEC 60748-3]

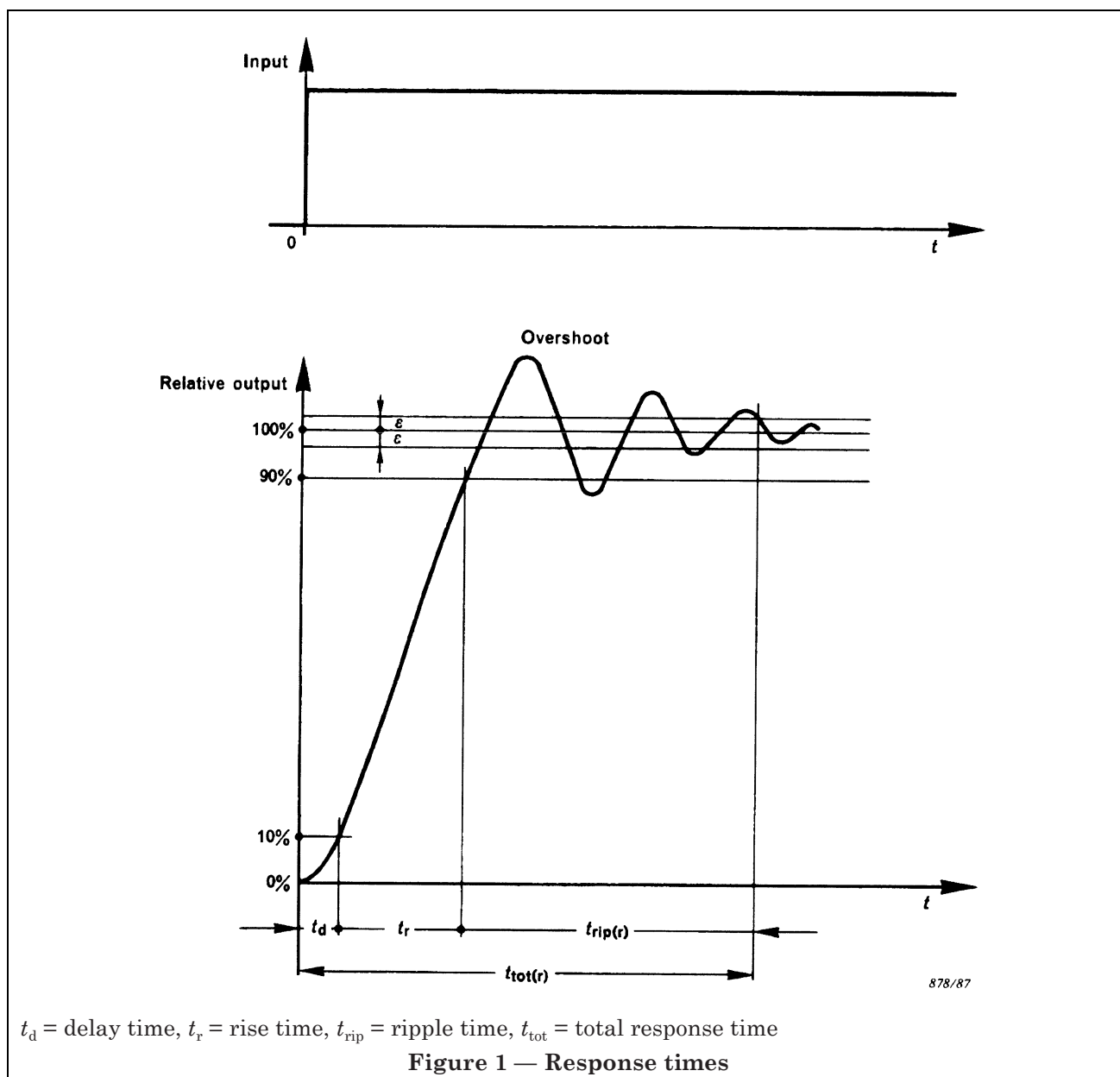
1.2.3.2**response times**

- a) for analogue-input, digital-output devices

- 1) **delay time (t_d)**: The time interval between a step-function change of the input signal level and the instant at which the magnitude of the output signal passes through a specified value which is close to its initial value.

NOTE The level normally specified for the end of the delay time (the beginning of the slope time) is 10 %. The level for the end of the slope time (the beginning of the ripple time) is 90 %.

The difference between the initial and final steady-state values of the output signal is defined as 100 %.



2) **slope time (rise time, fall time)** (t_r , t_f): For a step-function change of the input signal level, the time interval between the end of the delay time and that instant at which the magnitude of the output signal first passes through a specified value close to its final value. [2.1.17, chapter II, IEC 60748-3]

NOTE See note to item 1).

3) **ripple time** (t_{rip}): For step-function change of the input signal level, the time interval between the end of the slope time and that instant at which the magnitude of the output signal reaches, for the last time, a specified level range containing the final output signal level. [2.1.18, chapter II, IEC 60748-3]

4) **total response time** (t_{tot}): The sum of delay time, slope time and ripple time. [2.1.20, chapter II, IEC 60748-3]

b) for digital-input, digital output devices

1) **high-level to low-level (low-level to high-level) propagation time** (t_{PHL} t_{PLH}): The time interval between specified reference points on the input and on the output pulses, when the output is going to the low (high) level and when the device is driven and loaded by typical devices of stated types. [1.4.7, chapter II, IEC 60748-2]

NOTE 1 In some circumstances, the driving and the loading circuits may be replaced for test purposes by equivalent networks, which must be specified.

NOTE 2 The mean value between the upper limit of the input low range and the lower limit of the input high range is generally used as the specified reference level.

2) **high-level to low-level (low-level to high-level) transition time** (t_{THL} t_{TLH}): The time interval between specified reference points on the edge of the output pulse when the output is going to the low (high) level and when a specified input signal is applied through a specified network, and the output is loaded by another specified network. [1.4.8, chapter II, IEC 60748-2]

1.2.3.3

strobe propagation time

the propagation time measured from a specified point on the strobe or similar control input waveform and a specified point on the output waveform

NOTE If applicable, this time includes ripple time.

1.2.3.4

differential-input overload recovery time (t_{ord} , see note to 1.2.3.3)

the time necessary for the device to recover after the cessation of a specified differential overload input signal to the extent that the device can again respond to differential-input voltages in accordance with its specification

1.2.3.5

common-mode-input overload recovery time (t_{orc} , see note to 1.2.3.3)

the time necessary for the device to recover after the cessation of a specified common-mode overload input signal to the extent that the device can again respond to differential input voltages in accordance with its specification

2 Category II (linear and non-linear analogue-to-digital and digital-to-analogue converters)

2.1 General terms

2.1.1

analogue-to-digital converters (ADC)

a converter that uniquely represents all analogue input values within a specified total input range by a limited number of digital output codes, each of which exclusively represents a fractional part of the total analogue input range (see Figure 2a)

NOTE This quantization procedure introduces inherent errors of 1/2 LSB (LSB — least significant bit) in the representation since, within this fractional range, only one (input) analogue value can be represented free of error by a single digital output code.

2.1.2

analogue-to-digital processor

an integrated circuit providing the analogue part of an ADC; provision of external timing, counting and arithmetic operations is necessary for implementing a full analogue-to-digital converter

2.1.3

digital-to-analogue converter (DAC)

a converter that represents a limited number of different digital input codes by a corresponding number of discrete analogue output values (see Figure 2b)

2.1.4

conversion code (of an ADC or a DAC)

the set of correlations between each of the fractional parts of the total analogue input range or each of the digital input codes, respectively, and the corresponding digital output codes or analogue output values, respectively (see Figure 2a and Figure 2b)

2.1.5

step (of an analogue-to-digital or digital-to-analogue conversion)

in the conversion code: any of the individual correlations. In the transfer diagram: any part of the diagram equating to an individual correlation

- For an ADC, a step represents both a fractional range of analogue input values and the corresponding digital output code (see Figure 2a).
- For a DAC, a step represents both a digital input code and the corresponding discrete analogue output value (see Figure 2b).

2.1.6

midstep value (of an ADC)

the analogue value for the centre of the step excluding the steps at the two ends of the total range of analogue values

NOTE For the end steps, the midstep value is defined as the analogue value that results when the analogue value for the transition to the adjacent step is reduced or enlarged as appropriate by half the nominal value of the step width (see Figure 2a and 2.1.10).

2.1.7

step value (of a DAC)

the value of the analogue output representing a digital input code (see Figure 2b)

2.1.8

nominal midstep value (of an ADC)

a specified analogue value within a step that is ideally represented free of error by the corresponding digital output code (see Figure 2a)

2.1.9

nominal step value (of a DAC)

a specified step value that represents free of error the corresponding digital input code (see Figure 2b)

2.1.10

step width (of an ADC)

the absolute value of the difference between the two ends of the range of analogue values corresponding to one step (see Figure 2a)

NOTE The term “step size” can be used instead of “step width”, if no ambiguity is likely to occur e.g. a confusion with “step height” of a DAC (see 2.1.11).

2.1.11

step height (step size) (of a DAC)

the absolute value of the difference in step value between two adjacent steps in the transfer diagram (see Figure 2b)

NOTE 1 For companding DAC, the term “step size” is in general use.

NOTE 2 The term “step size” can be used instead of “step height”, if no ambiguity is likely to occur e.g. a confusion with “step size” for “step width” of an ADC (see 2.1.10).

2.1.12

linear ADC

an ADC having steps ideally of equal width excluding the steps at the two ends of the total range of analogue input values

NOTE Ideally, the width of each end step is one half of the width of any other step (see Figure 2a).

2.1.13

linear DAC

a DAC having steps ideally of equal height (see Figure 2b)

2.1.14

multiplying DAC

a DAC having at least two inputs, at least one of which is digital, and whose analogue output value is proportional to the product of the inputs

2.1.15

non-linear ADC or DAC

an ADC or a DAC with a specified non-linear transfer function between the nominal midstep values or nominal step values, respectively, and the corresponding step widths or step heights, respectively

NOTE The function may be continuously non-linear or piece-wise linear.

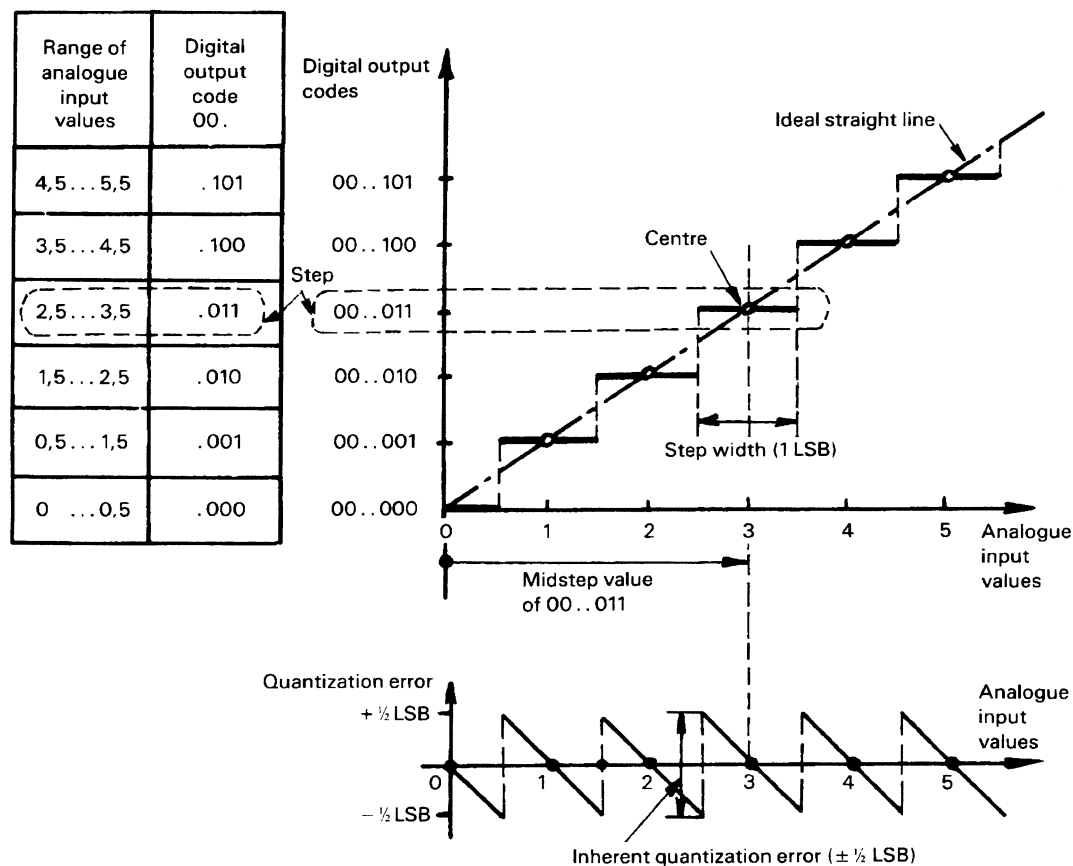


Figure 2a — Ideal linear ADC

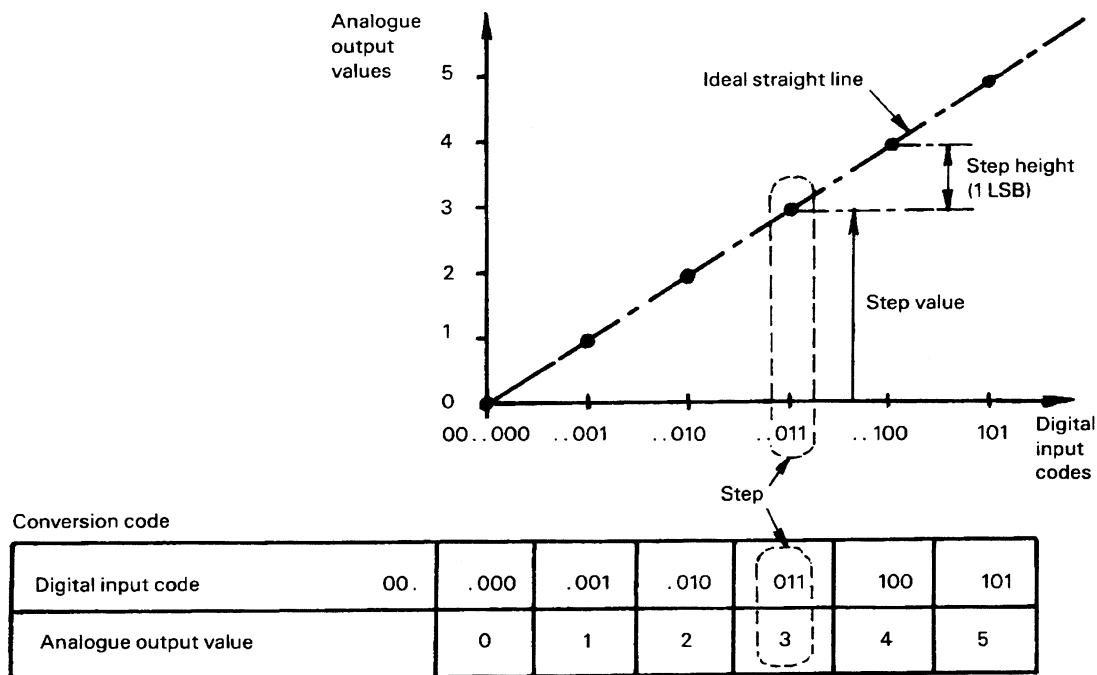


Figure 2b — Ideal linear DAC

Figure 2 — Elements of transfer diagrams

879/87

2.1.16**companding DAC**

a DAC whose transfer function complies with compression or expansion

NOTE The corresponding ADC normally consists of such a corresponding DAC and additional external circuitry.

2.1.17**ideal straight line** (of a linear ADC or DAC)

in the transfer diagram, a straight line between the specified points for the most-positive (least-negative) and most-negative (least-positive) nominal midstep values or nominal step values, respectively (see Figure 2 and Figure 3)

NOTE The ideal straight line passes through all the points for nominal midstep values or nominal step values, respectively.

2.1.18 full-scale ranges (of a linear ADC or DAC) (see Figure 3)**2.1.18.1****(practical) full-scale range** (V_{FSR} , I_{FSR}), (V_{FSRpr} , I_{FSRpr})

the total range of analogue values that correspond to the ideal straight line

NOTE 1 The qualifying adjective “practical” can nearly always be deleted from this term provided that, in a very few critical cases, the term from 2.1.18.2 is not also shortened in the same way. This permits use of the shorter letter symbols or abbreviations (see note 2).

NOTE 2 In place of the letter symbols, the abbreviation “FSR, FSR(pr)” are in common use.

NOTE 3 The (practical) full-scale range has only a nominal value, because it is referred to the end points of the ideal straight line.

Example: Using a straight binary n-bit code format, it follows:

- for an ADC: $\text{FSR} = (2^n - 1) \times (\text{nominal value of step width})$
- for a DAC: $\text{FSR} = (2^n - 1) \times (\text{nominal value of step height})$.

2.1.18.2**nominal full-scale range** (V_{FSRnom} , I_{FSRnom})

the total range in analogue values that theoretically can be coded with constant accuracy by the total number of steps

NOTE In place of the letter symbols, the abbreviation “FSR(nom)” can be used.

Example: Using a straight binary n-bit code format, it follows:

- for an ADC: $\text{FSR(nom)} = 2^n \times (\text{nominal value of step width})$
- for a DAC: $\text{FSR(nom)} = 2^n \times (\text{nominal value of step height})$.

2.1.19 full scale (of an ADC or a DAC) (see Figure 3)**2.1.19.1****full scale** (of an unipolar ADC or DAC)

a term used to refer a characteristic to that step within the transfer diagram whose nominal midstep value or nominal step value has the highest absolute value (see Figure 3a for a linear unipolar ADC)

NOTE 1 The subscript for the letter symbol of a characteristic at full scale is “FS”.

NOTE 2 In place of a letter symbol, the abbreviation “FS” is in common use.

2.1.19.2**positive full scale and negative full scale** (of a bipolar ADC or DAC)

terms used to refer a characteristic to one or the other of the two ends of the transfer diagram, that is, to the steps whose nominal midstep values or nominal step values have the highest absolute values (see Figure 3b and Figure 3c for bipolar linear ADC)

NOTE 1 The subscripts for the letter symbol of characteristics indicating these operating conditions are:

“FS+” for positive full scale ($V_{\text{FS+}}$, $I_{\text{FS+}}$);

“FS−” for negative full scale ($V_{\text{FS−}}$, $I_{\text{FS−}}$).

NOTE 2 In place of letter symbols, the abbreviations “FS+” and “FS−” are in common use.

2.1.20 zero scale (of an ADC or a DAC) (see Figure 3)**2.1.20.1****zero scale** (of an ADC or a DAC with true zero) (see Figure 3a, Figure 3b and Figure 3c)

a term used to refer a characteristic to the step whose nominal midstep value or nominal step value equals zero

NOTE 1 The subscript for the letter symbol of a characteristic at zero scale is “ZS”.

NOTE 2 In place of a letter symbol, the abbreviation “ZS” is in common use.

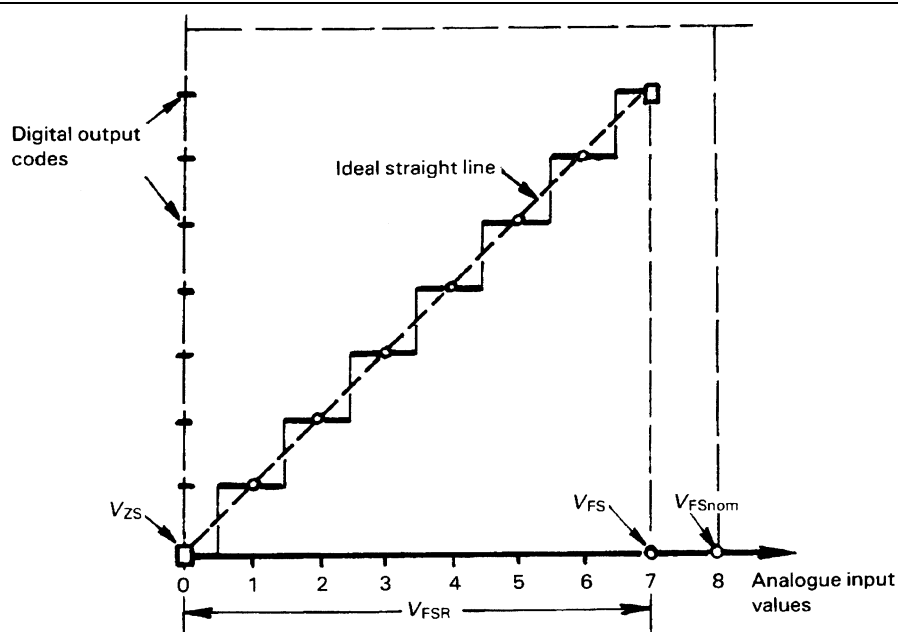


Figure 3a — Unipolar ADC

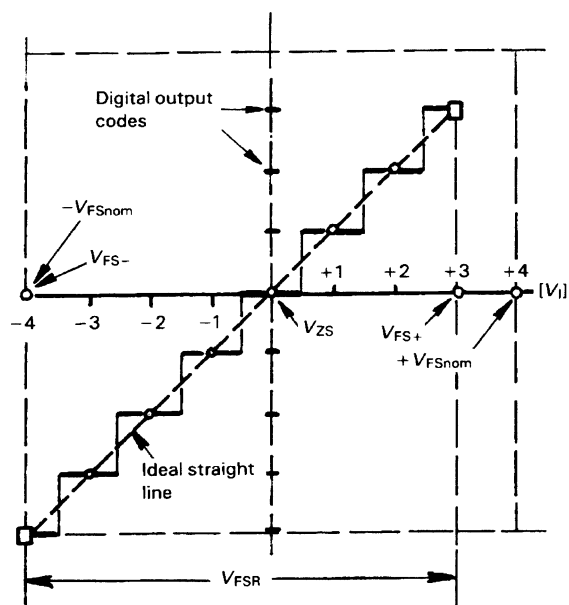


Figure 3b — Bipolar ADC with true zero

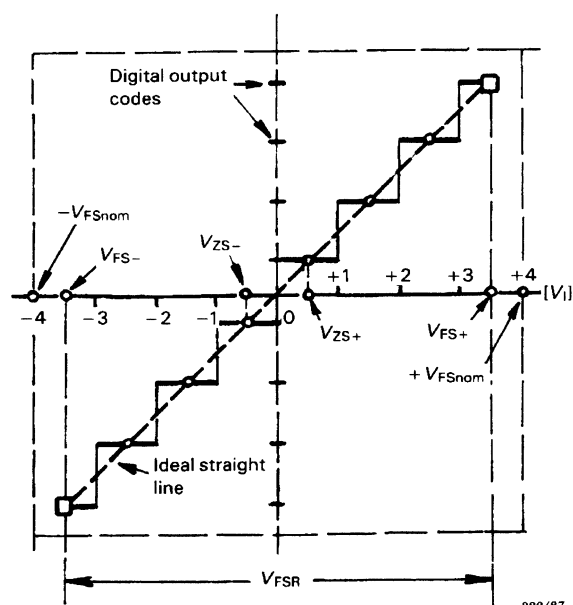


Figure 3c — Bipolar ADC with no true zero

Figure 3 — Ideal straight line, full-scale and zero-scale values (shown for ideal linear ADC)

2.1.20.2

positive zero scale and negative zero scale (of an ADC or a DAC with no true zero) (see Figure 3c)

terms used to refer a characteristic to one or the other of the two steps closest to analogue zero, that is, to the steps whose nominal midstep value or nominal step value have the two lowest absolute values

NOTE 1 The subscripts for the letter symbols of characteristics indicating these operating conditions are:

“ZS+” for positive zero scale (V_{ZS+} , I_{ZS+});

“ZS-” for negative zero scale (V_{ZS-} , I_{ZS-}).

NOTE 2 In place of letter symbols, the abbreviations “ZS+ and ZS-” are in common use.

2.1.21**nominal full-scale value** (V_{FSnom} , I_{FSnom})

a value derived from the nominal full scale range:

- for an unipolar converter: $V_{\text{FSnom}} = V_{\text{FSRnom}}$;
- for a bipolar converter: $V_{\text{FSnom}} = 1/2 V_{\text{FSRnom}}$

(see Figure 3).

NOTE 1 In some data sheets, this analogue value is used as a reference value for adjustment procedures or as a rounded value for the full-scale range(s).

NOTE 2 In place of letter symbols, the abbreviation “FS(nom)” is in common use.

2.1.22 offset characteristics**2.1.22.1****offset point** (of an adjustable ADC or DAC)

a point in the transfer diagram corresponding to the midstep value (for an ADC) or the step value (for a DAC) of the step for which the offset error is specified, and by reference to which the offset adjustment must be performed (see Figure 4)

NOTE The offset adjustment causes only a parallel displacement of the transfer diagram, without changing its slope.

2.1.22.2**offset output current** (of a DAC)

the output current at the offset point

2.1.23**gain point** (of an adjustable ADC or DAC)

a point in the transfer diagram corresponding to the midstep value (for an ADC) or the step value (for a DAC) of the step for which the gain error is specified, and in reference to which the gain adjustment is performed (see Figure 4)

NOTE Gain adjustment causes only a change of the slope of the transfer diagram, without changing the offset error.

2.1.24**gain** (within the transfer diagram of a linear ADC) (G)

the slope of the straight line of the transfer diagram, or of a specified part of it expressed as the quotient of a change in digital output quantity, stated as number of steps, by the change in analogue input quantity producing it

2.1.25**gain** (within the transfer diagram of a linear DAC) (G)

the slope of the straight line of the transfer diagram or of a specified part of it expressed as the quotient of a change in analogue output quantity, by the change in digital input quantity, stated as number of steps, producing it

2.1.26**transition value** (of an ADC) (V_{tr} , I_{tr})

the analogue input value at which the change between two adjacent digital output codes takes place

2.2 Static performance**2.2.1 resolution** (general term) (see notes)

NOTE 1 Resolution is a design parameter, having only a nominal value.

NOTE 2 Resolution as a capability can be expressed in different forms (see 2.2.2, 2.2.3 and 2.2.4).

NOTE 3 The terms for these different forms may all be shortened to “resolution” if no ambiguity is likely to occur (for example, when the dimension of the term is also given).

2.2.1.1**resolution** of an ADC

the degree to which nearly equal values of the analogue input quantity can be distinguished

2.2.1.2**resolution** of a DAC

the degree to which nearly equal values of the analogue output quantity can be produced

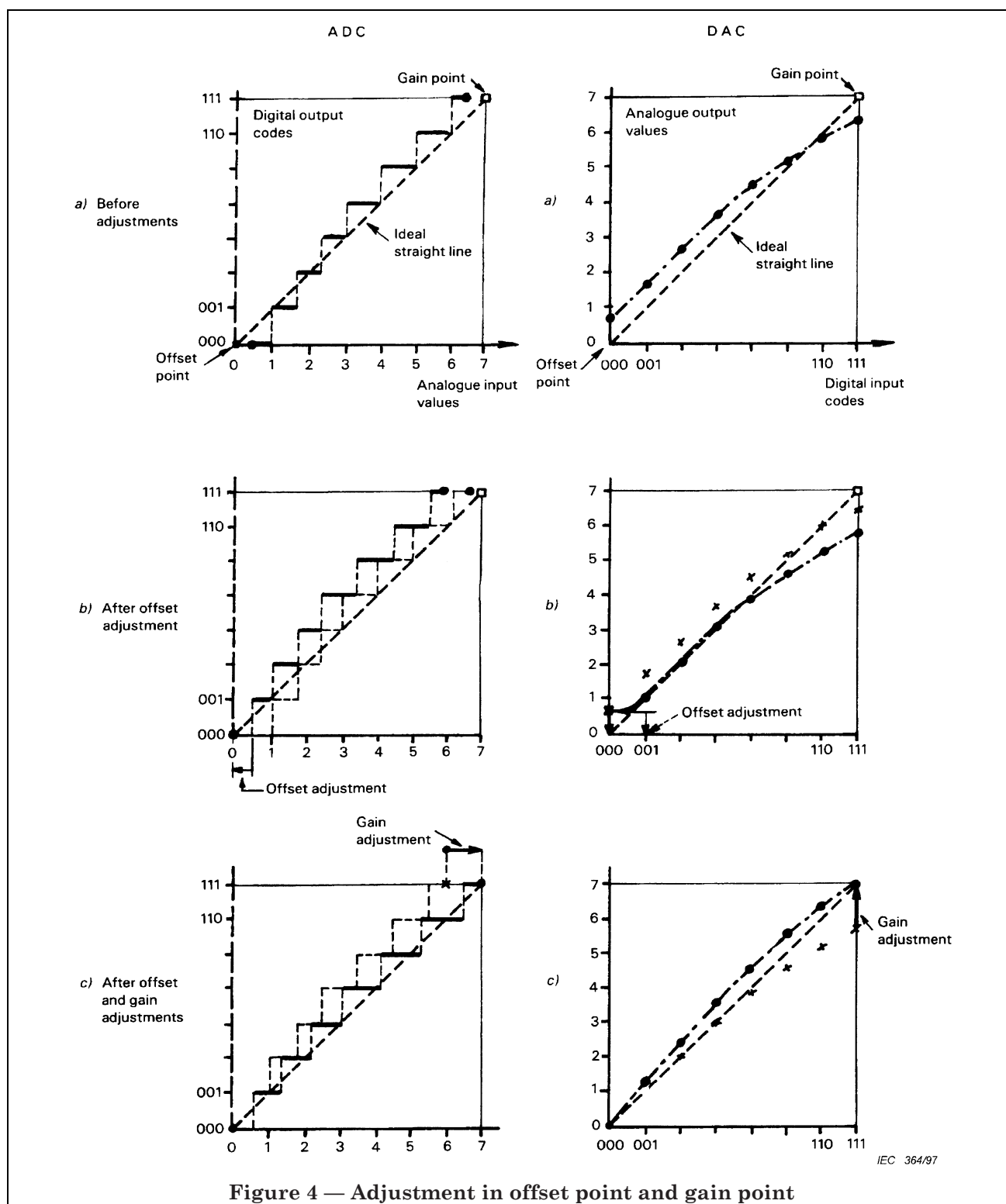
2.2.2

(numerical) resolution

the number (n) of digits in the chosen numbering system necessary to express the total number of steps

NOTE 1 The numbering system is normally a binary or a decimal system.

NOTE 2 In the binary-coded-decimal numbering system, "1/2 digit" is understood to be an additional decimal digit with the highest positional value, but limited to the decimal figures "0" or "1".



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2.2.3 (analogue) resolution

2.2.3.1

(analogue) resolution (of linear or non-linear ADC or DAC):

- For an ADC: the nominal value of the step width.
- For a DAC: the nominal value of the step height.

NOTE For a linear ADC or DAC, the constant magnitude of the analogue resolution is often used as a reference unit: LSB (see 2.2.3.2.1).

2.2.3.2 LSB

NOTE This letter group can have two meanings. In practice, the intended meaning is clarified by the context in which the letter group LSB is used.

2.2.3.2.1

unit symbol LSB (for linear converters only)

unit symbol for the magnitude of the analogue resolution of a linear converter, which serves as a reference unit to express the magnitude of other analogue quantities of that same converter, especially of analogue errors, as multiples or submultiples of the magnitude of the analogue resolution

Example: “1/2 LSB” means an analogue quantity equal to 0,5 times the analogue resolution.

NOTE The unit symbol LSB refers to the fact that, for a natural binary code, the analogue resolution corresponds to the nominal positional weight attributed to the least significant bit of the binary numeral.

In this case, the identity: 1 LSB = analogue resolution leads, for a n-bit resolution to:

$$1 \text{ LSB} = \frac{\text{FSR}}{2^n - 1} = \frac{\text{FSR}(\text{nom})}{2^n}$$

2.2.3.2.2

abbreviation LSB

abbreviation for “least significant bit”, that is, for the bit that has the lowest positional weight in a natural binary numeral

Example: In the natural binary numeral “1010”, the rightmost bit “0” is the LSB.

2.2.4

(relative) resolution (of a linear ADC or DAC)

the ratio between the analogue resolution and the full scale range (practical or nominal)

NOTE This ratio is normally expressed as a percentage of the full scale range [% of FSR, % of FSR(nom)]. For high resolutions (high value of n), it is of small importance whether this ratio refers to the practical or nominal full-scale range.

2.2.5 errors, accuracy

NOTE The definitions of 2.2.5 describe the errors as the difference between the actual value and the nominal value of the analogue quantity. As such they may be expressed in conventional units (for example, millivolts) or as multiples/submultiples of 1 LSB. An error can also be expressed as a relative value, for example, in “% of FSR”. In this case, it is common practice to use the same term as for the analogue value.

2.2.5.1

inherent quantization error (of an ideal ADC)

within a step, the maximum (positive or negative) possible deviation of the actual analogue input value from the nominal midstep value

NOTE 1 This error is inherently due to quantization. For a linear ADC, its value equals $\pm 1/2$ LSB (see Figure 5a).

NOTE 2 The term “resolution error” for the “inherent quantization error” is deprecated, because “resolution” as a design parameter has a nominal value only.

2.2.5.2

offset error (of a linear ADC or DAC) (E_0)

the difference between the actual midstep value (or step value) respectively, and the nominal midstep value (or step value), respectively (see Figure 5a)

NOTE 1 Usually the specified steps for the specification of offset error and gain error are the steps at the ends of the practical full-scale range. For an ADC, the midstep value of these steps is defined as the value for a point 1/2 LSB apart from the adjacent transition (see Figure 5a and Figure 5b).

NOTE 2 The terms “offset error” and “gain error” will only be used for errors that can be adjusted to zero. Otherwise, the term “zero-scale error” and “full-scale error” will be used.

2.2.5.3**gain error** (of a linear ADC or DAC) (E_G)

the difference between the actual midstep value (or step value), respectively, and the nominal midstep value or step value, respectively, in the transfer diagram at the specified gain point, after the offset error has been adjusted to zero (see Figure 5b)

NOTE See notes 1 and 2 to 2.2.5.2.

2.2.5.4 linearity error (of a linear and adjustable ADC or DAC)**2.2.5.4.1****(end-points) linearity error** (of a linear and adjustable ADC) (E_L)

the difference between the actual analogue value at the transition between any two adjacent steps and its ideal value, after offset error and gain error have been adjusted to zero (see Figure 6a)

NOTE 1 The short term “linearity error” is in common use when no ambiguity with the “best-straight-line linearity error” (2.2.5.4.3) is likely to occur.

NOTE 2 The inherent quantization error is not included in the linearity error of an ADC. The ideal value for the transition corresponds to the nominal midstep value $\pm 1/2$ LSB.

2.2.5.4.2**(end-points) linearity error** (of a linear and adjustable DAC) (E_L)

the difference between the actual step value and the nominal step value, after offset error and gain error have been adjusted to zero (see Figure 6a)

NOTE The short term “linearity error” is in common use when no ambiguity with the “best-straight-line linearity error” (2.2.5.4.4) is likely to occur.

2.2.5.4.3**best-straight-line linearity error** (of a linear and adjustable ADC) ($E_{L(adj)}$)

the difference between the actual analogue value at the transition between any two adjacent steps and its ideal value, after offset error and gain error have been adjusted to minimize the extreme values of this difference (either positive or negative) (see Figure 6b)

NOTE 1 The inherent quantization error is not included in the best-straight-line linearity error of an ADC. The ideal value for the transition corresponds to the nominal midstep value $\pm 1/2$ LSB.

NOTE 2 For an uniformly curved transfer diagram, the extreme values will yield half of the apparent absolute value of the end-points linearity error (see Figure 6b).

2.2.5.4.4**best-straight-line linearity error** (of a linear and adjustable DAC) ($E_{L(adj)}$)

the difference between the actual step value and the nominal step value, after offset error and gain error have been adjusted to minimize the extreme value of this difference (either positive or negative) (see Figure 6b)

NOTE For an uniformly curved transfer diagram, the extreme values will yield half of the apparent absolute value of the end-points linearity error (see Figure 6b).

2.2.5.5**differential linearity error** (of a linear ADC or DAC) (E_D)

the difference between the actual step width or step height and the ideal value (1 LSB) (see Figure 7)

NOTE A differential linearity error greater than 1 LSB can lead to missing codes in an ADC or to non-monotonicity of a DAC (see Figure 8 and Figure 9).

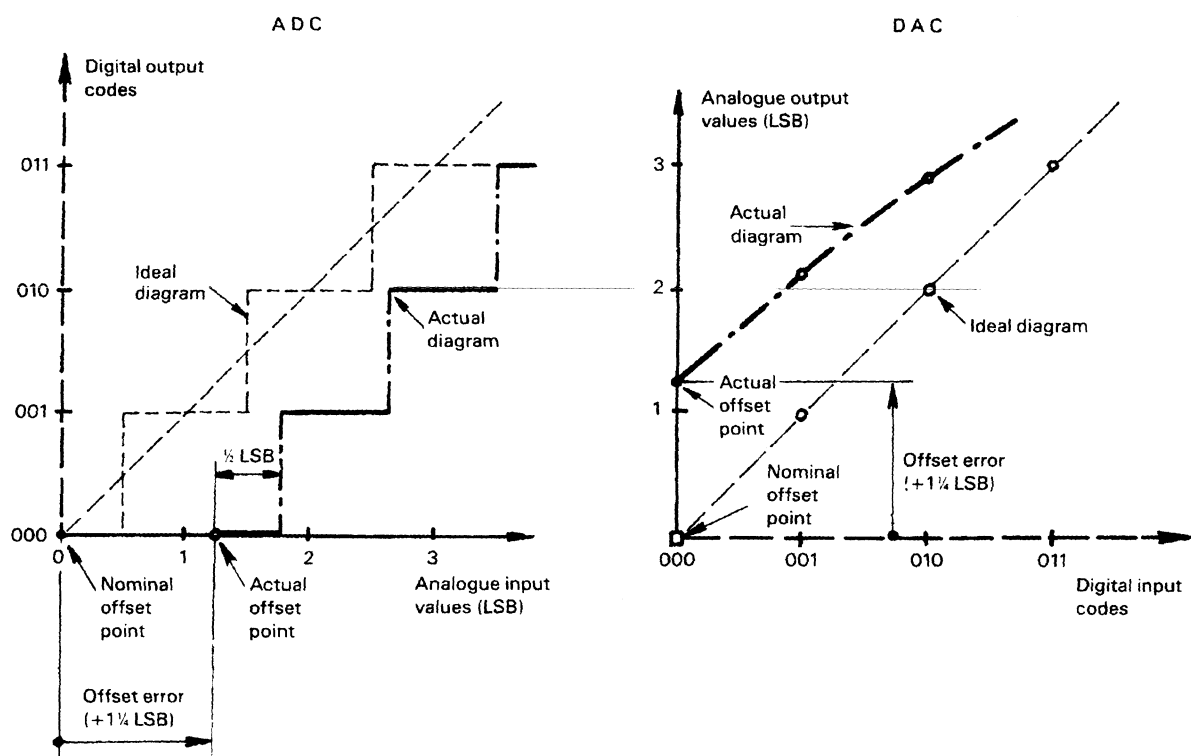


Figure 5a — Offset error (specified at step 000)

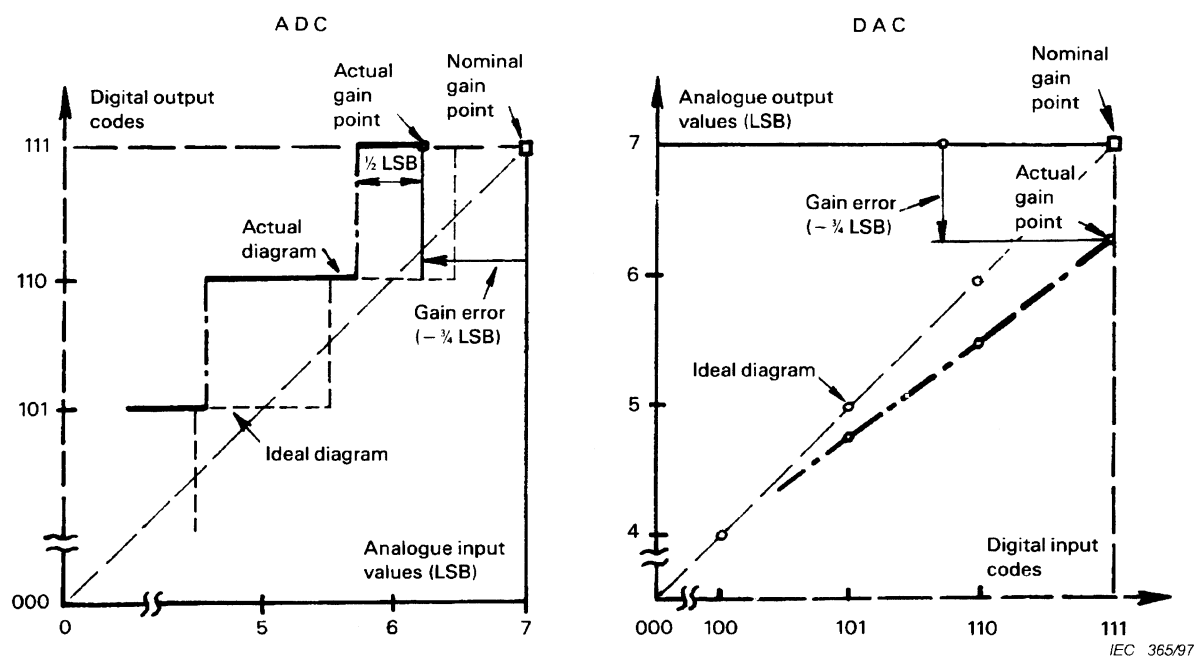


Figure 5b — Gain error (after correction of the offset error) (specified at step 111)

Figure 5 — Offset error, gain error (of a linear 3-bit natural binary-coded converter)

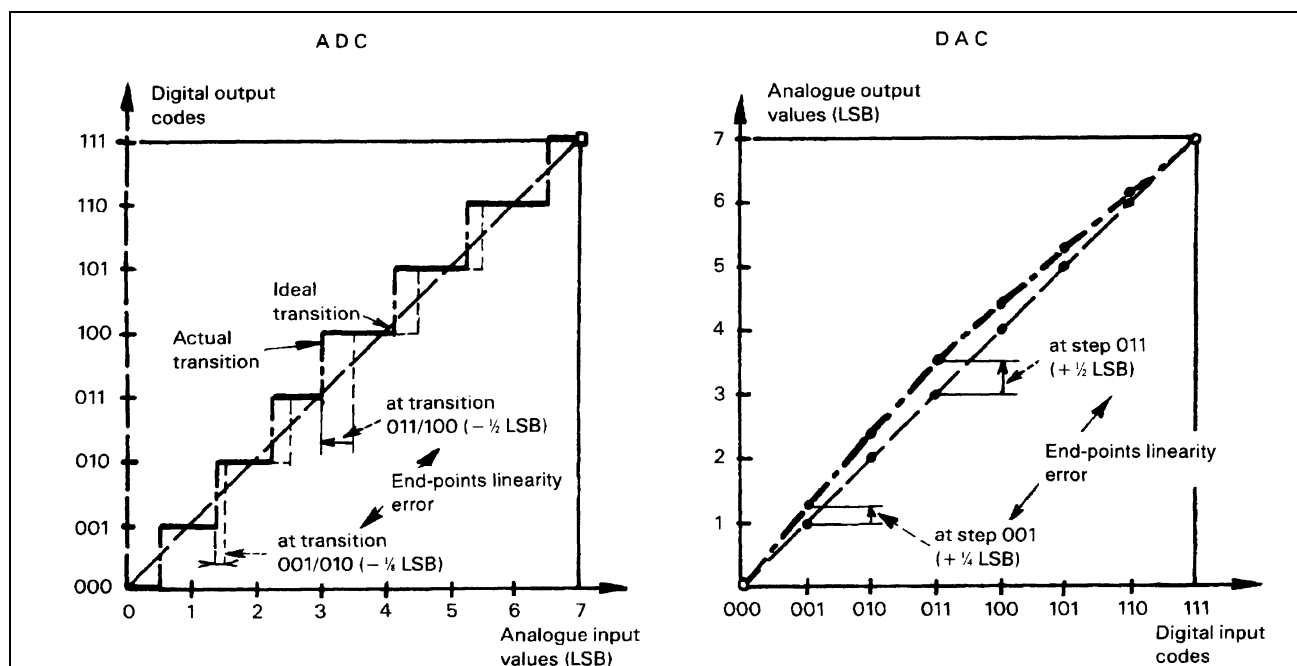


Figure 6a — End-points linearity error of a linear ADC or DAC (offset error and gain error are adjusted to the value zero)

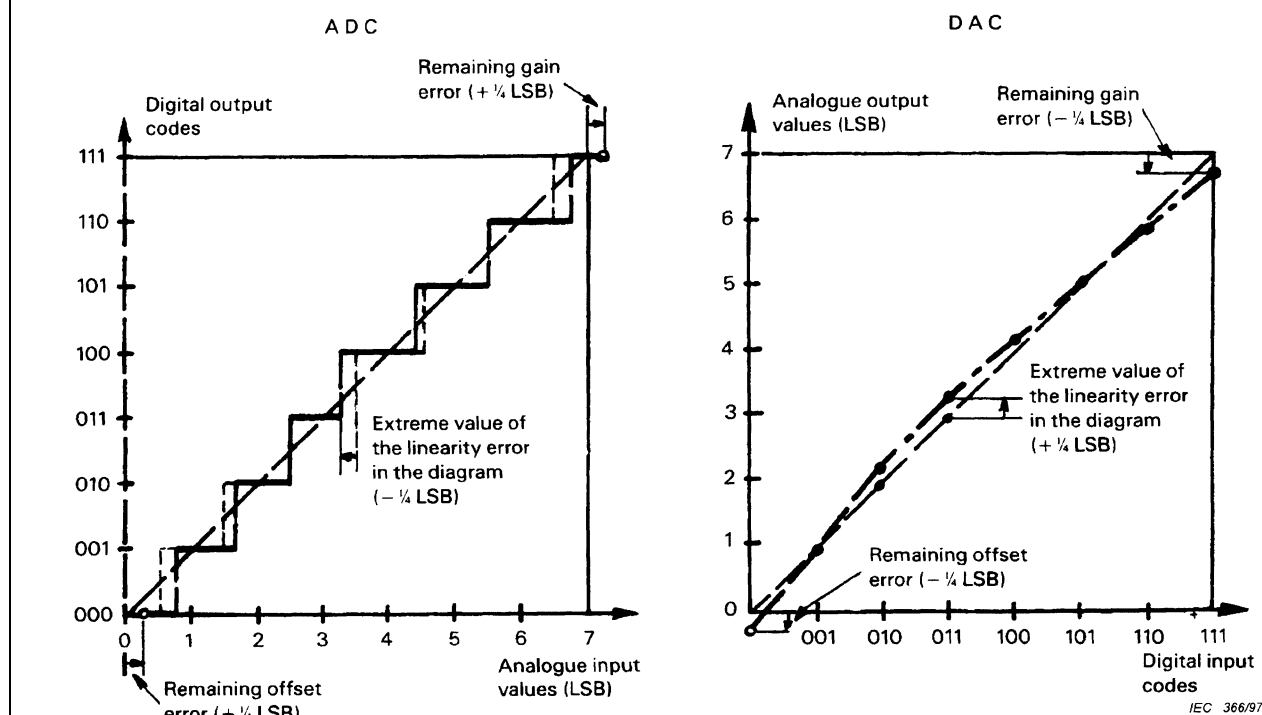
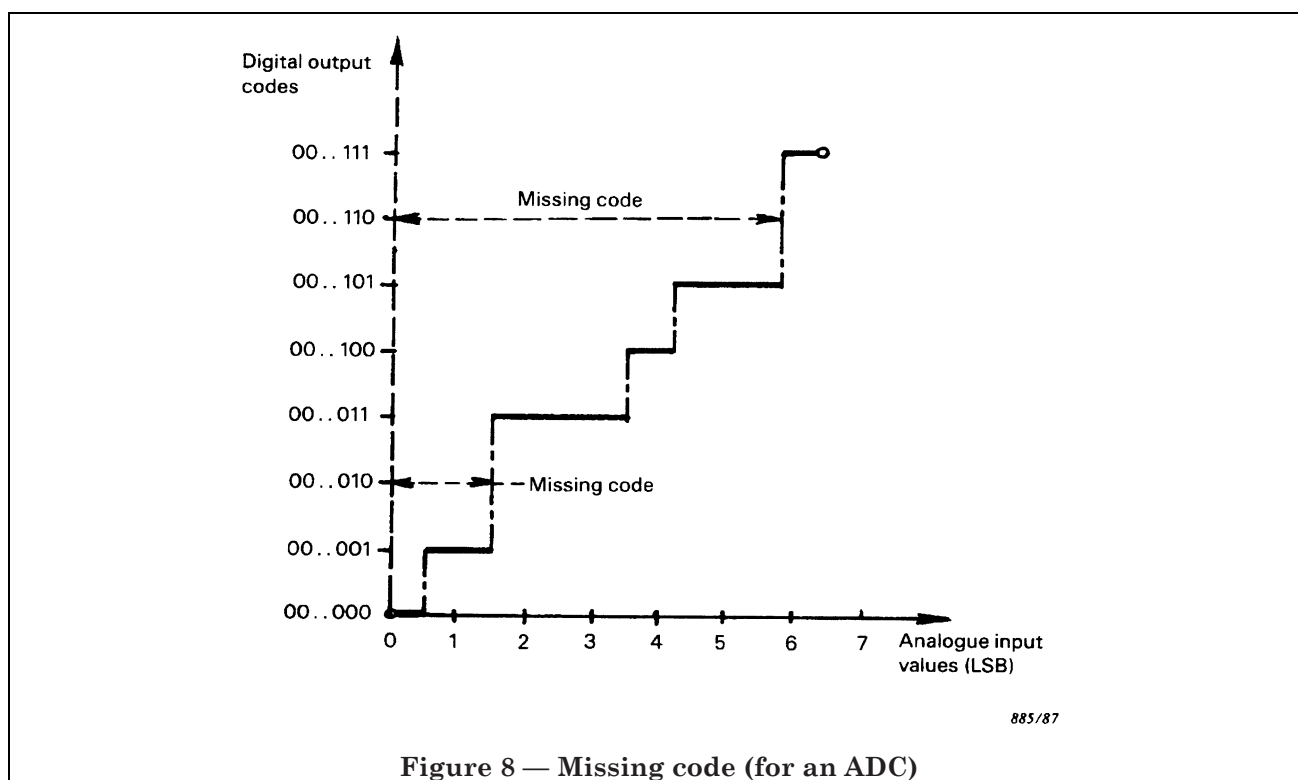
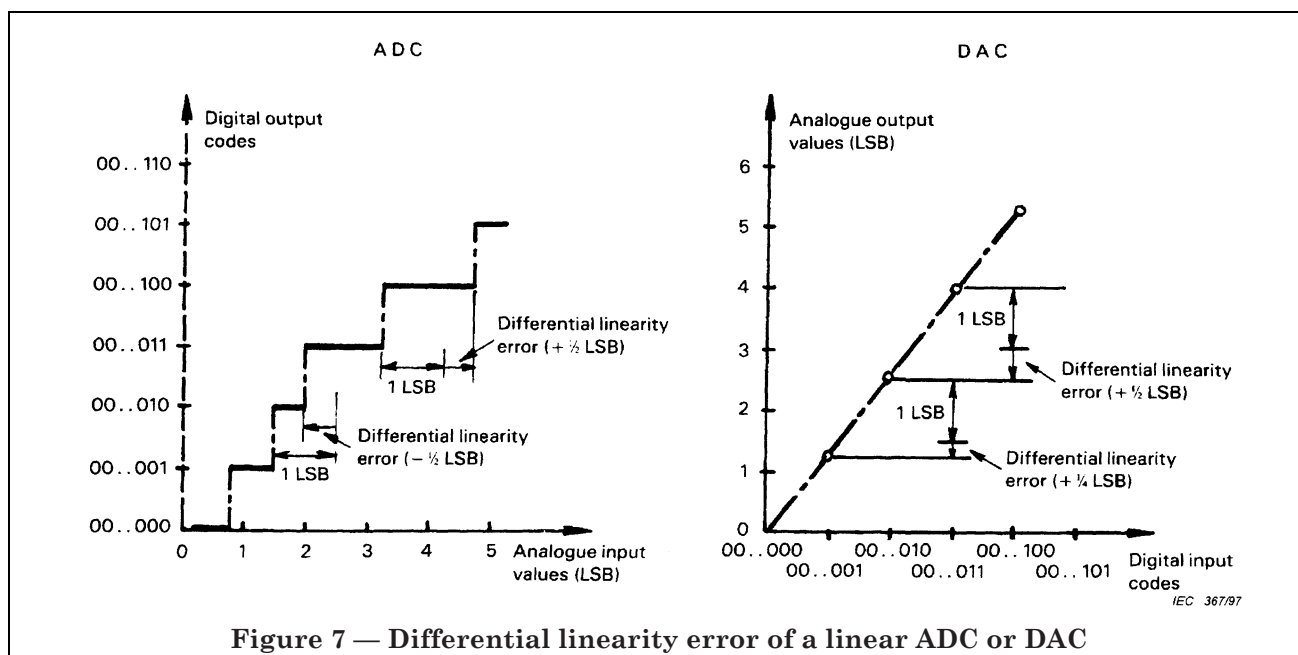
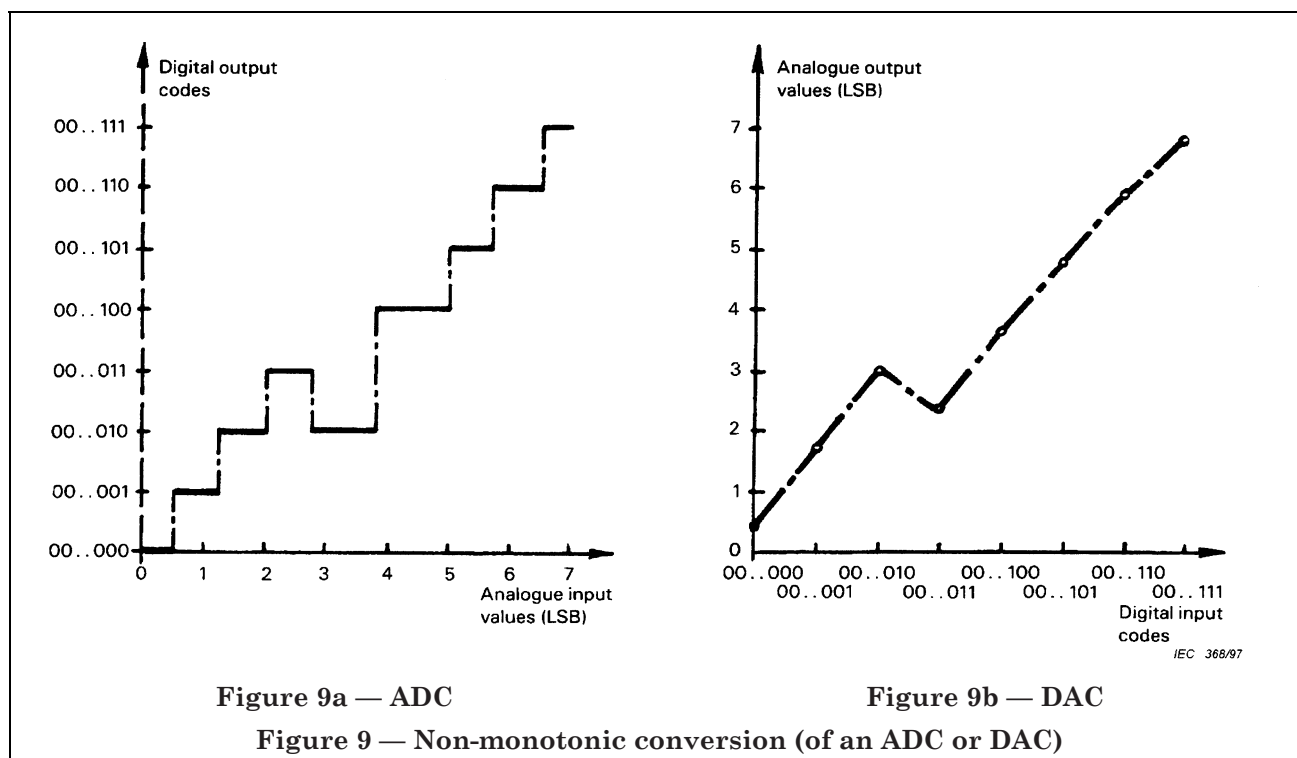


Figure 6b — Best-straight-line linearity error (values between $\pm 1/4$ LSB)
Figure 6 — Linearity errors (of a linear, 3-bit natural binary-coded converter)



**2.2.5.6****missing code** (of an ADC)

an intermediate code that is absent when the changing analogue input to an ADC causes a multiple code change at the digital output (see Figure 8)

2.2.5.7**monotonicity** (of an ADC or a DAC)

a property of the transfer function that ensures that the increase or decrease of the analogue output of a DAC or the digital output of an ADC is consistent with an increase or decrease of the digital or analogue input, respectively

NOTE An intermediate increment or decrement with the value zero does not invalidate monotonicity.

2.2.5.8**full-scale error** (of a linear ADC or DAC) (E_{FS})

the difference between the actual midstep value or step value and the nominal midstep value or step value, respectively, at specified full scales

NOTE Normally, this error specification is applied to converters that have no arrangement for an external adjustment of offset error and gain error.

2.2.5.9**zero-scale error** (of a linear ADC or DAC) (E_{ZS})

the difference between the actual midstep value or step value and the nominal midstep value or step value, respectively, at specified zero scale

NOTE See the note to 2.2.5.8.

2.2.5.10 absolute accuracy error, total error (of a linear ADC or DAC) (E_T)

NOTE If this error is expressed as a relative value, the term “relative accuracy error” will be used instead of “absolute accuracy error”.

2.2.5.10.1**absolute accuracy error, total error** (of a linear ADC)

the maximum difference (positive or negative) between an analogue value and the nominal midstep value, within any step (see Figure 10a)

NOTE This error includes contributions from offset error, gain error, linearity error and the inherent quantization error.

2.2.5.10.2

absolute accuracy error, total error (of a linear DAC)

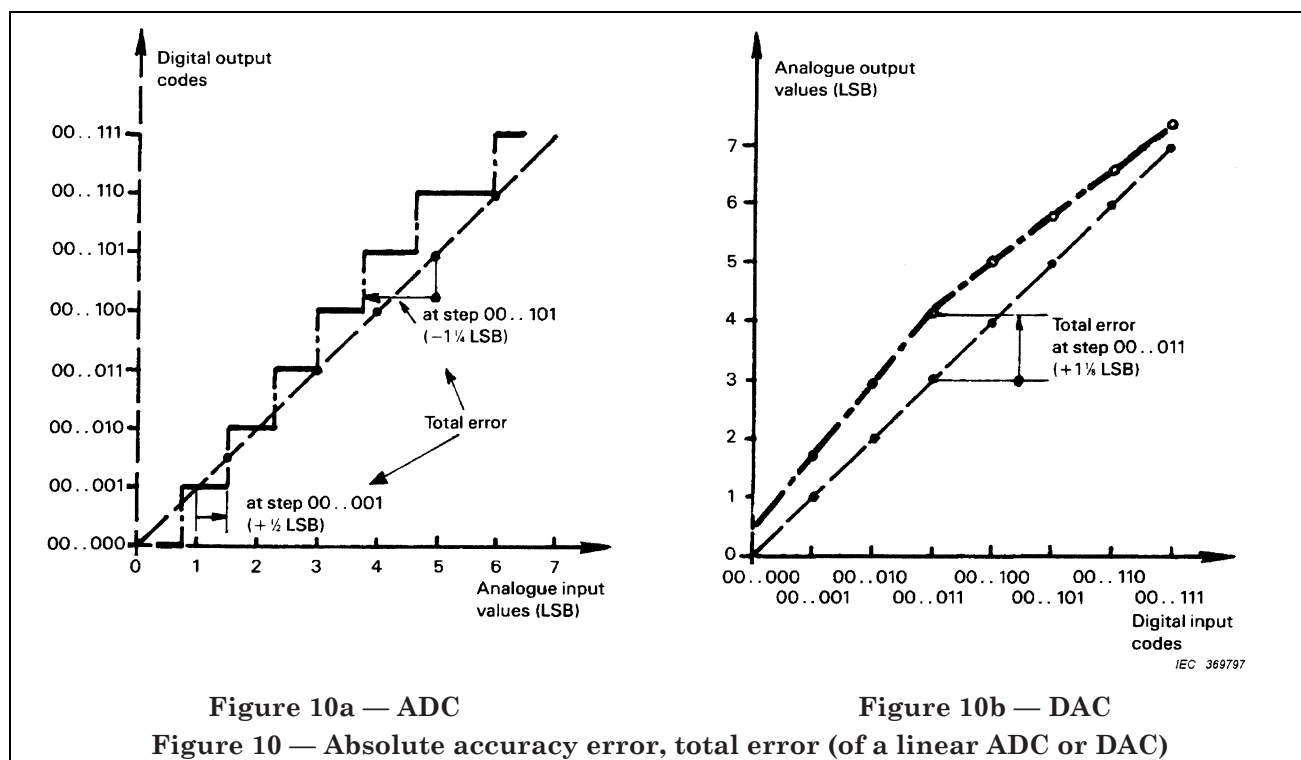
the difference (positive or negative) between the actual step value and the nominal step value, for any step (see Figure 10b)

NOTE This error includes contributions from offset error, gain error and inherent linearity error.

2.2.5.11

roll-over error (of an ADC with decimal output and autopolarity) (E_{R0})

the difference in output reading for a same magnitude of analogue input (close to full-scale), when switched between positive and negative polarity



2.2.6 supply voltage sensitivity of DAC or ADC

2.2.6.1

output current (or output voltage) supply voltage sensitivity of a DAC ($k_{SVS(I)}$, $k_{SVS(V)}$)

the quotient of the change in full-scale of output current (or output voltage) range by the change in supply voltage causing it:

$$k_{SVS(I)} [k_{SVS(V)}] = \frac{\Delta FSR}{\Delta V_{SS}}$$

NOTE 1 Usually, this characteristic is expressed as the ratio of the percent (or ppm) change of the full-scale range to the percent change in supply voltage, that is in %/% (or ppm/%).

NOTE 2 The expression in terms of “power supply rejection ratio”: $PSSR = 20 \log (1/k_{SVS})$ is deprecated.

2.2.6.2

input current (or input voltage) supply voltage sensitivity of an ADC ($k_{SVS(I)}$, $k_{SVS(V)}$)

the quotient of the change in full-scale of input current (or input voltage) range by the change in supply voltage causing it:

$$k_{SVS(I)} [k_{SVS(V)}] = \frac{\Delta FSR}{\Delta V_{SS}}$$

NOTE 1 Usually, this characteristic is expressed as the ratio of the percent (or ppm) change of the full-scale range to the percent change in supply voltage, that is in %/% (or ppm/%).

NOTE 2 The expression in terms of “power supply rejection ratio”: $PSRR = 20 \log (1/k_{SVS})$ is deprecated.

2.2.7**voltage (or current) compliance** (of a DAC) ($\Delta V_{O(op)}$, $\Delta I_{O(op)}$)

for current (or voltage) as the output quantity, the permissible range of output voltage (or current), respectively, within which the specifications are valid

2.2.8**full-scale asymmetry** (of a DAC with complementary analogue outputs) (ΔI_{FSS} , ΔV_{FSS})

the difference in absolute value between the two full-scale analogue outputs

2.2.9**noise** (at the transition of a step of an ADC)

the stochastic change in a series of measurements of the transition value between two adjacent digital output codes

2.2.10**noise** (at the output of a DAC)

the noise at the analogue output at a particular digital input code

2.3 Dynamic performance**2.3.1****conversion time** (of an ADC) (t_c)

the time elapsed between the command to perform a conversion and the appearance at the converter output of the complete digital representation of the analogue input value

NOTE Due to additionally necessary settling and recovery times, the maximum specified conversion rate is smaller than the reciprocal of the worst-case conversion time.

2.3.2**conversion rate** (of an externally-controlled ADC) (f_c)

the number of conversions per unit time

NOTE 1 The maximum conversion rate shall be specified for full resolution.

NOTE 2 The conversion rate is usually expressed as the number of conversions per second.

2.3.3 digital characteristics (of a linear or a multiplying DAC) (see Figure 11)

NOTE For a multiplying DAC:

- these characteristics refer to a change at the digital input, the reference voltage being constant;
- the full terms and the additional subscript d or D must be used, to distinguish between the digital and the reference signal characteristics.

2.3.3.1**(digital) settling time** (t_s , t_{sd})

the time interval between the instant when the digital input changes and the instant when the analogue output value enters for last time a specified error band about its final value

2.3.3.2**(digital) delay time** (t_d , t_{dd})

the time interval between the instant when the digital input changes and the instant at which the magnitude of the analogue output passes a specified value that is close to its initial value

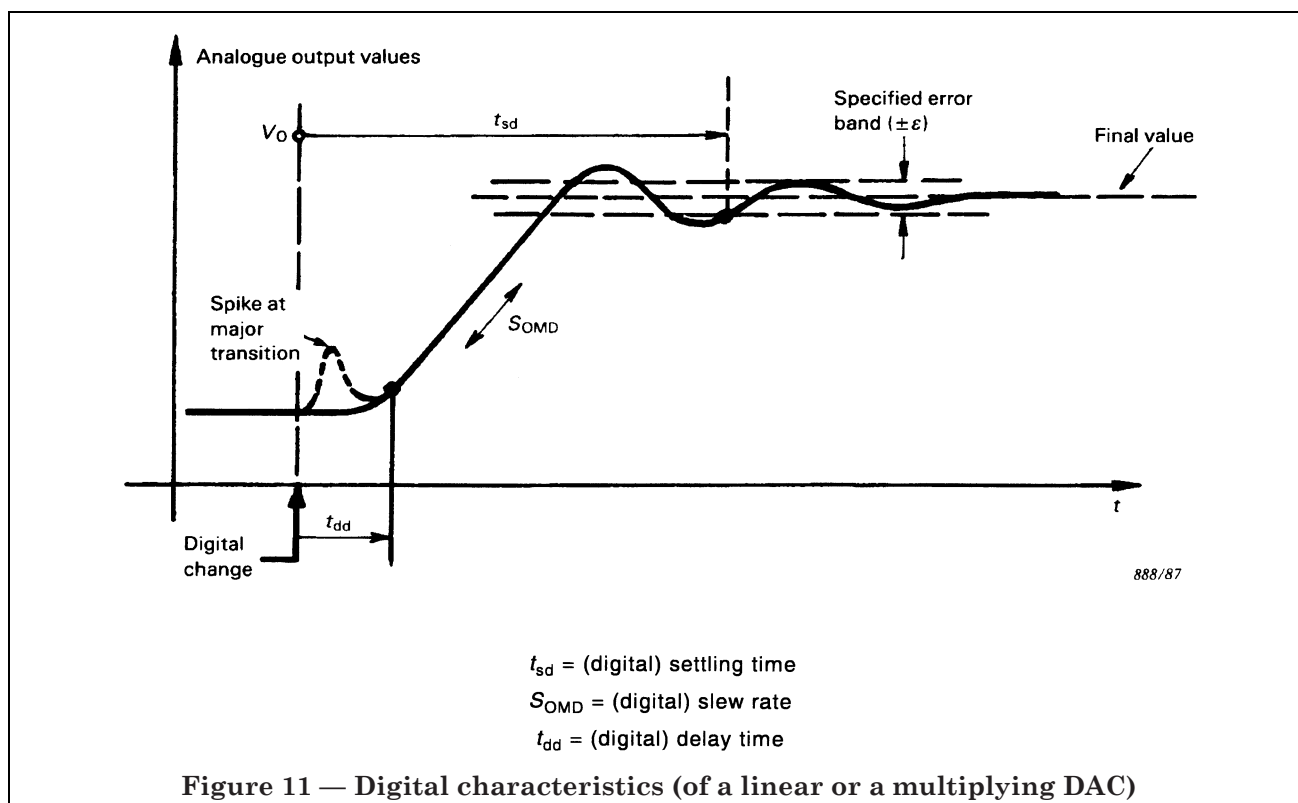
2.3.3.3**(digital) slew rate, maximum rate of (digital) change of the output** (S_{OM} , S_{OMD})

the inherently limited rate of change of the analogue output value when a change of the digital input code causes a large step change of the analogue output value

NOTE The abbreviations “SR, SR(dig)” are also used.

2.3.3.4**(digital) average rate of change of the output voltage** (S_{VOAVd})

for a change of the digital input code, the quotient of a specified large change of the analogue output voltage, by the time interval corresponding to that analogue output voltage change



2.3.4 analogue characteristics (of a DAC)

2.3.4.1

glitch

a short transient in the analogue output occurring following code changes at the digital input

2.3.4.2

glitch area

the time integral of the analogue value of the glitch transient

NOTE 1 Usually, the maximum specified glitch area refers to a specified worst-case code change.

NOTE 2 Instead of a letter symbol, the abbreviation "GA" is in use.

2.3.4.3

glitch energy

the time integral of the electrical power of the glitch transient

NOTE 1 Usually, the maximum specified glitch energy refers to a specified worst-case code change.

NOTE 2 Instead of a letter symbol, the abbreviation "GE" is in use.

2.3.4.4

internal skewing time

the difference in interval delay between the individual output transitions for a given change of digital input

NOTE The internal (and external) skew has a major influence on the settling time for critical changes in the digital input, for example, for a 1-LSB change from 011...111 to 100...000, and is an important source of commutation noise.

2.3.5 reference signal characteristics (of a multiplying DAC)

NOTE These characteristics refer to a change of the reference voltage, the digital input being constant.

2.3.5.1

reference settling time (t_{sr})

the time interval between the instant when a step change of the reference voltage occurs and the instant when the analogue output enters for the last time a specified error band about its final value (see Figure 12a)

NOTE Specifications for the reference settling time shall be given for the highest allowed step change in reference voltage.

2.3.5.2**reference delay time (t_{dr})**

the time interval between the instant when a step change of the reference voltage occurs and the instant when the magnitude of the analogue output passes a specified value that is close to its initial value (see Figure 12a)

2.3.5.3**reference slew rate (S_{OMR})**

the inherently limited rate of change of the analogue output voltage following a large step change of the reference voltage (see Figure 12a)

NOTE The abbreviation “SR(ref)” is also used.

2.3.5.4**(reference) average rate of change of the output voltage (S_{VOAVr})**

for a change of reference voltage by the time interval corresponding to that analogue output voltage change

2.3.5.5**steady-state ramp delay ($t_{d(ramp)}$)**

the time separation between the actual curve of the analogue output and the theoretical curve for a ramp in reference voltage, after the settling time to steady-state ramp has elapsed (see Figure 12b)

2.3.5.6**settling time to steady-state ramp ($t_{s(ramp)}$)**

the time interval between the instant when a ramp in reference voltage starts and the instant when the analogue output value enters for the last time a specified error band about the finally resulting output ramp (see Figure 12b)

2.3.5.7**feedthrough error (E_F)**

an error in analogue output due to variation in the reference voltage that appears as an offset error and is proportional to the frequency and amplitude of the reference signal

NOTE 1 The specification for the feedthrough error is given for the digital input for which the offset error is specified, and for a reference signal of specified frequency and amplitude.

NOTE 2 This error may also be expressed as a peak-to-peak analogue value.

2.3.5.8**feedthrough capacitance (C_F)**

the value of the capacitance for a specified value of R in an equivalent circuit for the calculation of the feedthrough effect

NOTE The equivalent circuit consists of a high-pass RC filter between reference input and analogue output.

2.4 Sundry characteristics**2.4.1****temperature coefficients of analogue characteristics (α)**

NOTE 1 The letter symbol for the temperature coefficient of an analogue characteristic consists of the letter symbol α with a subscript referring to the relevant characteristic.

Example: Temperature coefficient of the gain error: α_{EG} .

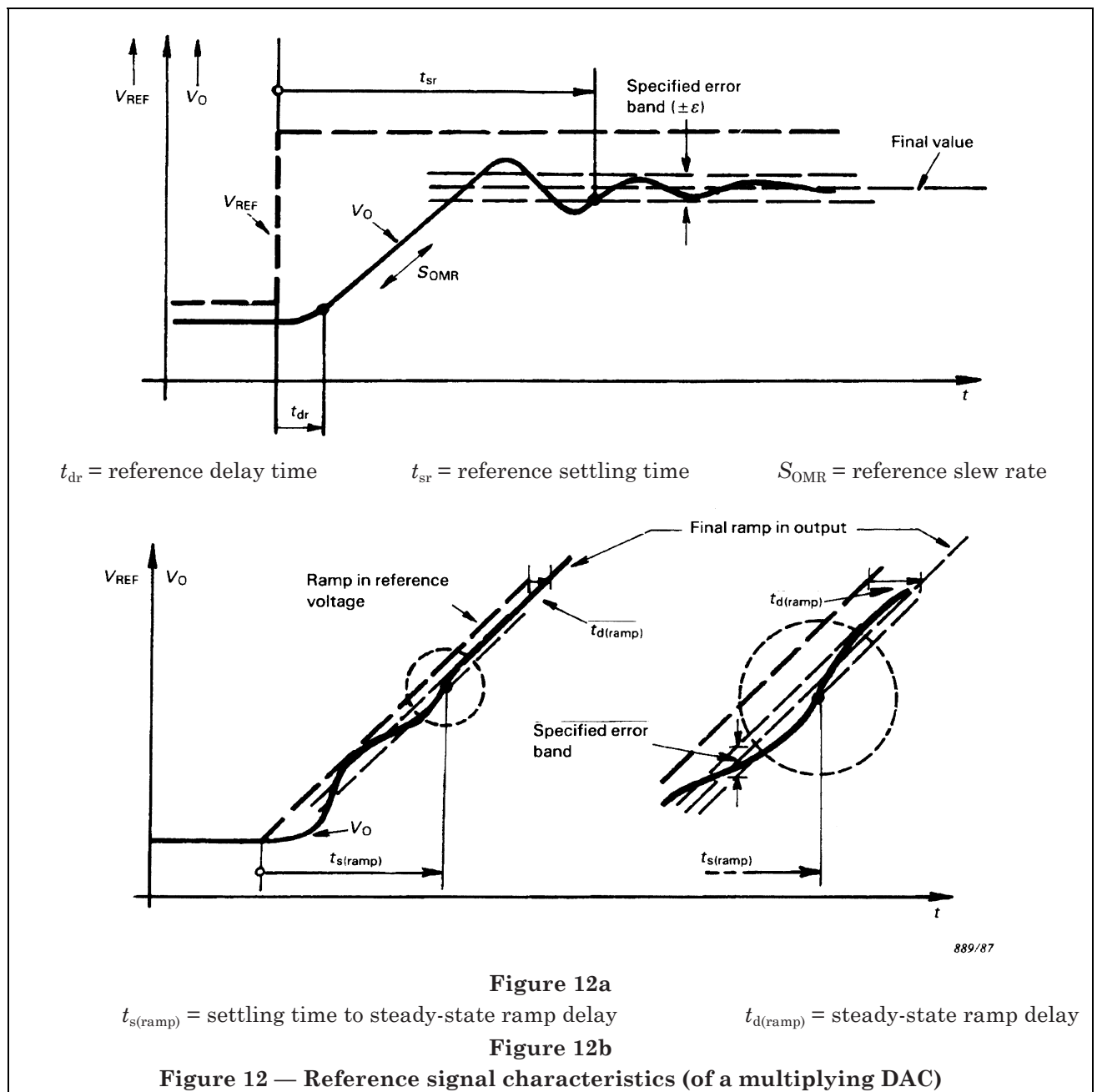
NOTE 2 Temperature coefficients are usually specified in “parts per million (relative to the full-scale value) per degree Celsius, that is in “ppm/°C”.

2.4.2**accuracy long-term instability ($\Delta E_{(\Delta t)}$, $\Delta E_{(t)}$)**

the additional error caused by the ageing of the components and specified for a longer period in time

2.4.3**pedestal (E_p)**

a dynamic offset error produced in the commutation process



3 Letter symbols

3.1 General

3.1.1 Basic letters

Chapter V, clause 1 of IEC 60748-1 (which refers back to chapter V, clauses 2, 3 and 4 of IEC 60747-1) applies.

3.1.2 Subscripts

Chapter V of IEC 60748-1 applies.

3.2 Letter symbols of category I (line circuits, sense amplifiers, peripheral drivers and level shifters, voltage comparators).

Name and designation	Letter symbol	Remarks and current abbreviations
3.2.1 Terms related to input characteristics		
Input impedance	Z_i	
High-level input voltage	V_{IH}	
Low-level input voltage	V_{IL}	
High-level input current	I_{IH}	
Low-level input current	I_{IL}	
Input offset voltage	V_{IO}	
Input offset current	I_{IO}	
High-level input threshold voltage	V_{ITH}	
Low-level input threshold voltage	V_{ITL}	
Mean temperature coefficient of the input offset voltage	αV_{IO}	
Mean temperature coefficient of the input offset current	αI_{IO}	
Overall input threshold voltage range	ΔV_{ITR}	
Differential input voltage	V_{ID}	
Differential input threshold voltage	V_{IDT}	
Average (mean) bias current	I_{IB}	
Common-mode input voltage	V_{IC}	
Common-mode input triggering voltage	V_{ICT}	
Common-mode rejection ratio	k_{CMR}	The abbreviations CMRR and CMR are in common use for the quantity
Input (output) clamping voltage	$V_{IK}; V_{OK}$	
Supply voltage rejection ratio	k_{SVR}	The abbreviations SVRR, SVR and PSRR are in common use for the quantity
3.2.2 Terms related to output characteristics		
High-level output voltage	V_{OH}	
Low-level output voltage	V_{OL}	
High-level output current	I_{OH}	
Low-level output current	I_{OL}	
Short-circuit output current	I_{OS}	
Off-state (high-impedance state) output current	$I_{O(off)}; I_{OZ}$	
Output change overvoltage for a comparator	V_{OO}	

Name and designation	Letter symbol	Remarks and current abbreviations
3.2.3 Terms related to transfer characteristics		
Differential-mode voltage amplification	$A_{VD}; A_{vd}; A_V$	
Delay time	t_d	
Rise time, fall time	$t_r; t_f$	
Total response time	t_{tot}	
High-level to low-level propagation time	t_{PHL}	
Low-level to high-level propagation time	t_{PLH}	
High-level to low-level transition time	t_{THL}	
Low-level to high-level transition time	t_{TLH}	
Differential-input overload recovery time	t_{ord}	
Common-mode input overload recovery time	t_{orc}	

3.3 Letter symbols for category II (linear and non-linear analogue-to-digital and digital-to-analogue converters)

Name and designation	Letter symbol	Remarks and current abbreviations
3.3.1 General terms		
(Practical) full-scale range	$V_{FSR}; I_{FSR}$ $V_{FSRpr}; I_{FSRpr}$	FSR and FSR(pr)
Nominal full-scale range	$V_{FSRnom}; I_{FSRnom}$	FSR(nom)
Full scale	$V_{FS}; I_{FS}$	FS
Positive full scale	$V_{FS+}; I_{FS+}$	FS+
Negative full scale	$V_{FS-}; I_{FS-}$	FS-
Zero scale	$V_{ZS}; I_{ZS}$	ZS
Positive zero scale	$V_{ZS+}; I_{ZS+}$	ZS+
Negative zero scale	$V_{ZS-}; I_{ZS-}$	ZS-
Nominal full-scale value	$V_{FSnom}; I_{FSnom}$	FS(nom)
3.3.2 Terms related to static performance		
Least significant bit		LSB
Offset error	E_O	
Gain error	E_G	
(End-points) linearity error	E_L	
Best straight-line linearity error	$E_{L(adj)}$	

Name and designation	Letter symbol	Remarks and current abbreviations
Differential linearity error	E_D	
Full-scale error	E_{FS}	
Zero-scale error	E_{ZS}	
Absolute accuracy error, total error	E_T	
Roll-over error	E_{RO}	
Output current (or output voltage) supply voltage sensitivity	$k_{SVS(I)}$ $k_{SVS(V)}$	
Voltage or current compliance	$\Delta V_{O(op)}$ or $\Delta I_{O(op)}$	
Transition value	V_{tr} , I_{tr}	
Gain	G	
3.3.3 Terms related to dynamic performance		
Conversion time	t_c	
Conversion rate	f_c	
(Digital) settling time	t_s ; t_{sd}	
(Digital) delay time	t_d ; t_{dd}	
(Digital) slew rate, maximum rate of (digital) change of the output	S_{OM} ; S_{OMD}	SR; SR(dig)
(Digital) average rate of change of the output voltage	S_{VOAVd}	
Glitch area		GA
Glitch energy		GE
Reference settling time	t_{sr}	
Reference delay time	t_{dr}	
Reference slew rate	S_{OMR}	SR(ref)
(Reference) average rate of change of the output voltage	S_{VOAVr}	
Steady-state ramp delay	$t_{d(ramp)}$	
Settling time to steady-state ramp	$t_{s(ramp)}$	
Feedthrough error	E_F	
Feedthrough capacitance	C_F	
3.3.4 Sundry characteristics		
Temperature coefficients of analogue characteristics	α	
Temperature coefficient of the gain error	α_{EG}	
Accuracy long-term instability	$\Delta_{E(\Delta t)}$; $\Delta_{E(t)}$	
Pedestal	E_p	
Noise	under consideration	

Chapter III. Essential ratings and characteristics

Section 1. Category I

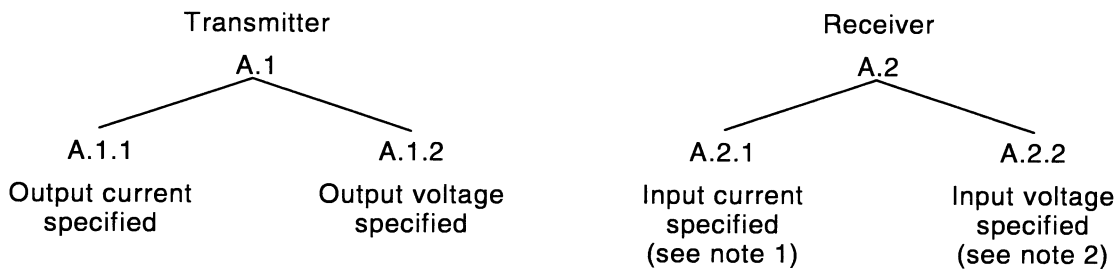
(Line circuits, sense amplifiers, peripheral drivers and level shifters, voltage comparators)

1 General

1.1 This section gives ratings and characteristics that are required to specify certain types of interface circuits in any of the following subcategories (for definitions, see chapter II):

— Subcategory A — Line circuits

This subcategory can be subdivided as follows:



NOTE 1 For example, where input impedance is lower than source impedance.

NOTE 2 For example, where input impedance is higher than source impedance.

— Subcategory B — Sense amplifiers

— Subcategory C — Peripheral drivers (including memory drivers and level shifters)

— Subcategory D — Voltage comparators

1.2 This section includes circuits that are completely integrated or that consist of combinations of integrated circuits and discrete devices (for example, transistors) that, while within one package, can be accessed separately via available terminations.

In the latter case, the transistor(s) or other discrete devices shall be specified separately according to the relevant standards of IEC 60747.

2 Functional specifications

2.1 Block diagram

A block diagram or equivalent circuit information of the interface integrated circuit shall be given.

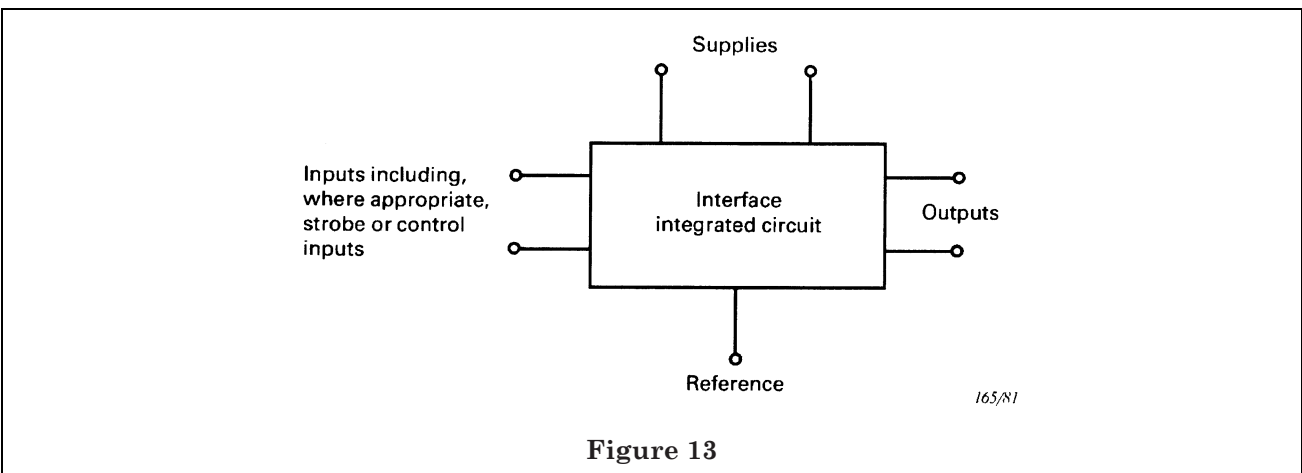


Figure 13

The following terminals may be distinguished:

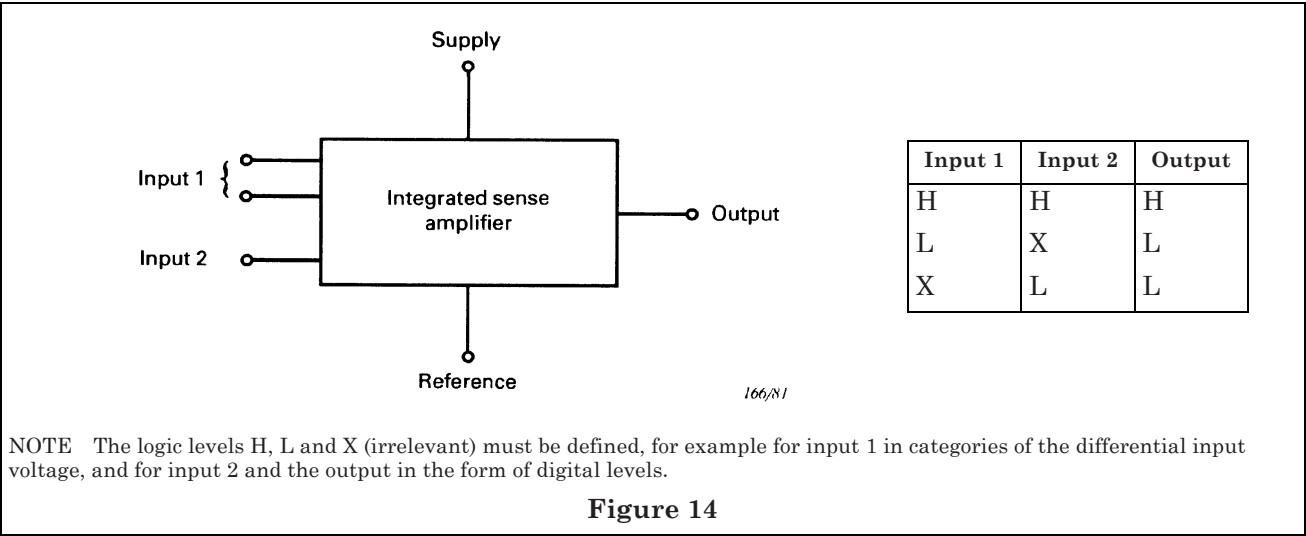
— supply terminals, that is, terminals intended to be connected to the power supplies;

— input and output terminals, that is, terminals into or out of which signals are passed.

The term “signal” includes both pulse and more complex waveforms, and includes strobe or control pulses.

2.2 Function

The function performed by the circuit shall be specified, for example, in the form of a function table.
Example: A function table of an integrated sense amplifier circuit.



2.3 Electrical compatibility

It shall be stated whether the device is compatible, with respect to electrical characteristics, with other devices or families of devices.

3 Description of the circuit

3.1 Technology

The manufacturing technology shall be stated, for example, semiconductor monolithic integrated circuit, hybrid integrated circuit, micro-assembly, etc.

3.2 Details of outline and encapsulation

3.2.1 IEC and/or national reference number of the outline drawing

3.2.2 Method of encapsulation

4 Ratings (limiting values)

In satisfying the following clauses, if maximum and/or minimum values are quoted, the manufacturer must indicate whether he refers to the absolute magnitude or to the algebraic value of the quantity.

The ratings given must cover the operation of the integrated circuit over the specified range of operating temperatures. Where such ratings are temperature dependent, this dependence should be indicated.

4.1 Electrical limiting values

4.1.1 Power supply voltage(s)

- a) Maximum value(s) and polarities.
- b) Maximum permissible ripple on the supply voltage(s) (where appropriate).
- c) Maximum values of transient or spurious signals from the supplies for a specified time duration (where appropriate).
- d) Maximum value of the voltage between any supply terminal and the case or reference terminal.
- e) The sequence of the application of supply voltages (where appropriate).

4.1.2 Power supply current(s)

- a) Maximum values (where appropriate).
- b) Maximum values for a specified time duration (external fault conditions) (where appropriate).

4.1.3 Input voltages

- a) Maximum values with respect to the reference terminal (and polarities, if appropriate).
- b) Maximum value between input terminals (where appropriate).
- c) Maximum value of two connected inputs with respect to the reference terminal (where appropriate).

4.1.4 Output voltages

- a) Maximum values with respect to the reference terminal.
- b) Maximum value between output terminals (where appropriate).
- c) Maximum value of two connected outputs with respect to the reference terminal (where appropriate).

4.1.5 Input currents (where appropriate)

Maximum values.

4.1.6 Output currents

- a) Maximum values.
- b) Maximum values of transient currents for a specified time duration (where appropriate).

4.1.7 Impedances (where appropriate)

Minimum value of load impedance.

4.1.8 Short-circuit duration (between terminals, or between a terminal and the reference terminal)

Maximum value (where appropriate).

4.1.9 Interterminal voltage (where appropriate)

Maximum value(s).

4.2 Temperatures**4.2.1 Operating temperatures**

Minimum and maximum values of ambient or reference-point operating temperatures.

4.2.2 Storage temperatures

Minimum and maximum values.

4.2.3 Lead temperatures

Maximum value of lead temperature and maximum duration for which it may be applied.

4.3 Power dissipation (where appropriate)

- a) Maximum total power dissipation as a function of temperature over the operating temperature range (ambient or reference-point).
- b) Where several integrated circuits or elements are encapsulated within a single package, the maximum power dissipation shall also be stated for each circuit or element independently.

5 Recommended operating conditions [within the specified operating temperature range and specified supply voltage(s)]

For all the subclauses included in this clause, the variation with temperature shall be stated (where appropriate).

5.1 Power supplies

5.1.1 Polarity, nominal values and tolerances for voltages provided by the power supplies

5.1.2 Polarity, nominal values and tolerances for currents provided by the power supplies (where appropriate)

5.1.3 Maximum value(s) of the impedance(s) of the power supplies (where appropriate)

5.2 Input terminals

Recommended values of the voltage(s) and/or current(s) of the input signal and (where appropriate) of the signal source impedance, and/or bias conditions applied to the input terminals.

5.3 Output terminals

Nominal value(s) of the voltage(s) and/or current(s) of the output signal, and recommended value of the load impedance.

(Where appropriate) bias conditions applied to the output terminal(s).

5.4 External elements (where appropriate)

Value(s) and tolerance(s) for the external element(s) that must be associated with the circuit.

5.5 Operating temperature range

Recommended ambient or reference-point temperature range.

6 Electrical characteristics

NOTE The characteristics to be specified for each subcategory are indicated in the relevant column by a “+” sign. The sign “+” indicates that a specification must be given only where appropriate.

6.1 Characteristics at 25 °C (ambient or reference-point temperature)

6.1.1 Supply current(s)

Maximum value(s) for specified values of:

- supply voltage(s);
- load conditions (where appropriate);
- dynamic conditions, for example: operating frequency, duty cycle (where appropriate);
- input voltage.

6.1.2 Input characteristics

6.1.2.1 Input impedance (Z_i)

Minimum value for specified values of:

- supply voltage(s);
- output voltage or current (as appropriate);
- load impedance (where appropriate);
- input signal amplitude;
- frequency.

6.1.2.2 High-level input voltage(s) (V_{IH})

Least positive (most negative) value for specified values of:

- supply voltage(s);
- other input voltages (where appropriate);
- load impedance (where appropriate).

6.1.2.3 Low-level input voltage(s) (V_{IL})

Most positive (least negative) value for specified values of:

- supply voltage(s);
- other input voltages (where appropriate);
- load impedance (where appropriate).

6.1.2.4 High-level input current(s) (I_{IH})

Maximum value(s) for specified values of:

- supply voltage(s);
- input voltage(s);
- load impedance (where appropriate);
- other input voltages (where appropriate).

Subcategory						
A				B	C	D
1.1	1.2	2.1	2.2			
+	+	+	+	+	+	+
		+	+			
+	+		+	+ ^a	+	
+	+		+	+ ^a	+	
+	+	+	+	+ ^a	+	

6.1.2.5 Low-level input current(s) (I_{IL})

Maximum value(s) for specified values of:

- supply voltage(s);
- input voltage(s);
- load impedance (where appropriate);
- other input voltages (where appropriate).

6.1.2.6 Input offset voltage (V_{IO})

Maximum value for specified values of:

- supply voltage(s);
- output voltage or current (as appropriate);
- source resistance (where appropriate);
- common-mode input voltage (where appropriate).

6.1.2.7 Input offset current (I_{IO})

Maximum value for specified values of:

- supply voltage(s);
- output voltage or current (as appropriate);
- common-mode input voltage (where appropriate);
- differential input voltage (where appropriate).

6.1.2.8 Differential-input voltage range (V_{ID})

Minimum value for specified values of:

- supply voltage(s);
- load impedance (where appropriate);
- output voltage or current (as appropriate);
- reference voltage (where appropriate).

6.1.2.9 Overall input threshold voltage range (ΔV_{ITR})

Minimum and/or maximum value(s) for specified values of:

- supply voltage(s);
- source resistance (where appropriate);
- common-mode input voltage (where appropriate);
- other input voltage(s) (where appropriate);
- reference voltage (where appropriate);
- load impedance (where appropriate);
- output voltage or current (as appropriate);
- logic levels of output voltage (as appropriate).

NOTE Separate pairs of values may need to be given for each direction of transition at the output.

6.1.2.10 Average bias current (I_{IB})

Maximum value for specified values of:

- supply voltage(s);
- common-mode input voltage (where appropriate);
- differential input voltage (where appropriate).

6.1.2.11 Common-mode input voltages

Whichever is appropriate:

- a) Common-mode input voltage range (V_{IC}), or
- b) Common-mode input triggering voltage (V_{ICT}).

Subcategory						
A				B	C	D
1.1	1.2	2.1	2.2			
+	+	+	+	+ ^a	+	
			(+)	(+)		+
		(+)		(+)		+
			+ ^b	+		+
			+ ^b	+		+
		+ ^b	+ ^b	+		+
		+ ^b	+ ^b	+		+

Minimum value for specified values of:

- supply voltage(s);
- output voltage or current (as appropriate);
- input pulse conditions (including driving networks);
- differential input voltage.

6.1.2.12 Common-mode rejection ratio (K_{CMR})

Minimum value for specified values of:

- supply voltage(s);
- common-mode input signal amplitude;
- output voltage or current (as appropriate);
- strobe voltage (where appropriate);
- load and source impedances;
- frequency (where appropriate).

6.1.2.13 Input clamping voltage (V_{IK})

Maximum value for specified values of:

- supply voltage(s);
- input current.

6.1.2.14 Supply voltage rejection ratio (K_{SVR})

Minimum value for specified values of:

- supply voltage(s);
- change in supply voltage;
- output voltage or current as specified for offset voltage;
- load impedance (where appropriate).

6.1.3 Output characteristics

6.1.3.1 High-level output voltage (V_{OH})

Least positive (most negative) value for specified values of:

- supply voltage(s);
- load current or resistance;
- input voltage(s);
- strobe voltage (where appropriate).

6.1.3.2 Low-level output voltage (V_{OL})

Most positive (least negative) value for specified values of:

- supply voltage(s);
- load current or resistance;
- input voltage(s);
- strobe voltage (where appropriate).

6.1.3.3 Output current (I_o)

Minimum and/or maximum value for specified values of:

- supply voltage(s);
- input voltage;
- output voltage.

NOTE For digital outputs, values shall be given for both the high-level and low-level output currents (I_{OH} , I_{OL})

Subcategory						
A				B	C	D
1.1	1.2	2.1	2.2			
		bc (+)	bc (+)			+
(+)	(+)				(+)	
			b (+)	(+)		+
	+	+	+	+	+	+
	+	+	+	+	+	+
+						

6.1.3.4 Short-circuit output current (I_{OS})

Maximum value for specified values of:

- supply voltage(s);
- input voltage;
- strobe voltage (where appropriate);
- duration of the short-circuit.

6.1.3.5 Off-state (high-impedance-state) output current ($I_{O(off)}$, I_{OZ})

Maximum value for specified values of:

- supply voltage(s);
- output voltage.

NOTE This characteristic is only applicable for open-collector or open-emitter output devices or three-state devices in the off-state.

6.1.4 Transfer characteristics**6.1.4.1 Differential-mode voltage amplification (A_{vd})**

Minimum value for specified values of:

- supply voltage(s);
- amplitude of the output signal in differential mode;
- load and source impedances.

NOTE 1 (for subcategory A.2). This characteristic is applicable only if the transfer characteristic is linear over a substantial part of its range.

NOTE 2 The specified values shall be such that linear part of the transfer curve is used.

6.1.4.2 Response times

Maximum values for specified values of:

- supply voltage(s);
- input pulse conditions;
- source impedance and load resistance and capacitance or inductance;
- strobe voltage (where appropriate);
- a) for a low-to-high transition at the output;
- b) for a high-to-low transition at the output.

NOTE 1 For analogue-input, digital-output devices, the response times [delay time (t_d), slope time (t_r , t_f), and total response time (t_{tot})] shall be stated as required for analogue-input, analogue-output devices by chapter III, section 2, subclause 5.1.4.3 of IEC 60748-3.

NOTE 2 For digital-input, digital-output devices, the propagation and transition times shall be stated as required by chapter III, section 1, subclause 7.2 of IEC 60748-2.

6.1.4.3 Strobe propagation time

Maximum values for specified values of:

- supply voltage(s);
- voltages on the input terminals;
- source impedance and load resistance and capacitance or inductance;
- strobe input pulse conditions;
- a) for a low-to-high transition at the strobe input;
- b) for a high-to-low transition at the strobe input.

	Subcategory						
	A				B	C	D
	1.1	1.2	2.1	2.2			
e		+	+	+	+	+	+
	+	+	+	+	+	+	+
			+ ^b	+ ^b			+
	+	+	+	+	+	+	+
r							
y							
	+	+	+	+	+	+	+
	+	+	+	+	+	+ ^a	+
d							
f							

^c This characteristic is applicable only if the transfer characteristic is linear over a substantial part of its range.

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