

Implementation of
IEC 796-1:1990

Microprocessor system bus — 8-bit and 16-bit Data (MULTIBUS I) —

Part 1: Functional description with
electrical and timing specifications

Committees responsible for this British Standard

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National foreword

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Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, the IEC title page, pages ii to vi, pages 1 to 37 and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

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INTERNATIONALE
INTERNATIONAL
STANDARD**

**CEI
IEC
796-1**

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**Bus système à microprocesseurs -
Données: 8 bits et 16 bits (MULTIBUS I)**

Première partie:

Description fonctionnelle avec spécifications
électriques et chronologiques

**Microprocessor system bus -
8-bit and 16-bit data (MULTIBUS I)**

Part 1:

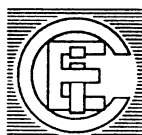
Functional description with electrical
and timing specifications

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Foreword

- 1) The formal decisions or agreements of the IEC on technical matters, prepared by Technical Committees on which all the National Committees having a special interest therein are represented, express, as nearly as possible, an international consensus of opinion on the subjects dealt with.
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Preface

This standard has been prepared by Sub-Committee 47B¹⁾: Microprocessor Systems, of IEC Technical Committee No. 47: Semiconductor Devices.

This standard forms Part 1 of a series of publications, the other parts being:

- Publication 796-2:1990: *Microprocessor system bus — 8-bit and 16-bit data (MULTIBUS I) — Part 2: Mechanical and pin descriptions for the system bus configuration, with edge connectors (direct).*
- Publication 796-3:1990: *Part 3: Mechanical and pin descriptions for the Eurocard configuration with pin and socket (indirect) connectors.*

The text of this standard is based upon the following documents:

Six Months' Rule	Report on Voting
47B(C0)8	47B(C0)14

Full information on the voting for the approval of this standard can be found in the Voting Report indicated in the above table.

The following IEC publication is quoted in this standard:

- Publication No. 625-1:1979: *An interface system for programmable measuring instruments (byte serial, bit parallel), Part 1: Functional specifications, electrical specifications, mechanical specifications, system applications and requirements for the designer and user.*

¹⁾ IEC Sub-Committee 47B has now been transferred to ISO/IEC JTC 1.

This standard was approved according to IEC procedures and is therefore published as an IEC standard.

Introduction

This standard is one of a series which deals with the electrical and mechanical interfaces to allow various microprocessor system components to interact with each other. The interface bus serves as a parallel transfer and utility signal interconnect for closely coupled system components. The series consists of one functional description and two alternative mechanical standards.

Section 1. General

1.1 Scope

This standard is applicable to interface system components, for use in interconnecting data processing, data storage, and peripheral control devices in a closely coupled configuration. This interface system contains the necessary signals to allow the various system components to interact with each other. It allows memory and Input/Output (I/O) data transfers, direct memory accesses, generation of interrupts, etc. This standard provides a detailed description of all the elements and features that make up the system bus.

The bus supports two independent address spaces: memory and I/O. During memory cycles the bus allows direct addressability of up to 16 megabytes using 24-bit addressing. During I/O bus cycles, the bus allows addressing of up to 64K I/O ports using 16-bit addressing. Both memory and I/O cycles can support 8-bit data transfers.

The bus structure is built upon the master-slave concept where the master device in the system takes control of the bus and the slave device, upon decoding its address, acts upon the command provided by the master. This handshake (master-slave relationship) between the master and slave devices allows modules of different speeds to be interfaced via the bus. It also allows data rates up to five million transfers per second (bytes or words) to take place across the bus.

Another important feature of the bus is the ability to connect multiple master modules for multiprocessing configurations. The bus provides control signals for connecting multiple masters in either a serial or parallel priority fashion. With either of these two arrangements, more than one master may share bus resources.

This standard has been prepared for those users who intend to evaluate or design products that will be compatible with the system bus structure. To this end, the necessary signal definitions and timing and electrical specifications have been covered in detail.

This standard deals only with the interface characteristics of microcomputer devices and not with design specifications, performance requirements, and safety requirements of modules.

Throughout this standard, the term “system” denotes the byte or word interface system that, in general, includes all the circuits, connectors, and control protocol to effect unambiguous data transfer between devices. The term “device” or “module” denotes any product connected to the interface system that communicates information via the bus, and that conforms to the interface system definition.

1.2 Object

This standard is intended to:

- 1) define a general purpose microcomputer system bus;
- 2) specify the device-independent electrical and functional interface requirements that a module shall meet in order to interconnect and communicate unambiguously via the bus system;
- 3) specify the terminology and definitions related to the system;
- 4) enable the interconnection of independently manufactured devices into a single functional system;
- 5) permit products with a wide range of capabilities to be interconnected to the system simultaneously;
- 6) define a system with a minimum of restrictions on the performance characteristics of devices connected to the system.

1.3 Definitions

The following general definitions apply for the purpose of this standard. More detailed definitions can be found in the relevant sub-clause.

1.3.1 General System Terms

1.3.1.1

compatibility (IEC Publication 625-1)

the degree to which devices may be interconnected and used, without modification, when designed as defined throughout this standard (e.g. mechanical, electrical, functional)

1.3.1.2

bus cycle

the process whereby digital signals effect the transfer of data bytes or words across the interface by means of an interlocked sequence of control signals. “Interlocked” denotes a fixed sequence of events in which one event shall occur before the next event can occur

1.3.1.3

interface (IEC Publication 625-1)

a common boundary between a considered system and another system, or between parts of a system, through which information is conveyed

1.3.1.4

interface system (IEC Publication 625-1)

the set of device-independent mechanical, electrical and functional elements of an interface necessary to effect communication among a set of devices. Cables, connectors, driver and receiver circuits, signal line descriptions, timing and control conventions and functional logic circuits are typical system elements

1.3.1.5

override

a bus master overrides the bus control logic when it is necessary to guarantee itself back-to-back bus cycles. This is called “overriding” or “locking” the bus, temporarily preventing other masters from using the bus

1.3.1.6

system

a set of interconnected elements which achieve a given objective through the performance of a specified function

1.3.2 Signals and Paths (IEC Publication 625-1)

1.3.2.1

bus (IEC Publication 625-1)

a signal line or a set of signal lines used by an interface system to which a number of devices are connected and over which messages are carried

1.3.2.2

byte

a group of eight concurrent binary digits operated on as a unit

1.3.2.3

word

two bytes or sixteen bits operated on as a unit

1.3.2.4

signal (IEC Publication 625-1)

the physical representation of information

NOTE For the purpose of this standard, this is a restricted definition of what is often called “signal” in the general sense, and hereinafter refers to digital electrical signals only.

1.3.2.5

signal parameter (IEC Publication 625-1)

that parameter of an electrical quantity whose value or sequence of values conveys information

1.3.2.6**signal level (IEC Publication 625-1)**

the magnitude of a signal compared to an arbitrary reference magnitude (voltage in the case of this standard)

1.3.2.7**high state (IEC Publication 625-1)**

the more positive voltage level used to represent one of two logical binary states

1.3.2.8**low state (IEC Publication 625-1)**

the more negative voltage level used to represent one of two logical binary states

1.3.2.9**signal line (IEC Publication 625-1)**

one of a set of signal conductors in an interface system used to transfer messages among interconnected devices

1.3.2.10**master**

a functional module capable of initiating data bus transfer

1.3.2.11**slave**

a functional module capable of responding to data transfer operations generated by a master

Section 2. Functional specifications

This section provides an overall understanding of how the bus functions and describes the elements that connect to the bus, the signals that provide the interface to the bus and the different types of operations performed on the bus.

In this section, as well as throughout the standard, a clear and consistent notation for signals has been used. The Memory Write Command (MWTC) will be used to explain this notation. The terms one: zero and true: false can be ambiguous, so their use will be avoided. In their place, we will use the terms electrical High (H) and Low (L). A nathan (“*”, a non-superscript asterisk) following the signal name (MWTC*) indicates that the signal is active low as shown below:

MWTC* = asserted at 0 V

The signal (MWTC*) driven by a three state driver will be pulled up to VCC when not asserted. The following is used to further explain the notation used in this standard.

Function	Electrical	Definition logic	State
MWTC	H	1 True	Active, asserted
	L	0 False	
MWTC*	L	1 True	Active, asserted
	H	0 False	

2.1 Bus Elements

This clause describes the elements (masters and slaves) that interface to the bus and the bus signal lines that comprise this interface.

2.1.1 Masters

A master is any module having the ability to control the bus. The master exercises this control by acquiring the bus through bus exchange logic and then generating command signals, address signals, and memory or I/O addresses. To perform these tasks, the master is equipped with either a central processing unit or logic dedicated to transferring data over to the bus, to and from other destinations. Figure 1, page 4, depicts a system that includes a master and two slave modules.

The system bus architecture can support more than one master in the same system, but in order to do this, there shall be a means for each master to gain control of the bus. This is accomplished through the bus exchange logic (see Clause 2.4).

Masters may operate in one of two modes of operation. Modes 1 and 2 are defined as follows:

- Mode 1: Masters are limited to single bus transfers per bus connect. If all masters are in Mode 1, system timing is rendered deterministic by conformance with a maximum bus busy period. That period is limited by the parameter $t_{\text{BYSO max}}$. (see Sub-clause 3.2.5).
- Mode 2: Masters are unlimited in the bus control. They may invoke bus override. Bus timeouts are allowed. Conformance with the maximum busy period is not required.

The last classification is included to allow for a very broad class of operations, giving users maximum flexibility in meeting the needs of their applications. The first mode of operation is defined to allow system designers to predict the overall performance of their systems without concern for uncontrolled timing parameters such as bus timeout. For masters which can only operate in Mode 2, their specification shall state "Mode 2 master only".

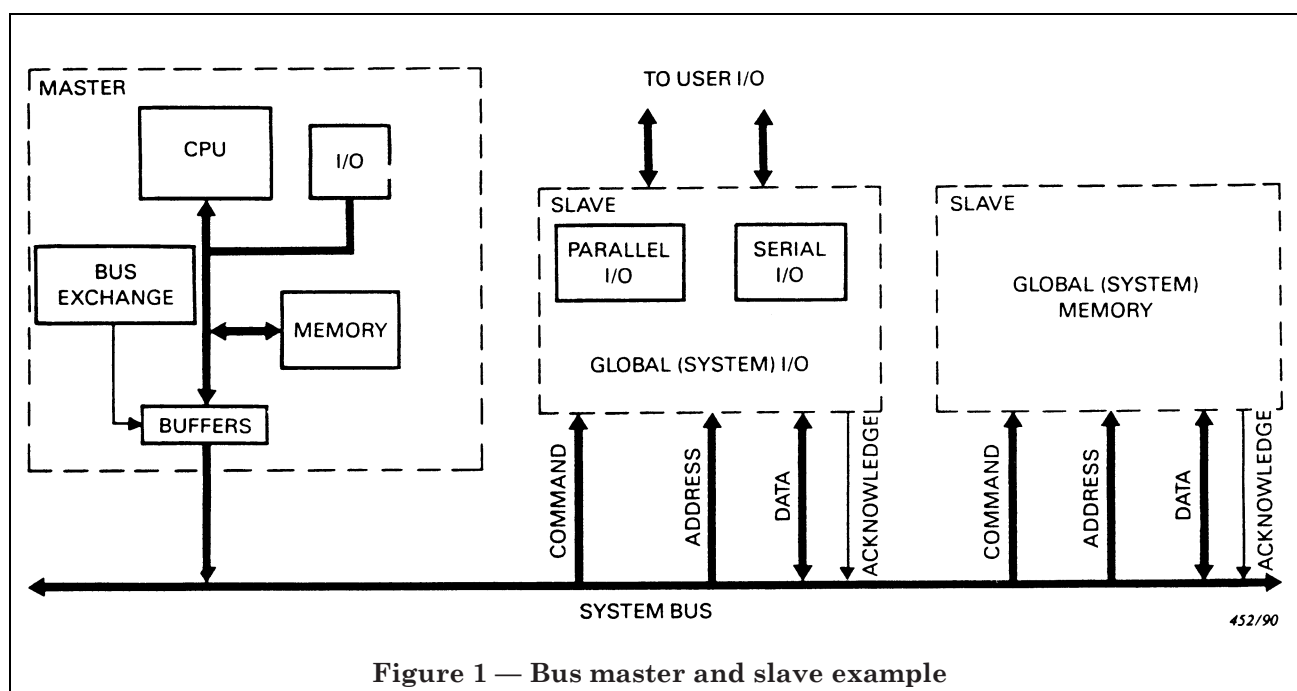
2.1.2 Slaves

Another type of module that can interface to the bus is the slave. Slave modules decode the address lines and act upon the command signals from the masters. The slaves are not capable of controlling the bus. Some examples of bus slaves are shown in Figure 1.

2.1.3 Bus Signals

Signals transferred over the bus can be grouped into several classes based on the functions they perform. The classes are:

- 1) Control lines
- 2) Address and inhibit lines
- 3) Data lines
- 4) Interrupt lines
- 5) Bus exchange lines



The following sub-clauses explain the different classes of bus signals.

2.1.3.1 *Control Lines*

The following signals are classified as control lines:

<i>Class</i>	<i>Function</i>	<i>Signal</i>
Clocks	Constant clock	CCLK*
	Bus clock	BCLK*
Commands	Memory write	MWTC*
	Memory read	MRDC*
	I/O write	IOWC*
	I/O read	IORC*
Acknowledge	Transfer acknowledge	XACK*
Initialize		INIT*
Lock		LOCK*

2.1.3.1.1 *Clock Lines*

1) Bus Clock (BCLK*)

A periodic signal used to synchronize the bus contention logic; it may be slowed, stopped, or single stepped. The Bus Clock shall be generated by one and only one source within the system. This means that each standalone bus master shall have the capability of generating an acceptable clock that can optionally be connected to, or disconnected from, the bus. In a multimaster system, only one of the masters shall have its clock connected to the bus.

2) Constant Clock (CCLK*)

A periodic signal of constant frequency, which may be used by masters or slaves as a master clock. The Constant Clock shall be generated by only one source within the system. This means that each bus master shall have the capability of generating an acceptable clock that can optionally be connected to, or disconnected from, the bus. In a multimaster system, only one of the masters shall have its clock connected to the bus.

2.1.3.1.2 *Command Lines* (MWTC*, MRDC*, IOWC*, IORC*)

The command lines are elements of a communication link between the masters and slaves. There are two command lines for memory and two command lines for I/O. An active command line indicates to the slave that the address lines are carrying a valid address, and that the slave is to perform the specified operation. In a data write cycle, the active command line (MWTC* or IOWC*) additionally indicates that the data is valid on the bus. In a data read cycle, the transition of the command (MRDC* or IORC*) from active to inactive indicates that the master has received the data from the slave.

2.1.3.1.3 *Transfer Acknowledge Line* (XACK*)

This line is used by the slaves to acknowledge commands from the master. XACK* indicates to the master that the requested action is complete, and that data has been placed on, or accepted from, the data lines.

2.1.3.1.4 *Initialize* (INIT*)

The INIT* signal is generated to reset the entire system to a known internal state. This signal is usually generated prior to starting any operation on the system. INIT* may be generated by any or all of the bus masters or by an external source such as a buffered and debounced front panel switch.

2.1.3.1.5 *Lock* (LOCK*)

The LOCK* signal is generated by the master in control of the bus to indicate that the bus is locked. LOCK* is used to extend mutual exclusion to multiple port RAM designs.