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BSI Standards Publication

Road vehicles — Controller area network (CAN)

Part 2: High-speed physical medium attachment (PMA) sublayer

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National foreword

This British Standard is the UK implementation of ISO 11898-2:2024. It supersedes BS ISO 11898-2:2016, which is withdrawn.

The UK participation in its preparation was entrusted to Technical Committee AUE/16, Data Communication (Road Vehicles).

A list of organizations represented on this committee can be obtained on request to its committee manager.

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Part 2: High-speed physical medium attachment (PMA) sublayer

Véhicules routiers — Gestionnaire de réseau de communication (CAN) —

Partie 2: Sous-couche de l'unité d'accès au support à haute vitesse (PMA)

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Foreword

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The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of ISO document should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

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This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

This third edition cancels and replaces the second edition (ISO 11898-2:2016), which has been technically revised.

The main changes are as follows:

— Clause 5 is restructured, the parameters are categorized by static parameter and dynamic parameter;

— Table 13 with bit rates above 1 Mbit/s and up to 2 Mbit/s is in this edition Table 15 (parameter set A). Table 14 with bit rates above 2 Mbit/s and up to 5 Mbit/s is now Table 16 (parameter set B). The parameter set C (see Table 17 and Table 18) in this edition is newly introduced;

— Annex A in this edition is newly introduced; it specifies HS-PMAs with the SIC mode and the FAST mode. Annex B and Annex C in this edition are Annex A and Annex B in the previous edition. The content is unchanged.

A list of all parts in the ISO 11898 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

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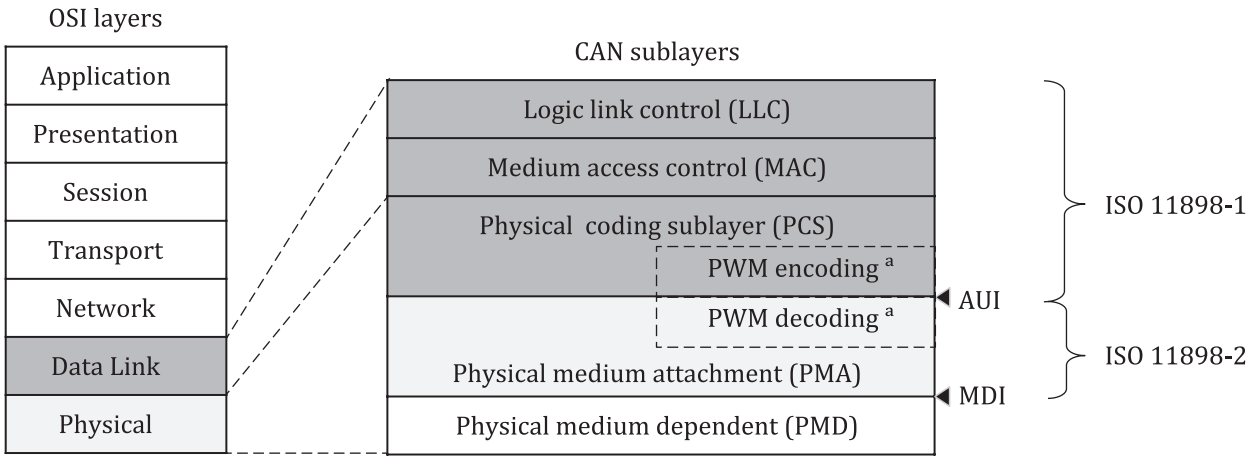
Introduction

The ISO 11898 series provides requirement specifications for the CAN data link layer and physical layer. It is intended for chip implementers, e.g. ISO 11898-1 for CAN protocol controllers and this document for CAN transceivers. Related conformance test plans are given in the ISO 16845 series. The CAN data link layer models the open system interconnect (OSI) data link layer; it is internally subdivided into logic link control (LLC) and medium access control (MAC). ISO 11898-1 also specifies the CAN physical coding sublayer (PCS) by means of the attachment unit interface (AUI). Optionally, the PCS also provides the PWM encoding to be linked to a CAN SIC XL transceiver, which provides the PWM decoding.

The open system interconnect (OSI) layers above the data link layer (e.g. the network layer) are not specified in the ISO 11898 series.

Figure 1 shows the relation between the OSI layers and the CAN sublayers.



Key

AUI attachment unit interface

MDI medium dependent interface

a Only supported by CAN XL.

Figure 1 — CAN data link and physical sublayers relation to the OSI model

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Road vehicles — Controller area network (CAN) —

Part 2: High-speed physical medium attachment (PMA) sublayer

1 Scope

This document specifies physical medium attachment (PMA) sublayers for the controller area network (CAN). This includes the high-speed (HS) PMA without and with low-power mode capability, without and with selective wake-up functionality. Additionally, this document specifies PMAs supporting the signal improvement capability (SIC) mode and the FAST mode in Annex A. The physical medium dependent (PMD) sublayer is not in the scope of this document.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 7498-1, *Information technology — Open Systems Interconnection — Basic Reference Model: The Basic Model*

ISO 11898-1[1)], *Road vehicles — Controller area network (CAN) — Part 1: Data link layer and physical signalling*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO/IEC 7498-1, ISO 11898-1 and the following apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at https://www.electropedia.org/

3.1
active recessive
intermediate high-speed physical medium attachment (HS-PMA) output drive with a dedicated lower than nominal impedance at transitions from dominant state or level_0 state towards the *passive recessive* (3.14) state with a dedicated duration

3.2
attachment unit interface
AUI
interface between the *physical coding sublayer (PCS)* (3.15) and the *physical medium attachment (PMA)* (3.16) sublayer

3.3
bus
shared medium of any topology

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3.4
bus state
state of the *medium dependent interface (MDI)* (3.11), which is dominant or recessive if the *physical medium attachment (PMA)* (3.16) sublayer is in arbitration mode, or is level_0 or level_1 otherwise

Note 1 to entry: The dominant state represents the logical 0 and the recessive state represents the logical 1. During simultaneous transmission of dominant and recessive bits, the resulting bus state is dominant. When no transmission is in progress, the *bus* (3.3) is idle. During idle time, it is in recessive state.

Note 2 to entry: The level_0 state represents the logical 0, and the level_1 state represents the logical 1.

3.5
CAN_H, CAN_L
pair of ports, where $V_{\mathrm{CAN_H}} - V_{\mathrm{CAN_L}}$ is positive at dominant *bus state* (3.4) and level_0 bus state

3.6
edge
difference in *bus states* (3.4) between two consecutive time quanta

3.7
FAST RX mode
mode in which the *physical medium attachment (PMA)* (3.16) sublayer drives the *bus state* (3.4) recessive and the receive thresholds are adjusted to distinguish between the bus states level_0 and level_1

3.8
FAST TX mode
mode in which the *physical medium attachment (PMA)* (3.16) sublayer drives the *bus states* (3.4) level_0 and level_1, which are not able to overwrite each other

3.9
legacy implementation
HS-PMA implementation compliant with previous ISO 11898-2 editions

3.10
low-power mode
mode in which the transceiver is not capable of transmitting or receiving frames, except for the purposes of determining if a WUP or WUF is being received

3.11
MDI
medium dependent interface
electrical interface consisting of CAN_H and CAN_L, that defines the signal transfer between the *physical medium dependent (PMD)* sublayer and the *physical medium attachment (PMA)* (3.16) sublayer

3.12
nominal bit time
duration of one bit in the arbitration phase

3.13
normal-power mode
mode in which the transceiver is capable of transmitting and receiving

3.14
passive recessive
final high-speed physical medium attachment (HS-PMA) output drive with nominal impedance, also known as recessive

3.15
physical coding sublayer
PCS
sublayer of the open system interconnect (OSI) physical layer that performs bit encoding/decoding and synchronization

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3.16
physical medium attachment
PMA
sublayer of the open system interconnect (OSI) physical layer that converts physical signals into logical signals and vice versa

3.17
PWM decoding
PWMD
physical medium attachment (PMA) (3.16) sublayer function decoding the pulse-width modulation (PWM) bit streams into the non-return-to-zero (NRZ) bit streams

3.18
PWM encoding
PWME
physical coding sublayer (PCS) (3.15) function encoding the non-return-to-zero (NRZ) bit streams into the pulse-width modulation (PWM) bit streams

3.19
receiver
node that, while the *bus* (3.3) is not idle, is neither a *transmitter* (3.23) nor is it integrating

3.20
RXD
port of the *attachment unit interface (AUI)* (3.2) used to transmit the actual state of the physical medium, in binary format, to the *physical coding sublayer (PCS)* (3.15)

3.21
signal improvement capability
SIC
capability to suppress the ringing on the MDI

Note 1 to entry: It is as specified in the high-speed physical medium attachment (HS-PMA) implementation parameter set C in Table 14 and Table 17.

3.22
SIC mode
mode according to the high-speed physical medium attachment (HS-PMA) during the arbitration phase

Note 1 to entry: For PMA implementations, it is according to parameter set C or Annex A.

3.23
transmitter
node sending CAN frames

3.24
TXD
port of the *attachment unit interface (AUI)* (3.2) driven by the *physical coding sublayer (PCS)* (3.15) to control how the *physical medium attachment (PMA)* (3.16) influences the actual state of the physical medium

4 Abbreviated terms

For the purposes of this document, the symbols and abbreviated terms given in ISO 11898-1 and the following apply. If the definition of the term in this document is different from the definition in ISO 11898-1, this definition applies.

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CAN	controller area network
DLC	data length code
ECU	electronic control unit
EMC	electromagnetic compatibility
ESD	electro static discharge
GND	ground
HS-PMA	high-speed PMA
NRZ	non-return-to-zero
OSI	open layer system
PMD	physical medium dependent
PN	partial networking
PWM	pulse width modulation
RF	radio frequency
WUF	wake-up frame
WUP	wake-up pattern

5 HS-PMA function

5.1 Base requirements

The HS-PMA comprises one transmitter and one receiving entity. It shall be able to bias the connected physical medium, an electric two-wire cable, relative to a common ground. The transmitter entity shall drive a differential voltage between the CAN_H and CAN_L signals to signal a logical 0 (dominant) or shall not drive a differential voltage to signal a logical 1 (recessive) to be received by other nodes connected to the very same medium. These two signals are the interface to the PMD sublayer.

The HS-PMA shall provide an AUI to the physical coding sublayer as specified in ISO 11898-1. It comprises the TXD and RXD signals as well as the GND signal. The TXD signal receives from the physical coding sublayer the bit stream to be transmitted on the MDI. The RXD signal transmits to the physical coding sublayer the bit stream received from the MDI.

Implementations that comprise one or more HS-PMAs shall at least support the normal-power mode of operation. A low-power mode may be implemented.

Some of the items specified in the following depend on the operation mode of the (part of the) implementation, in which the HS-PMA is included.

Table 1 shows the possible combinations of HS-PMA operating modes and expected behaviour.

Table 1 — HS-PMA operating modes and expected behaviour

Operating mode	Bus-biasing behaviour	Transmitter behaviour
Normal-power mode	Bus biasing active	Dominant or recessive[a]
Low-power mode	Bus biasing active or inactive	Recessive

[a] Depends on input conditions as described in this document.

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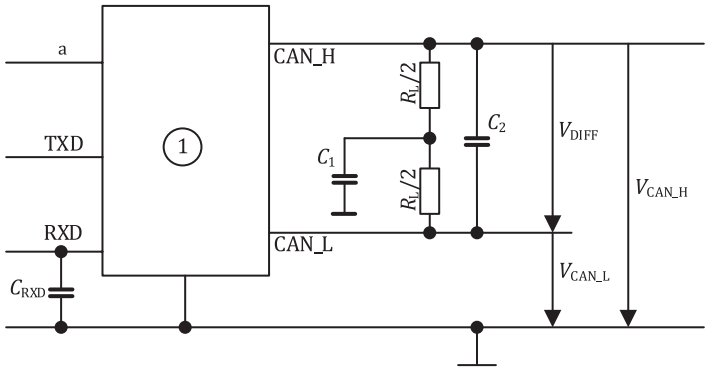
Parameters given in Clause 5 shall be fulfilled throughout the operating temperature range and supply voltage range (if not explicitly specified for unpowered) as specified individually for every HS-PMA implementation.

5.2 HS-PMA test circuit

The outputs of the HS-PMA implementation to the CAN signals are called CAN_H and CAN_L, TXD is the transmit data input and RXD is the receive data output. Figure 2 shows the external circuit used to measure the specified voltage and current parameters. R_L represents the effective resistive load (bus load) for an HS-PMA implementation, when used in a network, and C_1 represents an optional split-termination capacitor. The values of R_L and C_1 vary for different parameters that the HS-PMA implementation needs to meet and are given as condition in the tables of related parameters.



Key

1	PMA implementation
V_{Diff}	differential voltage between CAN_H and CAN_L wires
V_{CAN_H}	single-ended voltage on CAN_H wire
V_{CAN_L}	single-ended voltage on CAN_L wire
C_{RXD}	capacitive load on RXD
C_1	optional split-termination capacitor
C_2	differential capacitive load
R_L	differential load resistance
a	Power supply for the PMA implementation.

Figure 2 — HS-PMA test circuit

5.3 Static parameter

5.3.1 Maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}

Table 2 specifies upper and lower limit static voltages, which can be applied to CAN_H and CAN_L without causing damage, while V_{Diff} stays within in its own maximum rating range.

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Table 2 — HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}

Parameter description	Notation	Value	
		Min. [V]	Max. [V]
Maximum rating	V_{Diff}[a]	−5,0	+10,0
General maximum rating	V_{CAN_H}, V_{CAN_L}	−27,0	+40,0
Optional: Extended maximum rating	V_{CAN_H}, V_{CAN_L}	−58,0	+58,0

[a] This is required regardless whether general or extended maximum rating for V_{CAN_H} and V_{CAN_L} is fulfilled.

Applies to HS-PMA implementation powered and unpowered conditions. Applies to transmit data input de-asserted and transmit data input (TXD) becomes asserted while CAN_H or/and CAN_L connected to a fixed voltage.

The maximum rating for V_{Diff} excludes that all combinations of V_{CAN_H} and V_{CAN_L} are compliant to this document. $V_{Diff} = V_{CAN_H} - V_{CAN_L}$, see Figure 2.

5.3.2 Recessive output characteristics, bus biasing active

Table 3 specifies the recessive output characteristics when bus biasing is active.

Table 3 — HS-PMA recessive output characteristics, bus biasing active

Parameter	Notation	Value		
		Min. [V]	Nom. [V]	Max. [V]
Single-ended output voltage on CAN_H [a]	V_{CAN_H}	+2,0	+2,5	+3,0
Single-ended output voltage on CAN_H [b]	$V_{CAN_H_rec}$	+2,137	+2,5	+2,887
Single-ended output voltage on CAN_L [a]	V_{CAN_L}	+2,0	+2,5	+3,0
Single-ended output voltage on CAN_L [b]	$V_{CAN_L_rec}$	+2,137	+2,5	+2,887
Differential output voltage	V_{Diff}	−0,5	0	+0,05

NOTE The requirements in this table apply concurrently. Therefore, not all combinations of V_{CAN_H} and V_{CAN_L} are compliant with the defined differential output voltage.

[a] Measurement setup according to Figure 2 (including implementations with selective wake-up function):

$R_L > 10^{10}$ Ω (not present)

C_1 = 0 pF (not present)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

[b] Measurement setup according to Figure 2:

R_L = 60 Ω (tolerance ≤ ± 1 %)

C_1 = 0 pF (not present)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

5.3.3 Recessive output characteristics, bus biasing inactive

Table 4 specifies the recessive output characteristics when bus biasing is inactive.

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Table 4 — HS-PMA recessive output characteristics, bus biasing inactive

Parameter	Notation	Value [a]		
		Min. [V]	Nom. [V]	Max. [V]
Single-ended output voltage on CAN_H	V_{CAN_H}	−0,1	0	+0,1
Single-ended output voltage on CAN_L	V_{CAN_L}	−0,1	0	+0,1
Differential output voltage	V_{Diff}	−0,2	0	+0,2

NOTE See 5.5.6 to determine when bias is inactive.

[a] Measurement setup according to Figure 2:

$R_L > 10^{10}$ Ω (not present)

C_1 = 0 pF (not present)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

5.3.4 Dominant output characteristics

Table 5 specifies the output characteristics during dominant state. Figure 3 illustrates the voltage range for the dominant state.

Table 5 — HS-PMA dominant output characteristics

Parameter	Notation	Value [a]			Condition [b]
		Min. [V]	Nom. [V]	Max. [V]	
Single-ended voltage on CAN_H	V_{CAN_H}	+2,75	+3,5	+4,5	R_L = 50 Ω to 65 Ω
Single-ended voltage on CAN_L	V_{CAN_L}	+0,5	+1,5	+2,25	R_L = 50 Ω to 65 Ω
Differential voltage on normal bus load	V_{Diff}	+1,5	+2,0	+3,0	R_L = 50 Ω to 65 Ω
Differential voltage on effective resistance during arbitration	V_{Diff}	+1,5	Not defined	+5,0	R_L = 2 240 Ω (See NOTE)
Optional: Differential voltage on extended bus load range	V_{Diff}	+1,4	+2,0	+3,3	R_L = 45 Ω to 70 Ω

NOTE Assuming a maximum R_L of 70 Ω, this scenario covers a 32-node network (2 240 Ω/70 Ω = 32), 2 240 Ω is emulating a situation with up to 32 nodes transmitting dominant value simultaneously. In such case, the effective load resistance for single nodes decreases (a node does drive only a part of the nominal bus load).

[a] Requirements given in this table apply concurrently. Therefore, not all combinations of V_{CAN_H} and V_{CAN_L} are compliant with the defined differential voltage (see Figure 3).

[b] Measurement setup according to Figure 2:

C_1 = 0 pF (not present)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

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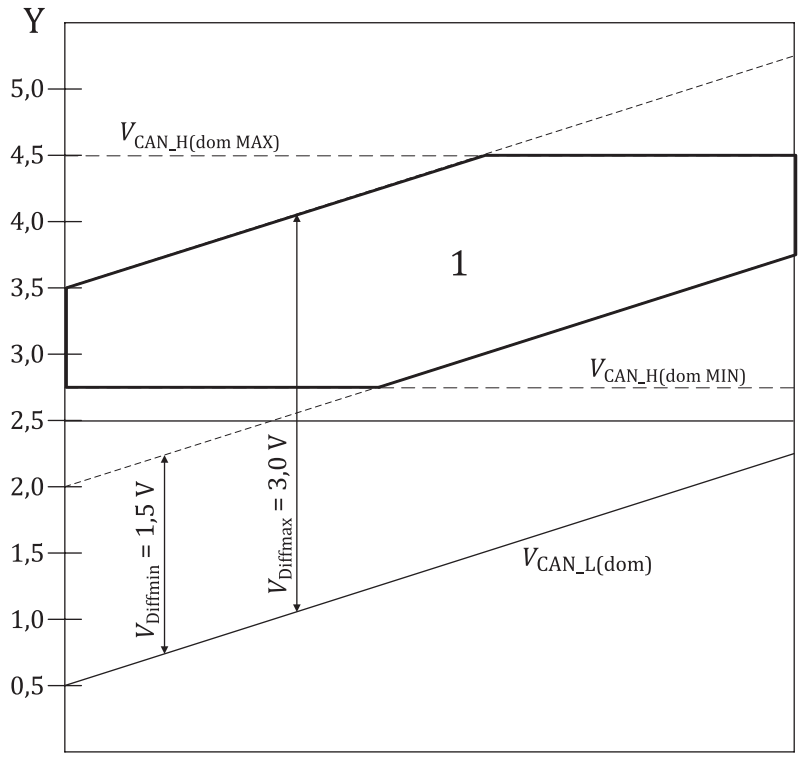

Key

Y	V_{CAN_H} and V_{CAN_L}
1	range of $V_{CAN_H(dom)}$
V_{Diff}	differential voltage between CAN_H and CAN_L wires
V_{CAN_H}	single-ended voltage on CAN_H wire
V_{CAN_L}	single-ended voltage on CAN_L wire

Figure 3 — Voltage range of V_{CAN_H} during dominant state of CAN node, when V_{CAN_L} varies from minimum to maximum voltage level (50-Ω to 65-Ω bus-load condition)

5.3.5 Maximum driver output current

Table 6 specifies the maximum HS-PMA driver output current.

Table 6 — Maximum HS-PMA driver output current

Parameter	Notation	Value [a]		Condition
		Min. [mA]	Max. [mA]	
Absolute current on CAN_H	I_{CAN_H}	not specified	115	$-3\ V \le V_{CAN_H} \le +18\ V$
Absolute current on CAN_L	I_{CAN_L}	not specified	115	$-3\ V \le V_{CAN_L} \le +18\ V$

NOTE It is expected that the implementation does not stop driving its output dominant when the differential voltage between CAN_H and CAN_L is outside the limits given in the condition column. The minimum output current is implicitly specified in Table 5 and thus can be expected to be above 30 mA.

[a] Measurement setup according to Figure 2:

$R_L > 10^{10}\ \Omega$ (not present)

$C_1 = 0$ pF (not present)

$C_2 = 0$ pF (not present)

$C_{RXD} = 0$ pF (not present)

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5.3.6 PMA static receiver input characteristics, bus biasing active and inactive

Table 7 specifies the voltage ranges for the HS-PMA static receiver in low-power mode, when the bus biasing is active.

Table 7 — HS-PMA static receiver input characteristics, bus biasing active

Parameter	Notation	Value [a]		Condition
		Min. [V]	Max. [V]	
Recessive state differential input voltage range	V_{Diff}	−3,0	+0,5	$-12{,}0\ V \le V_{CAN_L} \le +12{,}0\ V$ $-12{,}0\ V \le V_{CAN_H} \le +12{,}0\ V$
Dominant state differential input voltage range	V_{Diff}	+0,9	+8,0	$-12{,}0\ V \le V_{CAN_L} \le +12{,}0\ V$ $12{,}0\ V \le V_{CAN_H} \le +12{,}0\ V$

[a] Measurement setup according Figure 2:

$R_L > 10^{10}\ \Omega$ (not present)

$C_1 = 0$ pF (not present)

$C_2 = 0$ pF (not present)

$C_{RXD} = 0$ pF (not present)

NOTE A negative differential voltage can temporarily occur when the HS-PMA is connected to a medium in which common mode chokes and/or unterminated stubs are present. The maximum positive differential voltage can temporarily occur when the HS-PMA is connected to a medium while more than one HS-PMA is sending dominant and concurrently a ground shift between the sending HS-PMAs is present.

Table 8 specifies the the voltage ranges for the HS-PMA static receiver in low-power mode, when the bus biasing is inactive.

Table 8 — HS-PMA static receiver input characteristics, bus biasing inactive

Parameter	Notation	Value [a]		Condition
		Min. [V]	Max. [V]	
Recessive state differential input voltage range	V_{Diff}	−3,0	+0,4	$-12{,}0\ V \le V_{CAN_L} \le +12{,}0\ V$ $-12{,}0\ V \le V_{CAN_H} \le +12{,}0\ V$
Dominant state differential input voltage range	V_{Diff}	+1,15	+8,0	$-12{,}0\ V \le V_{CAN_L} \le +12{,}0\ V$ $-12{,}0\ V \le V_{CAN_H} \le +12{,}0\ V$

[a] Measurement setup according Figure 2:

$R_L > 10^{10}\ \Omega$ (not present)

$C_1 = 0$ pF (not present)

$C_2 = 0$ pF (not present)

$C_{RXD} = 0$ pF (not present)

NOTE A negative differential voltage can temporarily occur when the HS-PMA is connected to a medium in which common mode chokes and/or unterminated stubs are present. The maximum positive differential voltage can temporarily occur when the HS-PMA is connected to a medium while more than one HS-PMA is sending dominant and concurrently a ground shift between the sending HS-PMAs is present.

5.3.7 Receiver input resistance

Figure 4 shows an equivalent circuitry of the HS-PMA internal differential input resistance. Table 9 specifies the HS-PMA receiver input resistance parameter. Table 10 specifies the HS-PMA receiver input resistance matching parameters.

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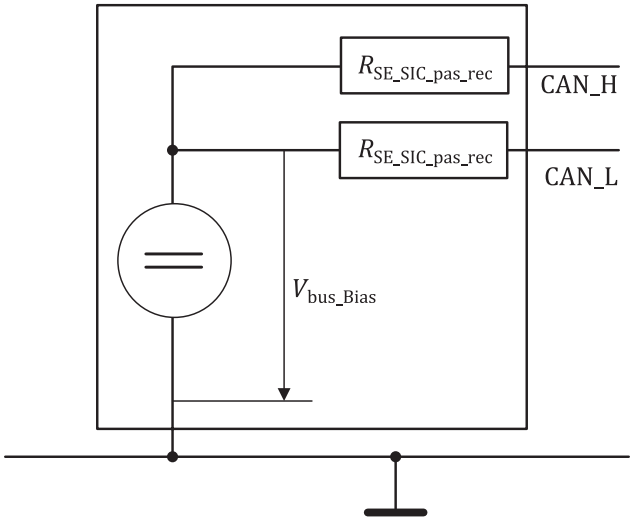

Figure 4 — Illustration of HS-PMA internal differential input resistance

Table 9 — HS-PMA receiver input resistance

Parameter	Notation	Value		Condition
		Min. [kΩ]	Max. [kΩ]	
Differential internal resistance	$R_{DIFF_pas_rec}$ [a]	12	100	$-2\ V \leq V_{CAN_L}$ $V_{CAN_H} \leq +7\ V$
Single-ended internal resistance	$R_{SE_pas_rec_H}$ $R_{SE_pas_rec_L}$	6	50	
[a] $R_{DIFF_pas_rec} = R_{SE_pas_rec_H} + R_{SE_pas_rec_L}$.				

Table 10 — HS-PMA receiver input resistance matching

Parameter	Notation	Value		Condition
		Min.	Max.	
Matching[a] of internal resistance	m_R	−0,03	+0,03	V_{CAN_L}, V_{CAN_H}: +5 V
[a] The matching shall be calculated as $m_R = 2 \times (R_{SE_H} - R_{SE_L})/(R_{SE_H} + R_{SE_L})$.				

5.3.8 Maximum leakage currents of CAN_H and CAN_L

An unpowered HS-PMA implementation shall not disturb the communication of other HS-PMAs that are connected to the same medium. Table 11 specifies the HS-PMA maximum leakage currents.

Table 11 — HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered

Parameter	Notation	Value	
		Min. [µA]	Max. [µA]
Leakage current on CAN_H, CAN_L	I_{CAN_H}, I_{CAN_L}	−10	+10
$V_{CAN_H} = 5\ V$, $V_{CAN_L} = 5\ V$, all supply inputs are connected to GND. Positive currents are flowing into the implementation.			

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5.4 Dynamic parameter

5.4.1 Driver symmetry

In order to achieve a level of RF emission that is acceptably low, the transmitter shall meet the driver signal symmetry as specified in Table 12.

Table 12 — HS-PMA driver symmetry

Parameter	Notation	Value [c]		
		Min.	Nom.	Max.
Driver symmetry based on V_{CC} [a]	v_{sym_vcc}	+0,9	+1,0	+1,1
Driver symmetry based on V_{rec_sum} [b]	v_{sym_vrec}	+0,9	+1,0	+1,1

[a] $v_{sym_vcc} = (V_{CAN_H} + V_{CAN_L})/V_{CC}$, with V_{CC} being the power supply of the transmitter
[b] $v_{sym_vrec} = (V_{CAN_H} + V_{CAN_L})/V_{sum}$, without V_{CC} reference
$V_{rec_sum} = V_{CAN_H_rec} + V_{CAN_L_rec}$

V_{sym_vcc} and V_{sym_vrec} shall be observed during dominant state and recessive state and also during the transition from dominant to recessive and vice versa, while TXD is stimulated by a square wave signal with a frequency that corresponds to the highest bit rate for which the HS-PMA implementation is intended, however, at most 1 MHz (2 Mbit/s) (HS-PMA in normal-power mode).

[c] Measurement setup according to Figure 2:
R_L = 60 Ω (tolerance ≤ ± 1 %)
C_1 = 4,7 nF (tolerance ≤ ± 5 %)
C_2 = 0 pF (not present)
C_{RXD} = 0 pF (not present)

5.4.2 Optional transmit dominant timeout

An implementation of an HS-PMA may limit the duration of dominant transmission in order not to prevent other CAN nodes from communication when the TXD input is permanently asserted. The HS-PMA implementation should implement a timeout. Table 13 recommends the optional HS-PMA transmit dominant timeout value range.

Table 13 — Optional HS-PMA transmit dominant timeout

Parameter	Notation	Value [a]	
		Min. [ms]	Max. [ms]
Transmit dominant timeout[a]	t_{dom}	0,8	10,0

[a] A minimum value of 0,3 ms is accepted for legacy implementations.

NOTE There is a relation between the t_{dom} minimum value and the minimum bit rate. A t_{dom} minimum value of 0,8 ms accommodates 17 consecutive dominant bits at bit rates greater than or equal to 21,6 kbit/s and 36 consecutive dominant bits at bit rates greater than or equal to 45,8 kbit/s. The value 17 reflects PMA implementation attempts to send a dominant bit and every time sees a recessive level at the receive data input. The value 36 reflects six consecutive error frames when there is a bit error in the last bit of the first five attempts.

5.4.3 Transmitter and receiver timing behaviour

Figure 5 defines the HS-PMA implementation timing. Table 14 specifies the the HS-PMA implementation loop-delay requirements for parameter set A, parameter set B, and parameter set C. Table 15 specifies the HS-PMA implementation data signal timing requirements for parameter set A. Table 16 specifies the HS-PMA implementation data signal timing requirements for parameter set B. Table 17 and Table 18 specify HS-PMA implementation data signal timing requirements for parameter set C.

NOTE HS-PMA implementations with signal improvement capability developed prior to this document can refer to the CiA 601–4 specification.

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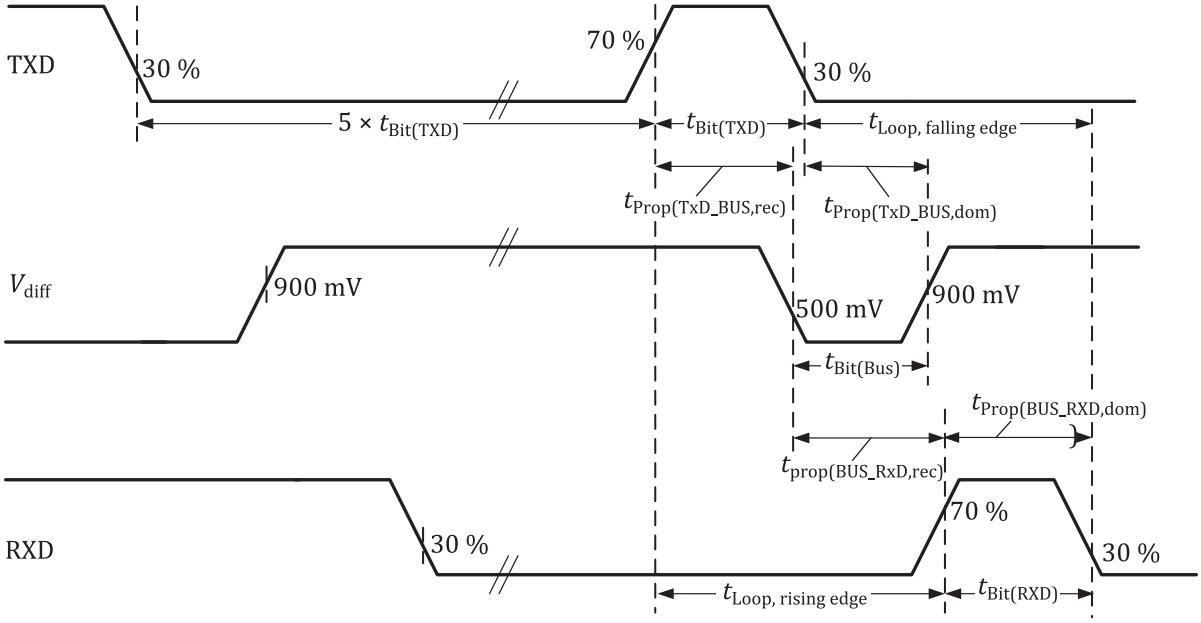

Key

$t_{Bit(TXD)}$ nominal bit time of the bit rates the HS-PMA supports

Figure 5 — HS-PMA implementation timing definitions

Table 14 — HS-PMA implementation loop-delay requirement for parameter sets A, B and C

Parameter	Notation	Value [b]	
		Min. [ns]	Max. [ns]
Loop delay for parameter set A and parameter set B [a]	t_{Loop}	not specified	255
Loop delay for parameter set C [a]	t_{Loop}	not specified	190
Propagation delay from TXD to CAN_H/CAN_L for parameter set C	$t_{prop(TXD_BUS)}$	not specified	80
Propogation delay from CAN_H/CAN_L to RXD for parameter set C	$t_{prop(BUS_RXD)}$	not specified	110

[a] Time span from signal edge on TXD input to the next signal edge with the same polarity on RXD output, the maximum of delay of both signal edges is to be considered.

[b] Measurement setup according to Figure 2:

R_L = 60 Ω (tolerance ≤ ± 1 %)

C_1 = 0 pF (not present)

C_2 = 100 pF (tolerance ≤ ± 1 %)

C_{RXD} = 15 pF (tolerance ≤ ± 1 %)

Measurement according to Figure 5:

The input signal on TXD shall have rise and fall times (10 %/90 %) of less than 10 ns.

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Table 15 — HS-PMA implementation data signal timing requirements for parameter set A

Parameter	Notation	Value [d]	
		Min. [ns]	Max. [ns]
Transmitted recessive bit width variation	$t_{\Delta\mathrm{Bit(Bus)}}$ [a]	−65	+30
Received recessive bit width variation	$t_{\Delta\mathrm{Bit(RXD)}}$ [b]	−100	+50
Receiver timing symmetry	$t_{\Delta\mathrm{REC}}$ [c]	−65	+40

[a] $t_{\Delta\mathrm{Bit(Bus)}} = t_{\mathrm{Bit(Bus)}} - t_{\mathrm{Bit(TXD)}}$

[b] $t_{\Delta\mathrm{Bit(RXD)}} = t_{\mathrm{Bit(RXD)}} - t_{\mathrm{Bit(TXD)}}$

[c] $t_{\Delta\mathrm{Rec}} = t_{\mathrm{Bit(RXD)}} - t_{\mathrm{Bit(Bus)}}$

The requirements in this table apply concurrently. Therefore, not all combinations of $t_{\Delta\mathrm{Bit(Bus)}}$ and $t_{\Delta\mathrm{Rec}}$ are compliant with $t_{\Delta\mathrm{Bit(RXD)}}$.

[d] Measurement setup according to Figure 2:

R_L = 60 Ω (tolerance ≤ ± 1 %)

C_1 = 0 pF (not present)

C_2 = 100 pF (tolerance ≤ ± 1 %)

C_{RXD} = 15 pF (tolerance ≤ ± 1 %)

Measurement according to Figure 5:

The input signal on TXD shall have rise and fall times (10 %/90 %) of less than 10 ns.

NOTE Limits for $t_{\mathrm{Bit(Bus)}}$ and $t_{\mathrm{Bit(RXD)}}$ are not defined for intended use with bit rates up to 1 Mbit/s.

Table 16 — HS-PMA implementation data signal timing requirements for parameter set B

Parameter	Notation	Value [d]	
		Min. [ns]	Max. [ns]
Transmitted recessive bit width variation	$t_{\Delta\mathrm{Bit(Bus)}}$ [a]	−45	+10
Received recessive bit width variation	$t_{\Delta\mathrm{Bit(RXD)}}$ [b]	−80	+20
Receiver timing symmetry variation	$t_{\Delta\mathrm{Rec}}$ [c]	−45	+15

[a] $t_{\Delta\mathrm{Bit(Bus)}} = t_{\mathrm{Bit(Bus)}} - t_{\mathrm{Bit(TXD)}}$

[b] $t_{\Delta\mathrm{Bit(RXD)}} = t_{\mathrm{Bit(RXD)}} - t_{\mathrm{Bit(TXD)}}$

[c] $t_{\Delta\mathrm{Rec}} = t_{\mathrm{Bit(RXD)}} - t_{\mathrm{Bit(Bus)}}$

The requirements in this table apply concurrently. Therefore, not all combinations of $t_{\Delta\mathrm{Bit(Bus)}}$ and $t_{\Delta\mathrm{Rec}}$ are compliant with $t_{\Delta\mathrm{Bit(RXD)}}$.

[d] Measurement setup according to Figure 2:

R_L = 60 Ω (tolerance ≤ ± 1 %)

C_1 = 0 pF (not present)

C_2 = 100 pF (tolerance ≤ ± 1 %)

C_{RXD} = 15 pF (tolerance ≤ ± 1 %)

Measurement according to Figure 5:

The input signal on TXD shall have rise and fall times (10 %/90 %) of less than 10 ns.

NOTE Limits for $t_{\mathrm{Bit(Bus)}}$ and $t_{\mathrm{Bit(RXD)}}$ are not defined for intended use with bit rates up to 1 Mbit/s.

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Table 17 — HS-PMA implementation data signal timing requirements for parameter set C

Parameter	Notation	Value [d]	
		Min. [ns]	Max. [ns]
Transmitted recessive bit width variation	$t_{\Delta Bit(Bus)}$ [a]	−10	+10
Received recessive bit width variation	$t_{\Delta Bit(RXD)}$ [b]	−30	+20
Receiver timing symmetry variation	$t_{\Delta Rec}$ [c]	−20	+15

[a] $t_{\Delta Bit(Bus)} = t_{Bit(Bus)} - t_{Bit(TXD)}$

[b] $t_{\Delta Bit(RXD)} = t_{Bit(RXD)} - t_{Bit(TXD)}$

[c] $t_{\Delta Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$

All requirements in this table apply concurrently. Therefore, not all combinations of $t_{\Delta Bit(Bus)}$ and $t_{\Delta Rec}$ are compliant with $t_{\Delta Bit(RXD)}$.

[d] Measurement setup according to Figure 2:

R_L = 60 Ω (tolerance ≤ ± 1 %)

C_1 = 0 pF (not present)

C_2 = 100 pF (tolerance ≤ ± 1 %)

C_{RXD} = 15 pF (tolerance ≤ ± 1 %)

Table 18 specifies the HS-PMA implementation SIC timing and impedance for parameter set C.

Table 18 — HS-PMA implementation SIC timing and impedance for parameter set C

Parameter	Notation	Value		Condition
		Min.	Max.	
Differential internal resistance (CAN_H to CAN_L)	$R_{DIFF_act_rec}$	75 Ω	133 Ω	+2 V ≤ $V_{CAN_H/L}$ ≤ V_{CC} −2 V, if R_{SE} fulfils $R_{SE_act_rec}$ otherwise −12 V ≤ $V_{CAN_H/L}$ ≤ +12 V
Optional internal single-ended resistance	$R_{SE_SIC_act_rec}$	37,5 Ω	66,5 Ω	+2 V ≤ $V_{CAN_H/L}$ ≤ V_{CC} −2 V, if R_{SE} fulfils R_{SE_SIC} otherwise −12 V ≤ $V_{CAN_H/L}$ ≤ V_{CC} +12 V
Start time of active signal improvement phase	$t_{act_rec_start}$	n.a.	120 ns	Measured from rising TXD edge with <5 ns slope at 50 % threshold
End time of active signal improvement phase	$t_{act_rec_end}$	355 ns	n.a.	
Start time of passive recessive phase	$t_{pas_rec_start}$	n.a.	530 ns	Measured from rising TXD edge with < 5 ns slope at 50 % threshold with R_{DIFF} ≥ min. R_{DIFF_REC} and R_{SE} ≥ min. R_{SE}.[a]

[a] Formerly specified in ISO 11898-2:2016, Table 10.

Figure 6 defines the SIC timing.

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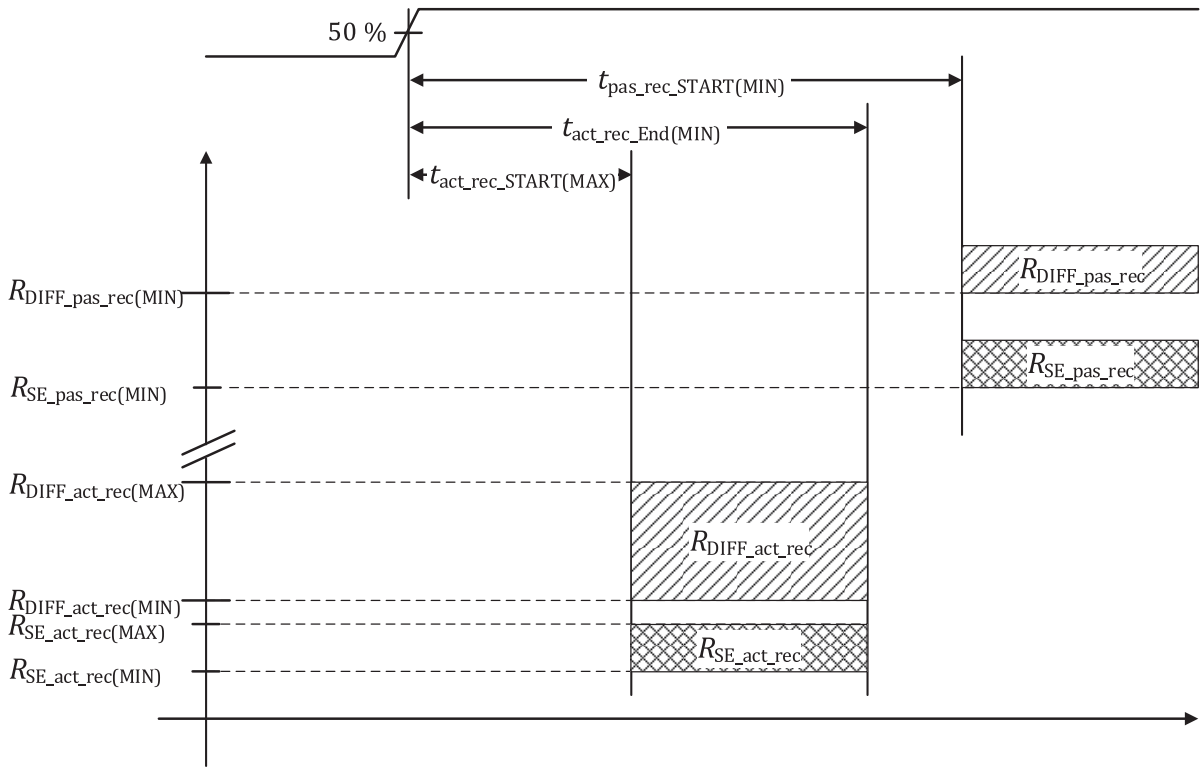

Figure 6 — SIC timing definitions

5.5 Wake-up from low-power mode

5.5.1 Wake-up procedures

When an implementation comprising one or more HS-PMAs implements a low-power mode, the HS-PMA can signal a wake-up event. Table 19 lists the wake-up procedures for defined types of HS-PMA implementations.

Table 19 — HS-PMA wake-up implementations

Type of HS-PMA implementation	Required wake-up mechanism
Without low-power mode	No wake-up
With low-power mode, but without selective wake-up	Either basic wake-up or wake-up pattern (WUP) wake-up
With selective wake-up	Selective wake-up frame (WUF) and wake-up pattern (WUP) wake-up

5.5.2 General requirement

In case more than one wake-up procedure is implemented in an HS-PMA, the wake-up procedure to be used shall be configurable.

5.5.3 Basic wake-up

After having received a dominant state for the duration of at least t_{Filter}, the HS-PMA shall detect a wake-up.

5.5.4 Via wake-up pattern

Upon receiving two consecutive dominant states each for duration of at least t_{Filter}, separated by a recessive state with a duration of at least t_{Filter}, a wake-up event shall happen. This method is illustrated inFigure 7.

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