

BS ISO 17458-4:2013



BSI Standards Publication

Road vehicles — FlexRay communications system

Part 4: Electrical physical layer specification

bsi.

...making excellence a habit.
AVA Documents™
Document Sharing Hub

National foreword

This British Standard is the UK implementation of ISO 17458-4:2013.

The UK participation in its preparation was entrusted to Technical Committee AUE/16, Electrical and electronic equipment.

A list of organizations represented on this committee can be obtained on request to its secretary.

This publication does not purport to include all the necessary provisions of a contract. Users are responsible for its correct application.

© The British Standards Institution 2013. Published by BSI Standards Limited 2013

ISBN 978 0 580 76715 9

ICS 43.040.15

Compliance with a British Standard cannot confer immunity from legal obligations.

This British Standard was published under the authority of the Standards Policy and Strategy Committee on 31 January 2013.

Amendments issued since publication

Date	Text affected
------	---------------

INTERNATIONAL STANDARD

BS ISO 17458-4:2013
ISO
17458-4

First edition
2013-02-01

Road vehicles— FlexRay communications system —

Part 4: Electrical physical layer specification

Véhicules routiers — Système de communications FlexRay —

Partie 4: Spécification de la couche d'application électrique



Reference number
ISO 17458-4:2013(E)

AVA Documents
Document Sharing Hub
© ISO 2013



COPYRIGHT PROTECTED DOCUMENT

© ISO 2013

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from either ISO at the address below or ISO's member body in the country of the requester.

ISO copyright office
Case postale 56 • CH-1211 Geneva 20
Tel. + 41 22 749 01 11
Fax + 41 22 749 09 47
E-mail copyright@iso.org
Web www.iso.org

Published in Switzerland

Contents

Page

Foreword	v
Introduction.....	vi
1 Scope	1
2 Normative references	1
3 Terms, definitions, symbols and abbreviated terms	1
3.1 Terms and definitions	1
3.2 Abbreviated terms	10
3.3 Symbols.....	12
4 Document reference according to OSI model	13
5 Conventions	14
5.1 General	14
5.2 Notational and parameter prefix conventions	14
5.3 Important preliminary notes	15
6 Communication channel basics	16
6.1 Objective.....	16
6.2 Propagation delay	16
6.3 Frame TSS length change	18
6.4 Symbol length change	18
6.5 FES1 length change	19
6.6 Collisions.....	19
6.7 Stochastic jitter.....	20
6.8 Wakeup patterns.....	20
7 Principle of FlexRay networking	22
7.1 Objective.....	22
7.2 Interconnection of nodes.....	22
7.3 Electrical signalling	23
8 Network components	24
8.1 Objective.....	24
8.2 Cables	24
8.3 Connectors.....	25
8.4 Cable termination	25
8.5 Termination concept	27
8.6 Common mode chokes	27
8.7 DC bus load.....	27
9 Network topology	28
9.1 Objective.....	28
9.2 Point-to-point connection.....	29
9.3 Passive star.....	29
9.4 Linear passive bus	30
9.5 Active star network	31
9.6 Cascaded active stars.....	32
9.7 Hybrid topologies	32
9.8 Dual channel topologies	33
10 Asymmetric delay budget.....	33
10.1 Objective.....	33
10.2 Basic topology for asymmetric delay budget.....	34
10.3 Definition of Test Planes.....	34

10.4	Requirements to the asymmetric delay budget.....	36
10.5	Definition of maximum asymmetric delay portions	36
10.6	Other networks.....	43
11	Signal integrity	43
11.1	Objective.....	43
11.2	Mask test at TP1 / TP11	44
12	Electrical bus driver	49
12.1	Overview	49
12.2	Operation modes	50
12.3	Operation mode transitions.....	51
12.4	Bus driver – communication controller interface.....	53
12.5	Bus driver – bus guardian interface (optional).....	57
12.6	Bus driver – host interface	57
12.7	Bus driver – power supply interface.....	61
12.8	Bus driver - level shift interface (optional).....	63
12.9	Bus driver - bus interface	63
12.10	Bus driver – wakeup interface (optional)	77
12.11	Remote wakeup event detector (optional)	78
12.12	Bus driver behaviour under fault conditions	80
12.13	Bus driver functional classes.....	85
12.14	Bus driver signal summary.....	87
13	Active Star	88
13.1	Overview	88
13.2	Hardware overview	88
13.3	Signal timing	90
13.4	Active star device operation modes	98
13.5	Autonomous power moding flag (APM flag).....	100
13.6	Branch operating states.....	101
13.7	Branch transmitter and receiver circuit	104
13.8	Active star - communication controller interface (optional)	105
13.9	Active star – bus guardian interface (optional)	115
13.10	Active star – host interface (optional)	115
13.11	Active star – power supply interface	115
13.12	Active star – level shift interface (optional)	118
13.13	Active star – bus interface	118
13.14	Active star – wake interface (optional)	119
13.15	Active star functional classes	119
13.16	Active star behaviour under fault conditions	120
13.17	Active star signal summary	122
14	Interface definitions.....	123
14.1	Overview	123
14.2	Communication controller – bus driver interface	123
14.3	Host	126
15	General features for FlexRay physical layer parts	127
15.1	Objective	127
15.2	Voltage limits for digital output signals	127
15.3	Input voltage thresholds for digital signals	127
15.4	ESD protection on chip level (HBM)	128
15.5	ESD protection on chip level (IEC61000-4-2)	128
15.6	ESD protection on ECU level.....	128
15.7	Operating temperature	128
15.8	Serial peripheral interface (SPI)	129
Annex A (informative)	Application notes	131

Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

International Standards are drafted in accordance with the rules given in the ISO/IEC Directives, Part 2.

The main task of technical committees is to prepare International Standards. Draft International Standards adopted by the technical committees are circulated to the member bodies for voting. Publication as an International Standard requires approval by at least 75 % of the member bodies casting a vote.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO shall not be held responsible for identifying any or all such patent rights.

ISO 17458-4 was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 3, *Electrical and electronic equipment*.

ISO 17458 consists of the following parts, under the general title *Road vehicles — FlexRay communications system*:

- *Part 1: General information and use case definition*
- *Part 2: Data link layer specification*
- *Part 3: Data link layer conformance test specification*
- *Part 4: Electrical physical layer specification*
- *Part 5: Electrical physical layer conformance test specification*

Introduction

The FlexRay communications system is an automotive focused high speed network and was developed with several main objectives which were defined beyond the capabilities of established standardized bus systems like CAN and some other proprietary bus systems. Some of the basic characteristics of the FlexRay protocol are synchronous and asynchronous frame transfer, guaranteed frame latency and jitter during synchronous transfer, prioritization of frames during asynchronous transfer, single or multi-master clock synchronization, time synchronization across multiple networks, error detection and signalling, and scalable fault tolerance.

The FlexRay communications system is defined for advanced automotive control applications. It serves as a communication infrastructure for future generation high-speed control applications in vehicles by providing:

- A message exchange service that provides deterministic cycle based message transport;
- Synchronization service that provides a common time base to all nodes;
- Start-up service that provides an autonomous start-up procedure;
- Error management service that provides error handling and error signalling;
- Wakeup service that addresses the power management needs.

Since start of development the automotive industry world-wide supported the specification development. The FlexRay communications system has been successfully implemented in production vehicles today.

The ISO 17458 series specifies the use cases, the communication protocol and physical layer requirements of an in-vehicle communication network called "FlexRay communications system".

This part of ISO 17458 has been established in order to define the electrical physical layer of the FlexRay data link.

To achieve this, it is based on the Open Systems Interconnection (OSI) Basic Reference Model specified in ISO/IEC 7498-1 and ISO/IEC 10731, which structures communication systems into seven layers. When mapped on this model, the protocol and physical layer requirements specified by ISO 17458 are broken into:

- Diagnostic services (layer 7), specified in ISO 14229-1 [7], ISO 14229-4 [9];
- Presentation layer (layer 6), vehicle manufacturer specific;
- Session layer services (layer 5), specified in ISO 14229-2 [8];
- Transport layer services (layer 4), specified in ISO 10681-2 [1];
- Network layer services (layer 3), specified in ISO 10681-2 [1];
- Data link layer (layer 2), specified in ISO 17458-2, ISO 17458-3;
- Physical layer (layer 1), specified in ISO 17458-4, ISO 17458-5;

in accordance with Table 1.

Table 1 — FlexRay communications system specifications applicable to the OSI layers

Applicability	OSI 7 layers	FlexRay communications system	Vehicle manufacturer enhanced diagnostics
Seven layer according to ISO 7498-1 and ISO/IEC 10731	Application (layer 7)	vehicle manufacturer specific	ISO 14229-1, ISO 14229-4
	Presentation (layer 6)	vehicle manufacturer specific	vehicle manufacturer specific
	Session (layer 5)	vehicle manufacturer specific	ISO 14229-2
	Transport (layer 4)	vehicle manufacturer specific	ISO 10681-2
	Network (layer 3)	vehicle manufacturer specific	
	Data link (layer 2)	ISO 17458-2, ISO 17458-3	
	Physical (layer 1)	ISO 17458-4, ISO 17458-5	

Table 1 shows ISO 17458 Parts 2 – 5 being the common standards for the OSI layers 1 and 2 for the FlexRay communications system and the vehicle manufacturer enhanced diagnostics.

The FlexRay communications system column shows vehicle manufacturer specific definitions for OSI layers 3 – 7.

The vehicle manufacturer enhanced diagnostics column shows application layer services covered by ISO 14229-4 which have been defined in compliance with diagnostic services established in ISO 14229-1, but are not limited to use only with them. ISO 14229-4 is also compatible with most diagnostic services defined in national standards or vehicle manufacturer's specifications. The presentation layer is defined vehicle manufacturer specific. The session layer services are covered by ISO 14229-2. The transport protocol and network layer services are specified in ISO 10681.

Road vehicles — FlexRay communications system — Part 4: Electrical physical layer specification

1 Scope

This part of ISO 17458 specifies the electrical physical layer for FlexRay communications systems.

The electrical physical layer for FlexRay is designed for time-triggered networks with data-rates up to 10 Mbit/s to connect automotive electronic control units (ECUs). The medium that is used is dual wires. Signalling on the bus is accomplished by asserting a differential voltage between those wires. Topology variations range from point-to-point connections via linear passive busses and passive stars up to active star topologies.

This part of ISO 17458 includes the definition of electrical characteristics of the transmission itself and also documentation of basic functionality for bus driver (BD) and active star (AS) devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 17458-1, *Road vehicles — FlexRay communications system — Part 1: General information and use case definition*

ISO 17458-2, *Road vehicles — FlexRay communications system — Part 2: Data link layer specification*

3 Terms, definitions, symbols and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 17458-1, ISO 17458-2 and the following apply.

3.1.1

alternating current busload

AC busload

equivalent circuit of a passive star from transmitting view of the bus driver

3.1.2

active elements

components which work with power supply and amplifiers

3.1.3

active star network

AS network

all *point-to-point* connections plugged to an AS

3.1.4

activity

See "bus state"

NOTE activity distinguishes two states: *Data_0* and *Data_1*.

3.1.5

Activity

signal to the Central_Logic when this *communication path* is not *idle*(see also *NoActivity*)

3.1.6

asymmetric delay budget

maximum bit-deformation in the time domain

NOTE It is derived from the specified synchronization and sampling procedure and the properties of their implementation. When transmitting a FlexRay data stream the receiving CC must be able to detect the data without any error. If the *asymmetric delay* of the data stream is higher than the *asymmetric delay budget*, the decoder samples faulty bit values.

3.1.7

asymmetric delay

bit-deformation in the time domain when passing a data stream e.g. via a *BD*

EXAMPLE

A data stream is applied to the *BD*'s input *TxD*: ...00100

The single 1 at the centre shall have a length of 100 ns

The *BD* passes the data stream to its output *BP* and *BM*.

The single 1 may be shortened or lengthened a little bit to e.g. 102 ns

In this case the *asymmetric delay* has to be determined to 2 ns.

3.1.8

bus driver – bus driver interface

BD-BD-interface

consideration of all involved effects of the timing of each *BD/AS*

NOTE The timing is specified based on measurement set-ups easy to be used. When connecting two *BDs/ASs* (via e.g. a *passive star*) the resulting delays are not equal to twice the specified values.

3.1.9

bus guardian enable

BGE

input pin of the *BD* that allows deactivating the bus output stage of the *BD*

3.1.10

bias voltage

voltage source with high output impedance

3.1.11

bus minus

BM

bidirectional pin of the *BD/AS* to allow the *BD/AS* the access to the bus.

3.1.12

bus plus

BP

bidirectional pin of the *BD/AS* to allow the *BD/AS* the access to the bus.

3.1.13

branch

component within *active star topologies*

NOTE A *branch* can be built of a *point-to-point* connection, a *linear bus* or a *passive star*.

3.1.14

byte start sequence

BSS

pre-defined sequence of two bits (logical: 10) which is sent in front of each byte

3.1.15

bus guardian

BG

component which allows the node only to transmit during the pre-defined timing slots

3.1.16

bus state

status of the bus FlexRay communication

NOTE Several different states are visible due to the operating modes of the FlexRay system.

EXAMPLE

idle: there is no communication on the bus. Approximately 0 V differential voltage is measurable.

activity: there is an on-going communication on the bus. Approximately ± 600 mV up to $\pm 1\,000$ mV differential voltage is measurable, etc.

3.1.17

cascade

topology character

NOTE If a topology uses more than 1 AS the wording "*cascaded ASs*" is used.

3.1.18

common mode

mode in which two test points are handled simultaneously against ground

EXAMPLE

common mode input impedance of the BD's bus pins *BP* and *BM* to ground.

common mode voltage on the bus: $\frac{1}{2} (u_{BP} + u_{BM})$

3.1.19

communication path

branches CC interface and Intra Star Interface

3.1.20

connection network

components like CMC, termination resistors, *ESD* protection circuits, lines on the *PCB*, connectors, etc

NOTE When implementing a FlexRay system each *BD/AS* has to be plugged to a FlexRay *cable* via these components.

3.1.21

Data_0

bus-state "*activity*" where a logical 0 is transmitted

3.1.22

Data_1

bus-state "*activity*" where a logical 1 is transmitted.

3.1.23

differential mode

mode in which two test points are handled against each other

EXAMPLE

differential mode input impedance of the BD's bus pins BP and BM to ground.

differential mode voltage on the bus: ($u_{BP} - u_{BM}$).

differential mode impedance of the FlexRay cable

3.1.24

dummy load

summary of loads that can be applied to components which are specified by easy-to-use measurement set-ups

EXAMPLE

dummy load at BP and BM: $40\ \Omega \parallel 100\ \text{pF}$.

dummy load at RxD: $15\ \text{pF}$

3.1.25

eye-diagram

diagram that is visible when overlying edge synchronized measured bus signals

NOTE The shape of the eye allows specifying the bus-signals.

3.1.26

frame end sequence

FES

bit sequence that consists of two bits (01) and is sent at the end of each FlexRay data frame

NOTE The asymmetric delay budget is based on the end of a data frame:
in the worst case up to 10 consecutive identical bits can be seen.

$BSS + 1\ \text{byte} + FES = 10\ 00000000\ 01$

3.1.27

functional class

grouping of various features that are implemented together

NOTE The BD/AS offers various technical features. To keep the resulting products testable and to offer them a good chance on the market it is required to implement various features only together.

3.1.28

generic bus driver

simulation model which is derived from the specification directly

NOTE The knowledge about real implementations is taken into consideration. The generic BD supports a receiver stage, a transmitter stage and optionally the AS routing behaviour.

3.1.29

idle

see "bus state".

Idle distinguishes 3 bus biasing states:

idle while all nodes are neither un-powered nor in a low power mode, thus all nodes are biasing the bus.

idle while all nodes are either un-powered or in a low power, thus none of the nodes is biasing the bus.

idle while some nodes are biasing the bus and others not.

3.1.30

leg

passive network that is involved in the calculation of *timing budget*

NOTE A topology is interpreted as a single path from a transmitter to a receiver that contains several passive networks. Each of these passive networks is named *leg*.

3.1.31

linear passive bus

FlexRay bus that consists of 2 terminated FlexRay nodes with one *cable* between

NOTE Additionally some un-terminated FlexRay nodes are plugged to the cable by *splices* and short *stubs*.

3.1.32

monolithic

see: *active star*.

NOTE This term is used to characterize various implementations on an AS. If the AS is *monolithic* implemented all specified components are included in a single device.

3.1.33

NoActivity

signal to the Central_Logic when this communication path is *idle* is detected (see also *Activity*)

3.1.34

non-monolithic

character of various implementations on an AS

NOTE This term is used to characterize various implementations on an AS. If the AS is *non-monolithic* implemented all specified components are not included in a single device, two devices are used at least. See "*active star*".

3.1.35

NotReceiveActive

communication path signals *NotReceiveActive* to the Central_Logic when a state is entered at that the *communication path* is idle or is actively transmitting data

3.1.36

parasitic capacity

capacity that appears although it is not technically necessary

EXAMPLE

pins of a device housing generate a capacity

3.1.37

parasitic resistance

resistance that appears although it is not technically necessary

3.1.38

passive net

all possible implementation of AS *branches*

NOTE This summarizes: point-to-point connections, linear busses and passive stars. They do not include BD/ASs.

3.1.39

passive star network

network consisting of passive stars

3.1.40

physical layer

component that includes all components between *TP0* and *TP5*

3.1.41

ReceiveActive

communication path signals *ReceiveActive* to the Central_Logic when a state is entered at that the incoming data stream is forwarded to other *communication paths*

3.1.42

receiver

device or entity that receives an information transfer originated by a transmitter

NOTE A term that is used in various ways based on the context.

EXAMPLE

BD's input stage from the bus.

FlexRay *communication element* receiving node

3.1.43

receive enable not

RxEN

output pin at the *BD* to show the state of the bus

NOTE Two states are distinguished: *idle* or *activity*

3.1.44

serial peripheral interface

SPI

synchronously working hardware interface to exchange data among circuits mounted on a *PCB*

3.1.45

signal integrity

SI

procedures or requirements to *differential* bus signals to guarantee the faultless transmission of FlexRay *communication elements*

3.1.46

signal integrity voting

SI voting

procedure to determine *Sq* based on measured *bus* signals

3.1.47

specific line delay

propagation of a FlexRay signal per meter of a transmission line in ns/m

3.1.48

splice

any implementation of a connection-point where 3 or more transmission lines are plugged together

NOTE A *splice* may contain passive components to damp radiation

EXAMPLE

A *splice* in a linear bus allows to connect a stub to a FlexRay node.

3.1.49

signal quality

Sq

parameter to describe whether the required *signal integrity* of FlexRay signals on the bus is met

NOTE Pass or fail are the possible results.

3.1.50

stochastic jitter

jitter of data stream edges in the time domain due to e.g. radiation

NOTE The EPL-specification passes its appropriate consideration to the responsible system designer.

3.1.51

stub

component within *passive nets*

NOTE A *stub* consists of a single FlexRay *cable* connected to the centre of a passive star or to a linear bus (short: plugged to a *splice*).

The *stub* ends at the BD pins BP and BM within a FlexRay node.

3.1.52

termination

set-up of components between a BD and a *transmission line*

NOTE Mainly they are used to ensure *SI* and *EMC* requirements.

EXAMPLE

Resistors, capacitances, chokes etc.

3.1.53

termination area (of the cables)

assembly of FlexRay *cables* to *ECU*-connectors that require several procedures which disturb the geometric integrity of the FlexRay *cable*:

untwisted, unshielded and unsheathed *cable* segment.

twisted but unshielded or unsheathed *cable* segment.

Both segments together represent the termination area.

3.1.54

test plane

virtual or real places to get electrical signals and to determine their properties

NOTE The *test planes* are located on the path from a transmitter to a receiver.

3.1.55

topology

non-hierarchical flat geometric structure of the FlexRay system

NOTE A distributed FlexRay system consists of several components like nodes, busses, active and passive stars etc.

3.1.56

test plane 0

TP0

virtual time reference point that represents the digital output from the protocol machine with a perfect timing according the data link layer specification

3.1.57

test plane 1 flip flop (virtual)

TP1_FFi

transmitting CC's virtual test plane to visualize PLL jitter, clock skew and propagation delay of the flip flop

3.1.58

test plane 1 flip flop

TP1_FF

transmitting CC's internal test plane at 'Q' pin of last flip flop before output buffer

3.1.59

test plane 1 communication controller

TP1_CC

transmitting CC's output pin (TxD)

3.1.60

test plane 1 bus driver input

TP1_BD

test plane located at the transmitting *BD*'s input pin *TxD* directly

3.1.61

test plane 1 bus driver (virtual)

TP1_BDi

virtual test plane hidden in the transmitting *BD*'s output of its *TxD* logical state detection stage

3.1.62

test plane 1

TP1

test plane located at the transmitting *BD*'s output pins *BP* and *BM*

3.1.63

test plane 2

TP2

test plane located at the transmitting *ECU* connector's terminals to the wiring harness

3.1.64

test plane 3

TP3

test plane located at the receiving *ECU* connector's terminals from the wiring harness

3.1.65

test plane 4

TP4

test plane located at the receiving *BD*'s input pins *BP* and *BM*

3.1.66

test plane 4 bus driver (virtual)

TP4_BDi

virtual test plane hidden in the receiving *BD*'s output of its differential bus signal logical level detection stage

3.1.67

test plane 4 bus driver

TP4_BD

receiving *BD*'s output pin (RxD)

3.1.68

test plane 4 communication controller

TP4_CC

test plane located at the receiving *CC*'s input pin *RxD*

3.1.69

test plane 4 communication controller (virtual)

TP4_CCi

virtual test plane hidden in the receiving *CC*'s output of its *RxD* logical state detection stage

3.1.70

test plane 4 flip flop

TP4_FF

receiving *CC*'s internal test plane at 'D' pin of first flip flop after input buffer

3.1.71

test plane 4 flip flop (virtual)

TP4_FFi

receiving CC's virtual test plane to visualize PLL jitter, clock skew and propagation delay of the flip flop

3.1.72

test plane 5 communication controller

TP5_CC

clock input to CC

3.1.73

test plane 5

TP5

virtual test plane that represents the input of the decoding algorithm with a perfect timing according the data link layer specification

3.1.74

test plane 11

TP11

test plane located at the transmitting AS device's output pins *BP* and *BM*

3.1.75

test plane 12

TP12

test plane located at the transmitting AS *ECU* connector's terminals to the wiring harness

3.1.76

test plane 13

TP13

test plane located at the receiving AS *ECU* connector's terminals from the wiring harness

3.1.77

test plane 14

TP14

test plane located at the receiving AS device's input pins *BP* and *BM*

3.1.78

transmission line

FlexRay *cable* or a line on a PCB when their properties to transmit electrical signals are focused

3.1.79

transmission start sequence

TSS

bit sequence that is sent in front of each FlexRay data frame or CAS/MTS symbol. The *TSS* is necessary for a *BD* and an *AS* to detect *activity* on the bus. A *BD* and an *AS* is allowed to shorten or lengthen the *TSS*.

3.1.80

transmitter

term that is used in various ways based on the context

EXAMPLE

BD's output stage to the bus.
FlexRay traffic transmitting node

3.1.81

wiring harness

all components inside the component "vehicle wiring harness" to transmit FlexRay *communication elements*

NOTE This includes connectors to plug *ECUs*, in-line connectors, *cables*, *splices* etc.

3.2 Abbreviated terms

AC	alternating current
APM	autonomous power moding
AS	active star
AS_BGI	active star – bus guardian interface
AS_IVR	active star – internal voltage regulator
AS_VRC	active star – voltage regulator control
ASP	abstract service primitive
BD	bus driver
BD_VRC	bus driver – voltage regulator control
BD_BGCI	bus driver – bus guardian control interface
BD_IVR	bus driver – internal voltage regulator
BD_LLA	bus driver – logic level adaptation
BG	bus guardian
BGE	bus guardian enable
BM	bus minus
BP	bus plus
C	capacitor
CC	communication controller
CE	communication element
CHI	controller host interface
CMC	common mode choke
DUT	device under test
ECU	electronic control unit
EMC	electromagnetic compatibility
EN	optional/product specific mode control signals of the bus driver
ERRN	error not output pin of the <i>BD/AS</i> This pin allows the <i>BD/AS</i> signalling error events or/and errors.
I/R	interruption
Idle_LP	bus state in case all nodes (and active stars) are in a low power mode

INH	inhibit output pin of the <i>BD/AS</i> INH signals on one hand the <i>BD/AS</i> state and allows on the other hand to control the states of a voltage regulator.
INH1	inhibit 1 output signal of the bus driver / active star
INTN	interrupt not
IUT	implementation under test
LWU	local wakeup
PCO	point of control and observation
PDU	protocol data unit
PL	physical layer
PS	passive star
RWU	remote wakeup
RxD	receive data signal from the bus driver
RxEN	receive data enable not signal from the bus driver
S/C	short-circuit
SCSN	SPI chip select not input
SI	signal integrity
SOVS	system operating variable space
SPI	serial peripheral interface
Sq	signal quality
STBN	standby not Input pin at the <i>BD</i> to control its power modes
SUT	system under test
SV	supervisor
TCP	test coordination procedure
TP	test plane
TSS	transmission start sequence
TxD	transmit data signal to the bus driver
TxEN	transmit data enable not signal Output pin at the <i>CC</i> and input pin at the <i>BD</i> . The pin allows the <i>CC</i> to control the states which are generated by the <i>BD</i> . Two states are distinguished: <i>idle</i> or <i>activity</i> .
U _{GS}	ground shift voltage

WAKE local wakeup input signal of the bus driver

WU wakeup

3.3 Symbols

R_T Resistor to terminate a transmission line

X don't care. This term is used when the state of a signal is not relevant.

V_{BAT} supply voltage (battery)
Voltage of the vehicle battery measurable at *BD*'s pins.

V_{CC} supply voltage (+5 V)

V_{DIG} supply voltage for the digital I/O ports
This term is used in two ways, *BD*'s pin to connect the logical 1 reference voltage and voltage value of the logical 1 reference voltage.

V_{IO} supply voltage for the digital I/O ports
This term is used in two ways, *BD*'s pin to connect the logical 1 reference voltage and voltage value of the logical 1 reference voltage.

$V_{StarSupply}$ supply voltage of the active star
Can be derived from V_{BAT} and/or V_{CC}

4 Document reference according to OSI model

Figure 1 depicts the FlexRay document reference according to OSI model.

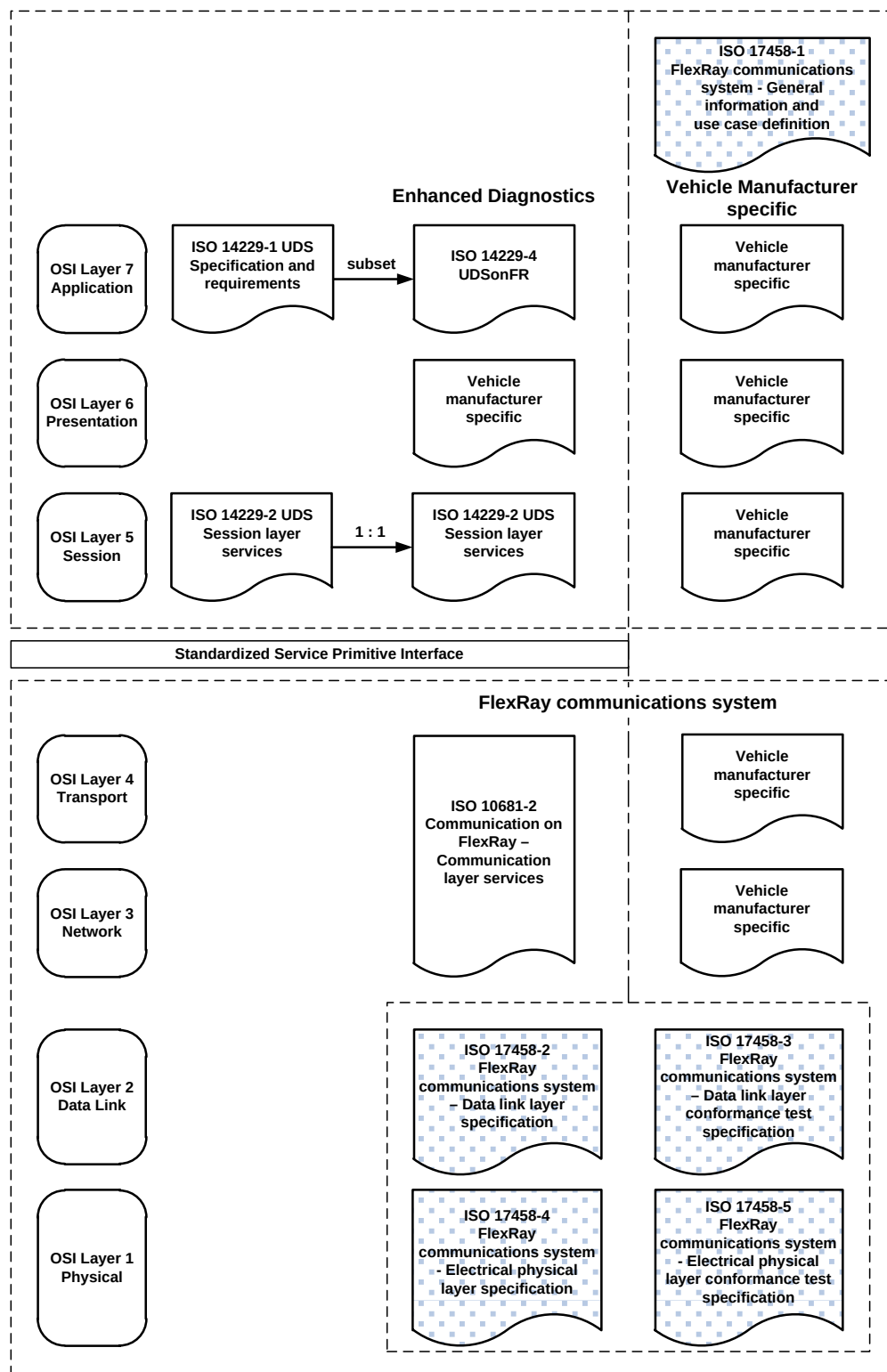


Figure 1 — FlexRay document reference according to OSI model

5 Conventions

5.1 General

ISO 17458, ISO 10681 and ISO 14229-4 are based on the conventions specified in the OSI Service Conventions (ISO/IEC 10731) as they apply for physical layer, protocol, network & transport protocol and diagnostic services.

5.2 Notational and parameter prefix conventions

Each FlexRay parameter is prefaced by two prefixes. The prefixes are applied in the following way:

<variable> ::= <prefix_1> <prefix_2> Name

<prefix_1> ::= a | c | v | g | p | z

<prefix_2> ::= d | l | n | s | u

Table 2 defines the values for prefix 1.

Table 2 — Prefix 1

Naming Convention	Information Type	Description
a	Auxiliary Parameter	Auxiliary parameter used in the definition or derivation of other parameters or in the derivation of constraints.
c	Protocol Constant	Values used to define characteristics or limits of the protocol. These values are fixed for the protocol and cannot be changed.
v	Node Variable	Values that vary depending on time, events, etc.
g	Cluster Parameter	Parameter that shall have the same value in all nodes in a cluster, is initialized in the <i>POC:default config</i> state, and can only be changed while in the <i>POC:config</i> state.
p	Node Parameter	Parameter that may have different values in different nodes in the cluster, is initialized in the <i>POC:default config</i> state, and can only be changed while in the <i>POC:config</i> state.
z	Local SDL Process Variable	Variables used in SDL processes to facilitate accurate representation of the necessary algorithmic behaviour. Their scope is local to the process where they are declared and their existence in any particular implementation is not mandated by the protocol.
—	—	<i>prefix_1</i> can be omitted for physical layer parameters.
NOTE This table is mirrored from ISO 17458-2, where the binding definitions are made.		

Table 3 defines the values for prefix 2.

Table 3 — Prefix 2

Naming Convention	Information Type	Description
d	Time Duration	Value (variable, parameter, etc.) describing a time duration, the time between two points in time.
l	Length	Physical length of e.g. a cable
n	Amount	Number of e.g. stubs
s	Set	Set of values (variables, parameters, etc.).
u	Voltage	Differential voltage between two conducting materials (e.g. copper wires)
NOTE The prefixes "l", "n" and "u" are defined binding here. For all other prefixes refer to ISO 17458-2.		

5.3 Important preliminary notes

5.3.1 Bus speed

The FlexRay communication system was specified focusing on a data rate of 10 Mbit/s.

This physical layer shall only be used for data rates in the range from 2,5 Mbit/s to 10 Mbit/s.

NOTE The 500 ppm crystal is used to allow electrical physical layer including one active star at 10 Mbit/s. The 1 500 ppm crystal is used to estimate the worst case clock accuracies etc. at any baud rate in ISO 17458-2.

5.3.2 Conformance tests

The conformance test for physical layer devices as specified in this specification is defined in ISO 17458-5.

For the static test cases of the conformance test every EPL parameter shall be pointed out in the BD/AS data sheet by using the EPL-naming conventions (optionally according to in-house naming convention) and the EPL measurement conditions.

In case other than the EPL parameter names are used, the data sheet shall contain a comparison table including the parameter names (EPL versus product) and the values. A proposal for such a table is given in ISO 17458-5.

5.3.3 Conformance test of FlexRay communication controllers

The test of the CC interface to the physical layer as specified in Clause of this part of ISO 17458 is part of the protocol conformance test.

6 Communication channel basics

6.1 Objective

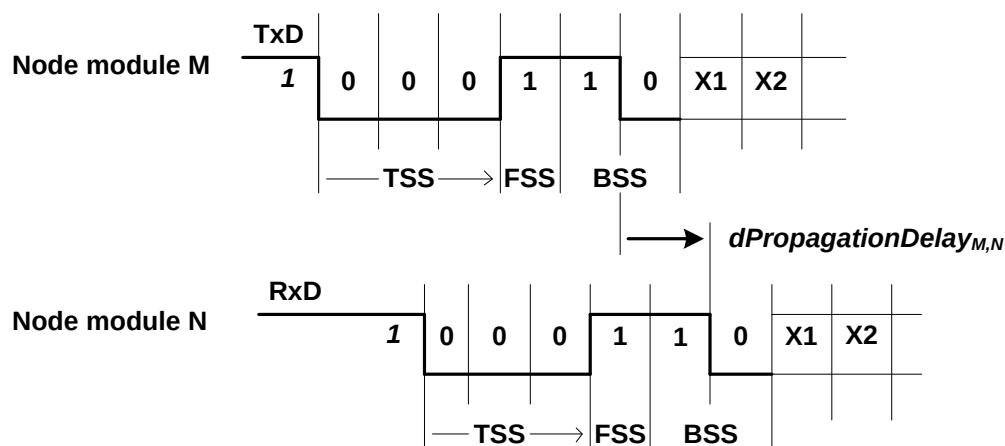
The electrical physical layer provides among other things an implementation of a FlexRay communication channel. This subclause defines an abstract of the physical properties of the communication channel.

Any physical layer that behaves according to these basics provides a valid FlexRay communication channel.

6.2 Propagation delay

Binary data streams transmitted from node module M are received at node module N with the propagation delay $dPropagationDelay_{M,N}$. The propagation delay shall be measured from the falling edge in the first Byte Start Sequence (BSS; see ISO 17458-2) in the transmit (TxD, TP1_BD) signal of node module M to the corresponding falling edge in the receive (RxD, TP4_BD) signal of node module N.

Figure 2 depicts the propagation delay.



Key

- BSS Byte start sequence
- FSS Frame start sequence
- TSS Transmission start sequence
- TxD Transmission
- RxD Reception

Figure 2 — Propagation delay

The actual propagation delay that occurs between two node modules M and N depends mainly on the topology of the path.

Table 4 defines the propagation delay.

Table 4 — Propagation delay

Name	Description	Min	Max	Unit
$dPropagationDelay_{M,N}$	Propagation delay from TP1_BD ^a of node module M to TP4_BD ^a of node module N	—	2 450	ns
^a For definition of "TP1_BD" and "TP4_BD", see Clause 10.				

6.2.1 Asymmetric delay

As defined above the propagation delay is defined with in relation to the first negative edge after the TSS in the binary data stream.

Due to the limitations of the FlexRay decoder module the channel plus the sending and receiving bus driver shall not introduce a static asymmetric delay that exceeds a certain level.

Definitions of maximum asymmetric delay portions can be found in 10.5. For further considerations see Annex A.

Figure 3 depicts the asymmetric propagation delay.

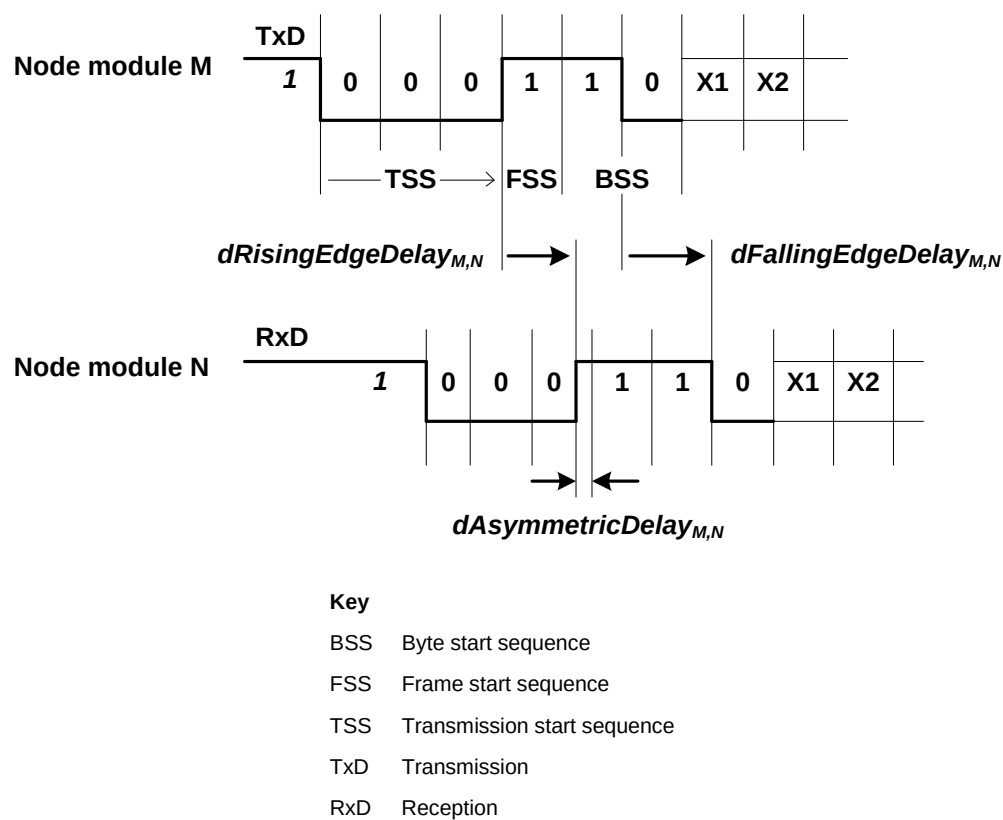


Figure 3 — Asymmetric propagation delay

$$dAsymmetricDelay_{M,N} = dRisingEdgeDelay_{M,N} - dFallingEdgeDelay_{M,N}$$

In case the rising edge is late, relative to the falling edge, the resulting asymmetry has a positive sign.

6.3 Frame TSS length change

The channel may truncate the TSS (see ISO 17458-2), but also may slightly lengthen the TSS. The interval by which the TSS length is changed from a transmitting node module M to a receiving node module N is denoted as $dFrameTSSLengthChange_{M,N}$. The effect of Frame TSS length change is shown in Figure 4.

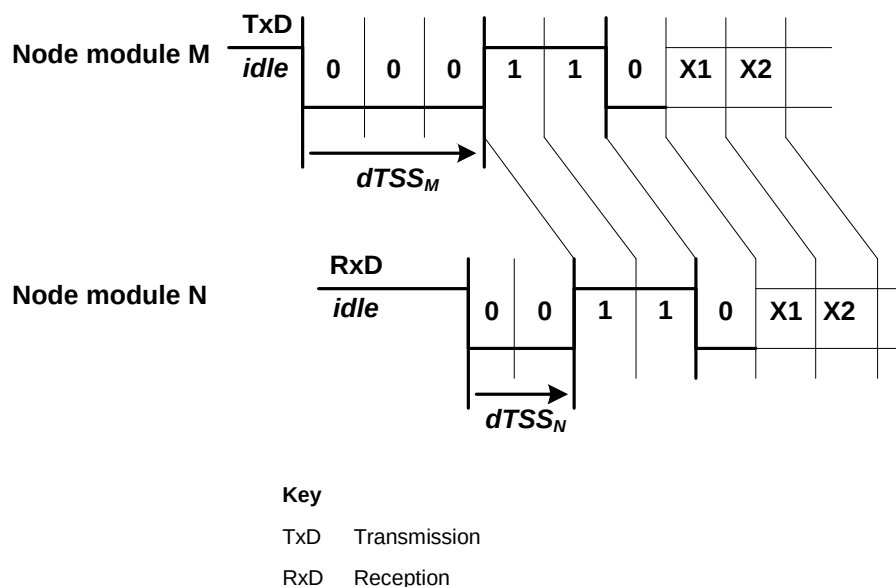


Figure 4 — Frame TSS length change

The length change is calculated as the difference of the duration of TSS at the receiver and duration of TSS at the sender: $dFrameTSSLengthChange_{M,N} = dTSS_N - dTSS_M$. Thus positive values would indicate that the TSS was lengthened.

The absolute maximum value of $dFrameTSSLengthChange_{M,N}$ needs to be less than the maximum configurable value of the protocol parameter $gdTSSTransmitter$. The effect of TSS length change sums up of different portions, which are contributed by active stars and the activity detection in the receiving bus drivers.

Table 5 defines the frame TSS length change.

Table 5 — Frame TSS length change

Name	Description	Min	Max	Unit
$dFrameTSSLengthChange_{M,N}$	TSS Length change from TP1_BD ^a of node module M to TP4_BD ^a of node module N	-1300	50	ns
NOTE The TSS length change depends on the number of active stars in the path from node M to node N. More detailed information is given in Annex A.				
^a For definition of "TP1_BD" and "TP4_BD", see Clause 10.				

6.4 Symbol length change

Quite similar to the length change of the TSS the length of symbols is changed while travelling through the physical layer. Besides the length change at the beginning by the activity detection time a lengthening at the end by the idle detection time occurs. More detailed information is given in Annex A.

Figure 5 depicts the symbol length change.

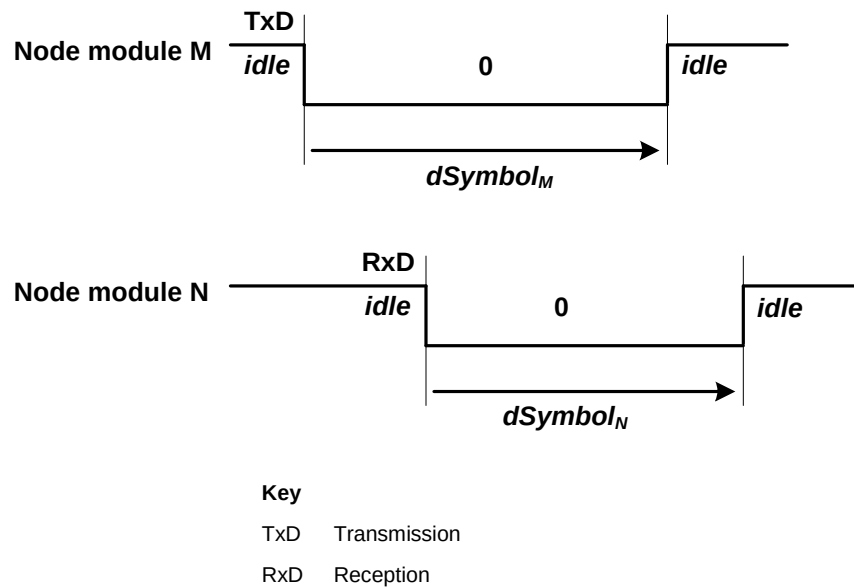


Figure 5 — Symbol length change

The length change is calculated as the difference of the duration of the symbols at the receiver and duration of the symbol at the sender: $dSymbolLengthChange_{M,N} = dSymbol_N - dSymbol_M$.

Table 6 defines the symbol length change.

Table 6 — Symbol length change

Name	Description	Min	Max	Unit
$dSymbolLengthChange_{M,N}$	Change of length of a symbol on path from TP1_BD ^a of node module M to TP4_BD ^a of node module N	-925	1 125	ns
NOTE A negative value means that the symbol is shortened; a positive value means the symbol is lengthened.				
^a For definition of "TP1_BD" and "TP4_BD", see Clause 10.				

6.5 FES1 length change

The last two bits in a FlexRay frame are called FES (Frame End Sequence). The last bit (FES1) is logical HIGH. This period of the FES1 is likely to be lengthened by active stars. For detailed information see 13.3. Besides the prolongation of the FES1 there is the chance that ringing occurs. For further information about ringing after frame and symbol end see Annex A.

6.6 Collisions

FlexRay is designed to perform communication without collisions. I.e. the nodes do not arbitrate on the channel and collisions do not happen during normal operation. However, during the startup phase of the protocol, collisions on the channel may happen. The electrical physical layer does not provide a means to resolve those collisions.

In case of collisions of communication elements on the bus (at least two nodes are transmitting different data simultaneously) it cannot be predicted what signal the nodes will receive. The received bus signal can also change within one bit time.

Table 7 defines the data signal collision on the bus.

Table 7 — Data signal collision on the bus

Transmitter 1	Transmitter 2	Resulting bus signal
<i>Data_0</i>	<i>Data_0</i>	<i>Data_0</i>
<i>Data_0</i>	<i>Data_1</i>	<i>Data_0</i> or <i>Data_1</i> or <i>Idle</i>
<i>Data_1</i>	<i>Data_0</i>	<i>Data_1</i> or <i>Data_0</i> or <i>Idle</i>
<i>Data_1</i>	<i>Data_1</i>	<i>Data_1</i>
<i>Idle</i>	<i>Data_0/Data_1</i>	<i>Data_0/Data_1</i>
<i>Data_0/Data_1</i>	<i>Idle</i>	<i>Data_0/Data_1</i>
NOTE For the definitions of <i>Data_0</i> , <i>Data_1</i> and <i>Idle</i> see Clause 6.		

6.7 Stochastic jitter

6.7.1 Introduction

Injection of RF fields results in a certain jitter portions seen in the RxD signal at receiving nodes. These different portions have been investigated and the results for systems with two active stars per channel are documented in the following subclauses. These values are not subject to the physical layer conformance test.

6.7.2 Stochastic jitter on data edges

Jitter on edges in the RxD signal, which are different from first transition from HIGH to LOW (start of frame) and the last transition from LOW to HIGH (the end of a frame), shall be considered in the course of system evaluation. See Annex A for further information about the allowable EMC jitter in specific network topologies.

6.7.3 Stochastic jitter on TSS length change

Jitter on the TSS length might lengthen or shorten the TSS additionally to the length change as described in 6.3. Further information is given in Annex A.

6.7.4 Stochastic jitter on symbol length change

The summation of jitter on the falling and rising edges of symbols might lead to deviations of the symbol length change as described in 6.4. Further information is given in Annex A.

6.8 Wakeup patterns

6.8.1 Overview

Independent from the data rate at least two wakeup symbols constitute a wakeup pattern. Such patterns shall wake bus drivers that implement the option 'BD voltage regulator control' and active stars that are in a low power mode.

6.8.2 Standard wakeup pattern

For remote wakeup in FlexRay systems, a wakeup pattern is sent via the bus as described in ISO 17458-2. The FlexRay wakeup pattern consists of at least two FlexRay wakeup symbols.

The wakeup symbol is defined as a phase of *Data_0* followed by a phase of *Idle*.

A valid remote wakeup event is the reception of at least two consecutive wakeup symbols via the bus.

A remote wakeup event occurs from bus drivers or active stars perspective when any sequence of

$\{ \text{Data_0}, \text{Idle}, \text{Data_0}, \text{Idle} \}$

that starts after *Idle* and has a timing according to Figure 6 is received.

The receiver shall detect wakeup patterns with the timing:

$dWU_{Phase0} > 4 \mu\text{s}$, $dWU_{Phase1} > 4 \mu\text{s}$, $dWU_{Phase2} > 4 \mu\text{s}$, $dWU_{Phase3} > 4 \mu\text{s}$, $dWU_{Phase4} > 4 \mu\text{s}$ and $dWU < 49 \mu\text{s}$.

The dWU consists of the minimum value for the detection timeout of the Data_0 phase $dWU_{0Detect}$ (which is $1 \mu\text{s}$) and the minimum of the wakeup acceptance timeout $dWU_{Timeout}$ (which is $48 \mu\text{s}$). A detailed description of the wakeup mechanism is given in 12.11.3.

Figure 6 depicts the valid signal for wakeup pattern recognition at receivers.

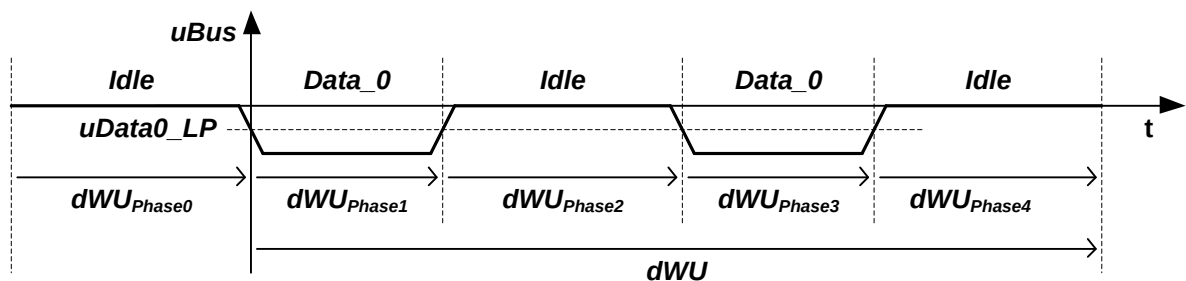


Figure 6 — Valid signal for wakeup pattern recognition at receivers

6.8.3 Alternative wakeup patterns

Other patterns as the above mentioned will also let the wakeup state machine (see 12.11.3) initiate a wakeup.

In the WUDOP ISO 17458-2 wakeup pattern the *Idle* phases of the standard wakeup pattern are replaced by *Data_1* phases. The timing requirements do not change. Such patterns can advantageously be used during the symbol window.

Figure 7 depicts the alternative wakeup pattern recognition at receivers.

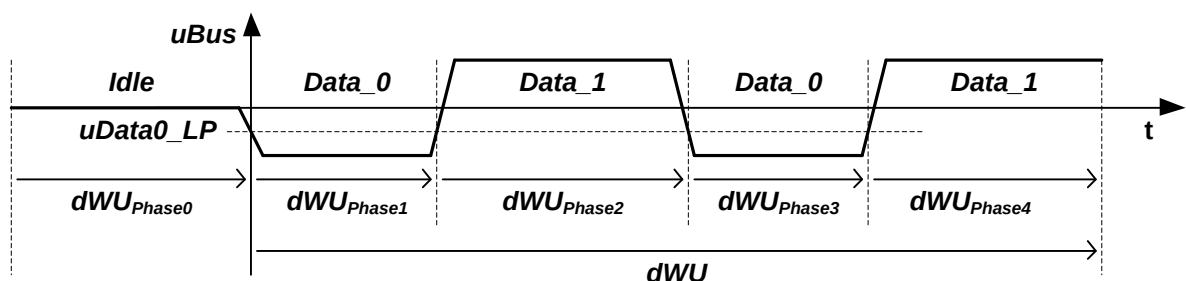


Figure 7 — Alternative wakeup pattern recognition at receivers

7 Principle of FlexRay networking

7.1 Objective

This Clause shows the basic operation principle of FlexRay networks.

7.2 Interconnection of nodes

The FlexRay electrical physical layer provides a differential voltage link (= bus) between a transmitting and one or more receiving communication modules. The differential voltage is measured between two signal lines, denoted BP (Bus Plus) and BM (Bus Minus) as defined in 7.3. The fundamental mechanism of the bidirectional differential voltage link is shown below. The bidirectional link between any two node modules requires a transmitter and receiver circuit, which are integrated in so called bus drivers.

Figure 8 depicts the principle of a differential voltage link.

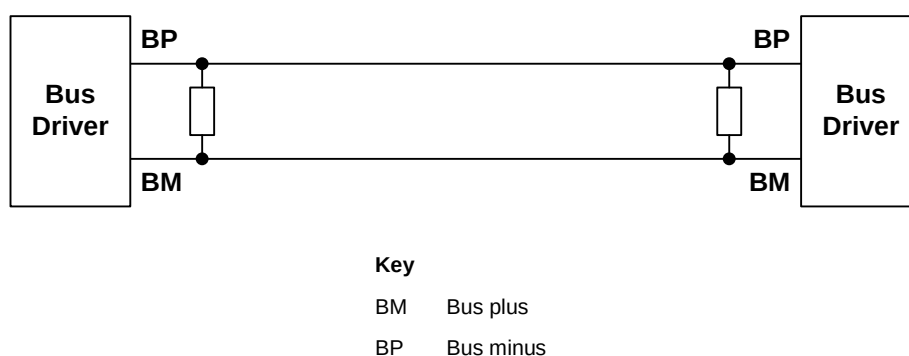


Figure 8 — Principle of a differential voltage link

This structure, which is named 'point-to-point connection' in Clause 9, can be extended with further bus drivers that are connected to the differential voltage link as depicted in Figure 9. A dual wire cable implements the differential voltage link. With each communication module one bus driver is added to the system, as shown in Figure 9.

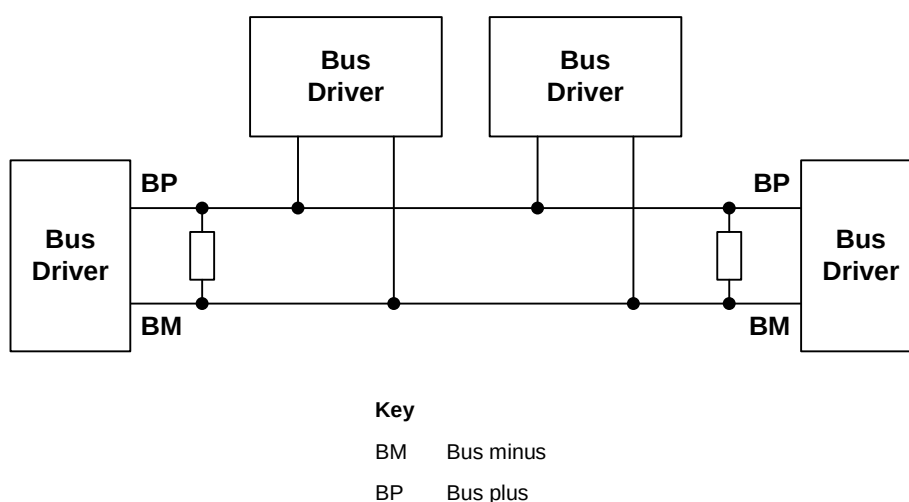


Figure 9 — Principle of a linear passive bus

The complete variety of possible topologies is defined in Clause 9.

Furthermore, the bus can also comprise active stars, which are working in principle as bidirectional repeaters. The functionality of active stars is specified in Clause 13.

Figure 10 depicts the principle of an active star network.

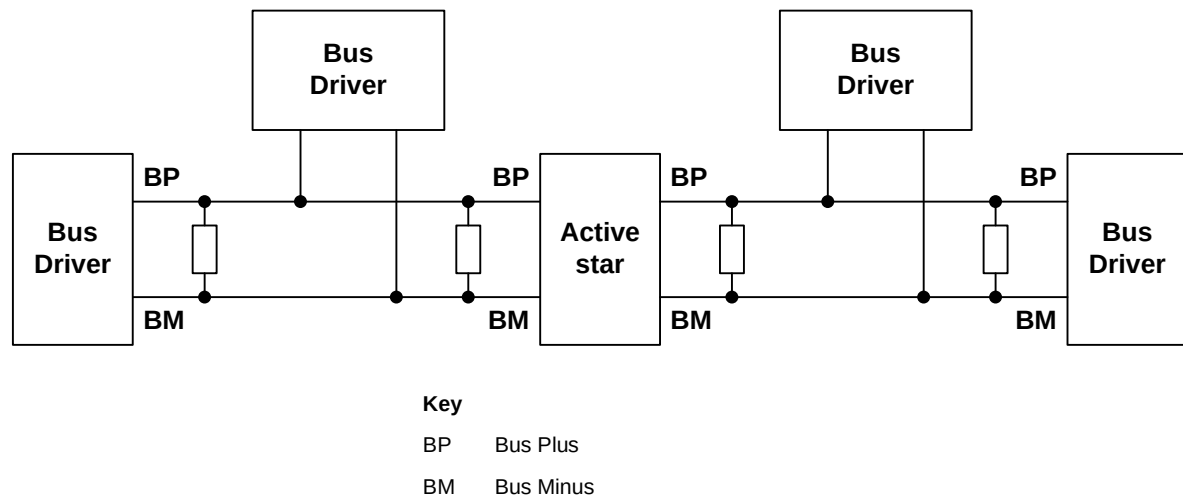


Figure 10 — Principle of an active star network

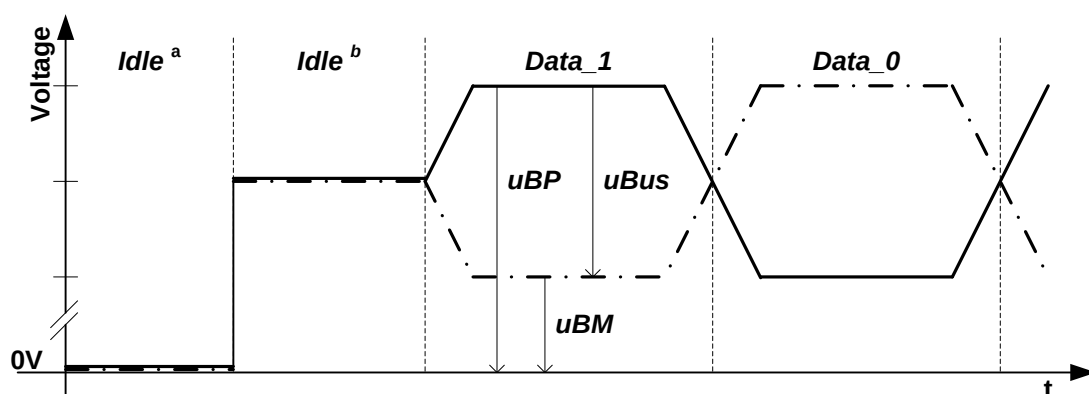
7.3 Electrical signalling

7.3.1 Overview

The bus may assume three different bus states, denoted as *Data_0*, *Data_1* and *Idle*.

A principle voltage level scheme is depicted in the following figure. The bus wires are denoted as BP and BM. Consequently the voltages on the wires (measured to ground) are denoted u_{BP} and u_{BM} . The differential voltage on the bus is defined as $u_{Bus} = u_{BP} - u_{BM}$.

Figure 11 depicts the electrical signalling.



- a In case all nodes (and active stars) are in a low power mode
- b in case no node (and no active star) is in a low power mode

Figure 11 — Electrical signalling

7.3.2 Bus state: Idle

To leave the bus in *Idle* state, no current is actively driven to BP or to BM. The connected bus drivers are biasing both BP and BM to a certain voltage level depending on their operating mode (see Table 49), i.e. in case all nodes (and active stars, if connected) are in a low power mode no bias voltage is applied to the bus wires. In case no node (and no active star, if connected) is in a low power mode the nominal bias voltage is 2 500 mV.

In case some of the nodes are in a low power mode and others are not, the resulting bias voltage on the bus wires will be less than 2 500 mV.

7.3.3 Bus state: Data_1

To drive the bus to *Data_1* at least one BD forces a positive differential voltage between BP and BM.

7.3.4 Bus state: Data_0

To drive the bus to *Data_0* at least one BD forces a negative differential voltage between BP and BM.

Figure 12 depicts the differential electrical signalling.

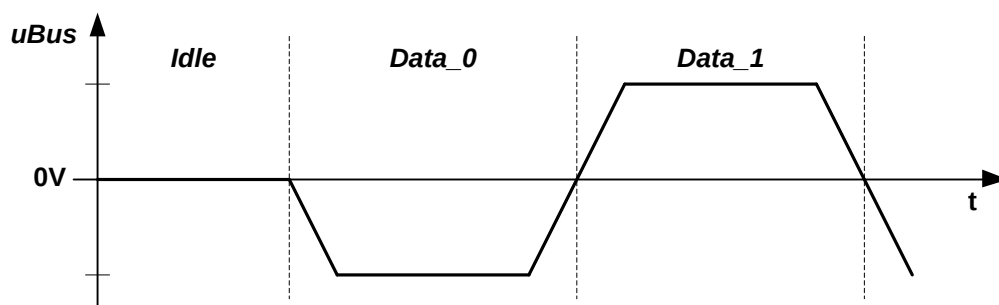


Figure 12 — Differential electrical signalling

8 Network components

8.1 Objective

This Clause introduces some basic network components that are used to build up FlexRay networks.

8.2 Cables

The objective of this subclause is to specify the required cable characteristics, but not to define a selection of cable types. The medium in use for FlexRay busses may be unshielded as well as shielded cables, as long as they provide the characteristics defined in Table 8.

Table 8 — Cable characteristics

Name	Description	Min	Max	Unit
Z_0	Differential mode impedance at 10 MHz ^a	80	110	Ω
T'_0	Specific line delay	3,4	10	ns / m
^a See Annex A.				

Cable attenuation and delay depend on temperature and frequency, but might also depend on more environmental conditions. The system integrator has to select the cable so that the receiver requirements at TP4 are fulfilled.

8.3 Connectors

This specification does not prescribe certain connectors for FlexRay systems. However, any electrical connector used in FlexRay busses shall meet the constraints defined in Table 9.

Table 9 — Connector parameters

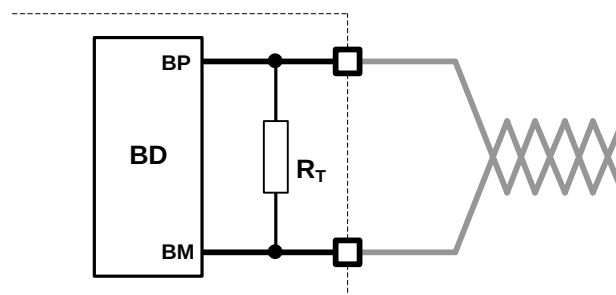
Name	Description	Min	Max	Unit
$R_{DCContact}$	Contact resistance (including crimps)	—	50	m Ω
$Z_{Connector}$	Impedance of connector	70	200	Ω
$l_{Coupling}$	Length coupling connection ^a	—	150	mm
$dContactInterruption$ ^b	Duration of contact interruption. Contact resistance $R_{DCContact} > 1 \Omega$	—	100	ns
NOTE See further recommendations about connectors in Annex A.				
^a this parameter defines the length of the connectors including the termination areas of the cables.				
^b this requirement is to be generally understood as a quality issue and has no direct link with the timing performance of FlexRay.				

8.4 Cable termination

8.4.1 Terminated cable end

The simplest way to terminate the cable at an ECU consists of a single termination resistor between the bus wires BP and BM. Other termination possibilities are shown in Annex A.

Figure 13 depicts the terminated cable end.



Key

BD Bus driver

BM	Bus minus
BP	Bus plus
R_T	Termination resistance

Figure 13 — Terminated cable end

In following subclauses, ECUs that have this kind of termination are symbolized with the following icon.

Figure 14 depicts the symbol for a terminated cable end.

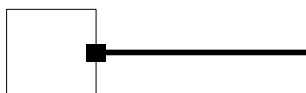


Figure 14 — Symbol for a terminated cable end

8.4.2 Un-terminated cable end

At an un-terminated cable end, no resistive element is connected between the bus wires.

Figure 15 depicts the un-terminated cable end.

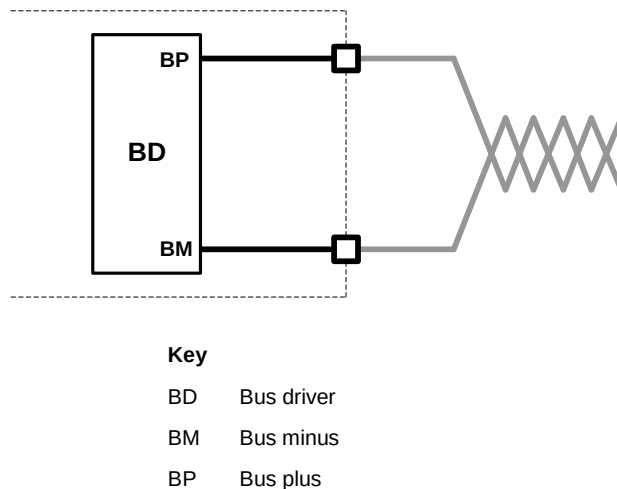


Figure 15 — Un-terminated cable end

In the following subclauses, ECUs that have this kind of termination are symbolized with the following icon.

Figure 16 depicts the symbol for an un-terminated cable end.

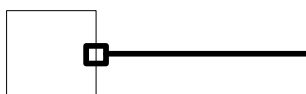


Figure 16 — Symbol for an un-terminated cable end

8.5 Termination concept

This specification does not prescribe a certain termination concept. Application specific solutions have to be applied. Some more general recommendations about cable termination can be found in Annex A.

8.6 Common mode chokes

This specification does not prescribe a certain common mode choke for FlexRay systems. However, any common mode choke used in FlexRay systems shall meet the following constraints over the entire temperature range as specified in 15.7.

Table 10 defines the common mode choke parameters.

Table 10 — Common mode choke parameters

Name	Description	Min	Max	Unit
R_{CMC}	Resistance (per line)	—	2	Ω

See further recommendations about common mode chokes in Annex A.

8.7 DC bus load

The DC load a BD sees between the bus wires is R_{DCLoad} .

A network equivalent DC circuit is as follows:

Figure 17 depicts the DC bus load.

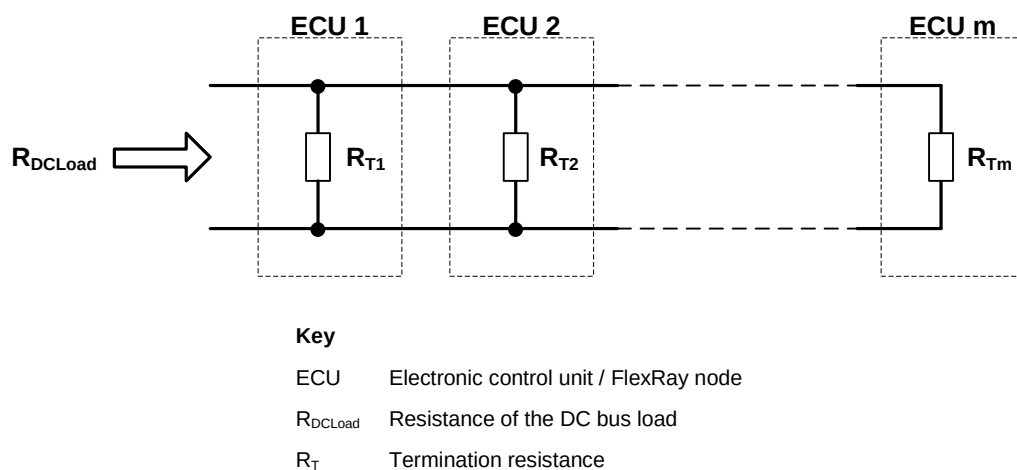


Figure 17 — DC bus load

The schematic does not include parasitic resistances from common mode chokes (R_{CMC}), connectors ($R_{Connector}$) and the series resistance of the wiring (R_{Wire}), since those shall be neglected in the following calculation:

The formula to calculate the overall DC bus load is shown in Equation 1.

$$R_{DCLoad} = \left(\sum_m \frac{1}{R_{Tm}} \right)^{-1} \quad (1)$$

where

R_{DCLoad} is the DC bus load;

R_{Tm} is the termination resistance of ECU m .

Table 11 defines the DC bus load limitation.

Table 11 — DC bus load limitation

Name	Description	Min	Max	Unit
R_{DCLoad}	DC bus load	40	55	Ω

Mind that the termination resistance R_{Tm} is usually a termination resistor in parallel to the BD's receiver common mode input resistance (see 12.9.5). The termination resistor might also be applied outside the ECU, e.g. at a network splice. In case of an un-terminated cable end, according to 8.4.2., the resistance R_{Tm} represents only the BD's receiver common mode input resistance.

Some exemplary termination concepts for different bus structures are described in Annex A. All termination concepts have to consider the DC bus load limitation as defined here.

9 Network topology

9.1 Objective

This Clause introduces possible bus structures, their names and parameters. The layout of busses has to follow the constraints that are explained in this Clause. Application examples and recommendations are given in Annex A.

Dual channel applications, a main feature of FlexRay, are discussed at the end of this Clause.

All FlexRay topologies are 'linear', which means that they are free from rings or closed loops respectively.

A termination concept has to be found for each topology implementation individually. General hints can be found in Annex A. Whether a topology/termination combination composes a valid FlexRay network, or not, has to be judged according to the signal integrity requirements as given in Clause 11.

9.2 Point-to-point connection

The point-to-point configuration is shown in Figure 18. It represents the simplest bus and can be regarded as the basic element for the construction of more complex busses. For simplicity, the two-wire bus is shown as one thick line in the figures of this document.

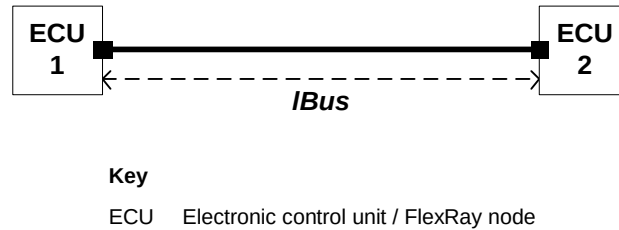


Figure 18 — Point-to-point connection

Practical limitations for *IBus* depend on factors like cable type and EMC disturbances.

Examples of practical values are given in Annex A, where also consideration about EMC robustness can be found in a separate subclause.

9.3 Passive star

For connecting more than two ECUs a passive star structure can be used, which is a special case of a linear passive bus that is described in the following subclause. At a passive star all ECUs are connected to a single splice. The principle of a passive star network is shown in Figure 19.

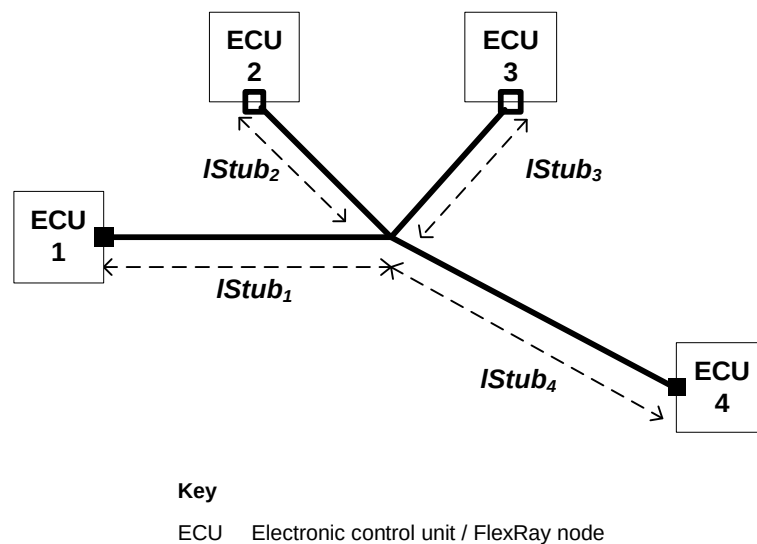


Figure 19 — Example of a passive star

Table 12 defines the parameters of a passive star.

Table 12 — Parameters of a passive star

Name	Description	Min	Max	Unit
$nSplice$	Number of splices ^a	1	1	—
^a If $nSplice$ is 0, then refer to 9.2, if $nSplice$ is greater than 1, then refer to 9.4.				

Practical limitations for $nStub$ and $IStub_N$ depend on each other and depend also on other factors like cable type and termination concept; i.e. a passive star with $nStub = 22$ and each $IStub = 12$ m for each stub is likely not to be operable.

Examples of practical values are given in Annex A, where also consideration about EMC robustness can be found in a separate subclause.

9.4 Linear passive bus

A structure without rings and without active elements is called "linear passive bus". The number of stubs is $nStub$. The length of a stub is $IStub_i$. The bus distance between two splices is denoted as $ISpliceDistance_{M,N}$. More than one stub may end at one splice. The number of splices is $nSplice$.

Figure 20 depicts the example of a linear passive bus.

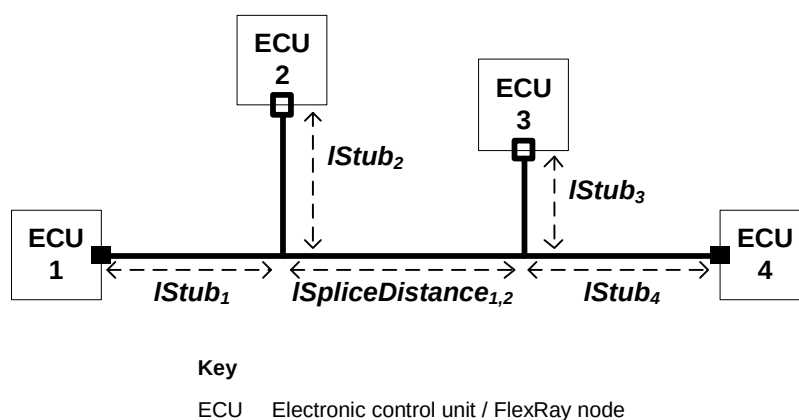


Figure 20 — Example of a linear passive bus

Table 13 defines the parameters of a linear passive bus structure.

Table 13 — Parameters of a linear passive bus structure

Name	Description	Min	Max	Unit
$nSplice$	Number of splices ^a	2	—	—
^a If $nSplice$ is 0, then refer to 9.2, if $nSplice$ is 1, then refer to 9.3.				

The parameters $IStub_i$, with $i = 1 \dots nStub$, are limited implicitly by the requirements of signal integrity.

Limitations for $nStub$, $nSplice$, $ISpliceDistance_{M,N}$ and $IStub_i$ depend on each other and further factors, like the chosen termination concept and cable type.

Examples of practical values are given in Annex A, where also consideration about EMC robustness can be found in a separate subclause.

9.5 Active star network

The active star network uses point-to-point connections between active stars and ECUs. The number of branches at an active star is $nActiveBranches$. The length of a branch is $IActiveStar_n$. The active star to which the ECUs are connected has the function to transfer data streams on one branch to all other branches. Since the active star device has a transmitter and receiver circuit for each branch, the branches are actually electrically decoupled from each other. The active star is specified in detail in Clause 13.

Figure 21 depicts the example of an active star network.

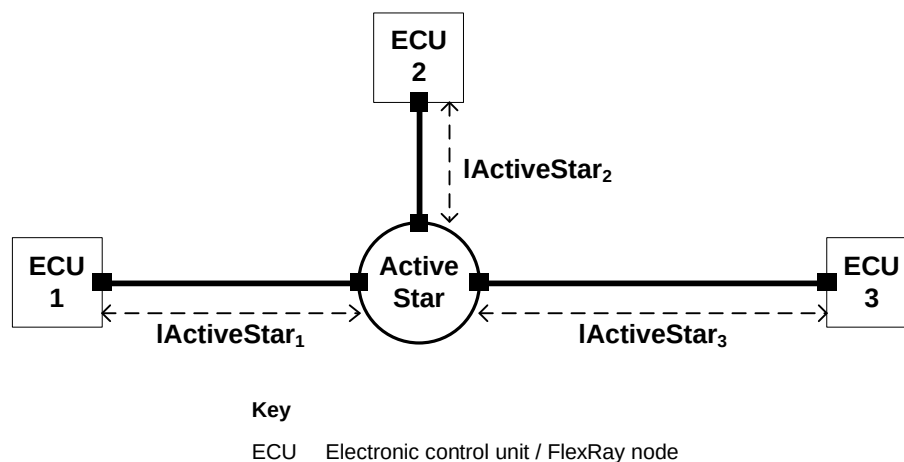


Figure 21 — Example of an active star network

Table 14 defines the limitations of active star networks.

Table 14 — Limitations of active star networks

Name	Description	Min	Max	Unit
$nActiveBranches$	Number of branches at an active star	2	—	—

An active star with only two branches may be considered as a degenerated star, a relay or hub for increasing overall bus length. Another reason for applying such active stars might be to take advantage of the fault containment behaviour of the active star between two linear passive busses. See Clause 13 for detailed information about the active star.

A branch of an active star may also be connected to a linear passive bus or a passive star. For these kinds of bus structures and their restrictions see 9.3. and 9.4.

A branch of an active star may also be connected to a second active star. For these kinds of bus structures and their restrictions see 9.6.

Examples of practical values are given in Annex A, where also consideration about EMC robustness can be found in a separate subclause.

9.6 Cascaded active stars

Active stars can be cascaded in systems that operate with 2,5 Mbit/s and 5 Mbit/s. This means two active stars are connected to each other with a point-to-point connection. A data stream that is sent from an ECU M to an ECU N passes $nStarPath_{M,N}$ active stars while being conveyed on the bus.

Chosen topologies shall remain in the asymmetric delay acceptance range of the decoder (see Annex A and configuration constraints in ISO 17458-2).

Figure 22 depicts the example of a bus with cascaded active stars.

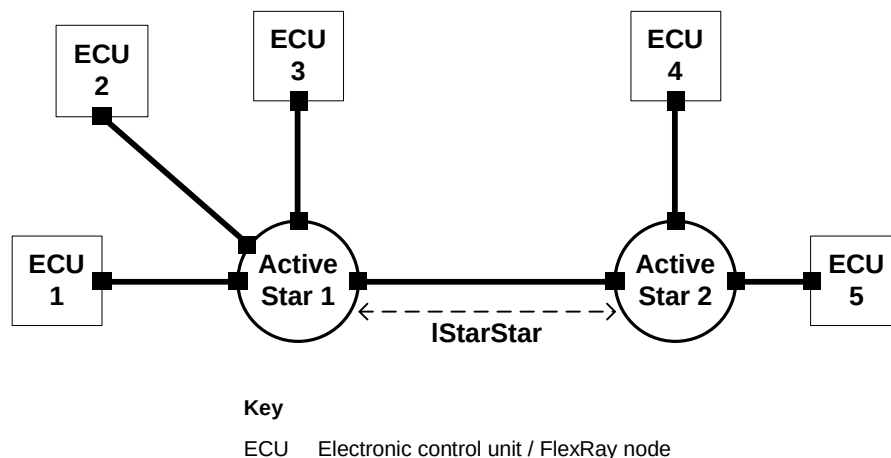


Figure 22 — Example of a bus with cascaded active stars

Table 15 defines the limitations of topologies with active stars.

Table 15 — Limitations of topologies with active stars

Name	Description	Min	Max	Unit
$nStarPath_{M,N}$	Number of active stars on the signal path from an ECU M to an ECU N 2,5 Mbit/s and 5 Mbit/s	0	2	—
	Number of active stars on the signal path from an ECU M to an ECU N 10 Mbit/s	0	1 ^a	—
^a Active stars are not possible since the asymmetric delay is too high. See Annex A.				

Practical limitations for *IStarStar* depend on factors like cable type and EMC disturbances.

Examples of practical values are given in Annex A, where also consideration about EMC robustness can be found in a separate subclause.

9.7 Hybrid topologies

In active star networks, one or more branches of the active star may be built as a linear passive bus or as a passive star. Considerations about signal asymmetries and about EMC robustness can be found in Annex A.

Figure 23 depicts the example of a hybrid bus structure.

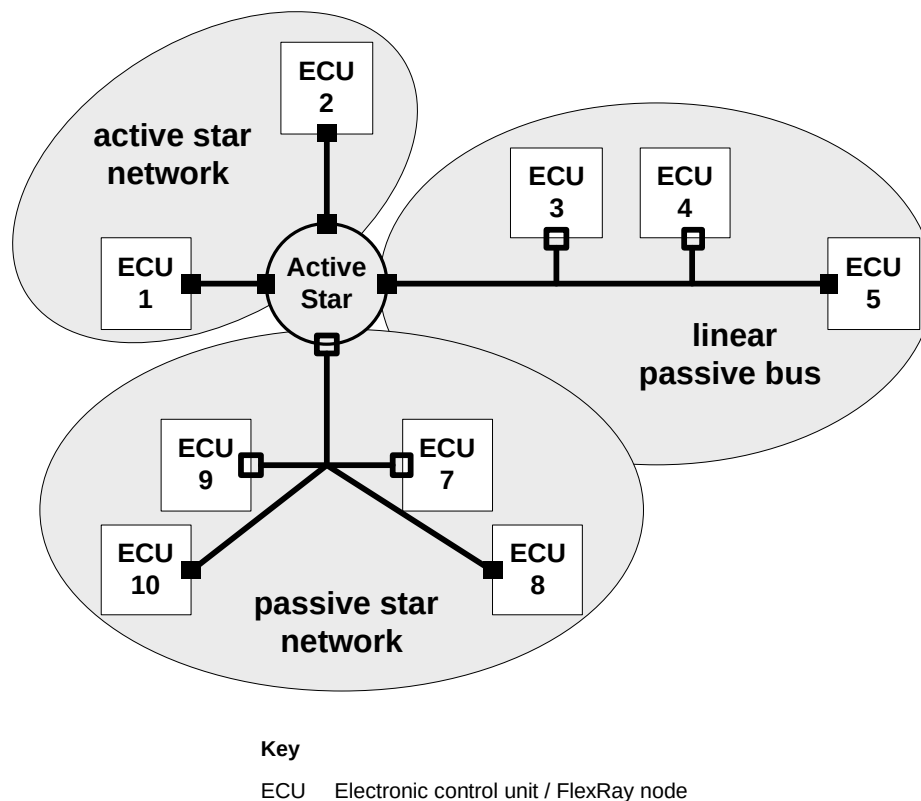


Figure 23 — Example of a hybrid bus structure

9.8 Dual channel topologies

FlexRay communication modules offer the possibility to serve up to two channels. This may be used to increase bandwidth and/or introduce a redundant channel in order to increase the level of fault tolerance. For further details see ISO 17458-2.

It is advisable to investigate and minimize the differences in the maximum propagation delays that occur on the two channels. See application hint about propagation delay in Annex A.

Furthermore the dual channel approach does not influence the BD definition.

10 Asymmetric delay budget

10.1 Objective

This Clause describes the specified ¹⁾ behaviour of the asymmetric delay on the way from a transmitting node to a receiving node via a dedicated FlexRay topology. The decoding procedure in the communication controller requires limiting the asymmetric delay (shifting of consecutive edges in the time domain) in a system.

1) The specification of the resulting requirements to the BD and CC is concretized in the corresponding chapters.

10.2 Basic topology for asymmetric delay budget

As basis for the definition of the asymmetric delay budget an active star network is used.

From the data communication point of view an active star network consists of several components in a row:

- A transmitting ECU consisting of:
a clock source, a CC, a BD and a connection hardware (e.g. CMC, connector, etc) to a first point-to-point network
- A first point-to-point network
- A retransmitting active star ECU consisting of:
a connection hardware to a first point-to-point network, the active star device and a connection hardware to a second point-to-point network
- A second point-to-point network
- A receiving ECU consisting of:
a connection hardware to a second point-to-point network, a BD, a CC and a clock source.

10.3 Definition of Test Planes

Various test planes are defined to derive test and measurement sceneries easily. The defined test planes are valid in any topology.

Figure 24 depicts the test planes in an active star network.

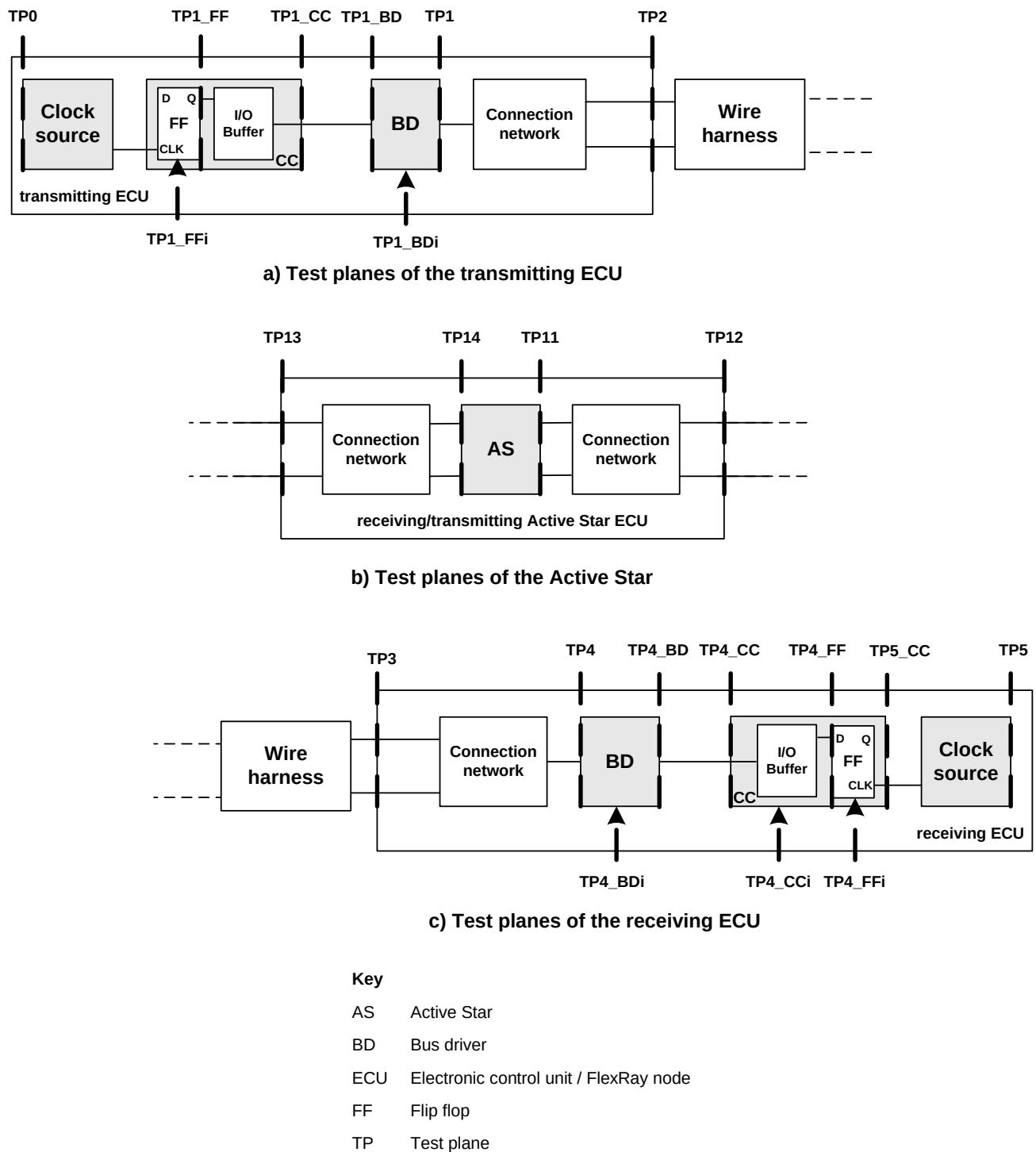


Figure 24 — Test planes in an active star network

Table 16 defines the test planes.

Table 16 — Test planes

Test plane	Description
TP0	Virtual time reference point.
TP1_FFi	Transmitting CC's virtual test plane to visualize PLL jitter, clock skew and propagation delay of the FlipFlop.
TP1_FF	Transmitting CC's internal test plane at 'Q' pin of last FlipFlop before output buffer
TP1_CC	Transmitting CC's output pin (TxD)
TP1_BD	Transmitting BD's input pin (TxD).
TP1_BDi	Transmitting BD's internal virtual test plane after detecting the logical state of the input signal.
TP1	Transmitting BD's output pins.
TP2	Transmitting ECU connector's terminals to the wiring harness.
TP13	Receiving AS ECU connector's terminals from the wiring harness.
TP14	Receiving AS devices input pins.
TP11	Transmitting AS device's output pins.
TP12	Transmitting AS ECU connector's terminals to the wiring harness.
TP3	Receiving ECU connector's terminals from the wiring harness.
TP4	Receiving BD's input pins.
TP4_BDi	Receiving BD's internal virtual test plane after detecting the logical state of the input signal.
TP4_BD	Receiving BD's output pin (RxD).
TP4_CC	Receiving CC's input pin (RxD).
TP4_CCi	Receiving CC's internal virtual test plane after detecting the logical state of the input signal.
TP4_FF	Receiving CC's internal test plane at 'D' pin of first FlipFlop after input buffer
TP4_FFi	Receiving CC's virtual test plane to visualize PLL jitter, clock skew and propagation delay of the FlipFlop.
TP5_CC	Clock input to CC
TP5	Virtual test plane at the input of the decoding algorithm.

10.4 Requirements to the asymmetric delay budget

The asymmetric delay shifts two consecutive edges against or away from each other. Each component (e.g. the transmitting BD) requires its portion (manufacturing tolerances, junction temperature, ageing etc.). Adding up all of these portions and subtracting the result from the decoder's asymmetric delay robustness gives a margin. This resulting margin can be used e.g. to ensure robustness against RF influences.

The decoder's asymmetric delay robustness shall be greater than the sum of all asymmetric delays of the entire network (see also Table 21).

10.5 Definition of maximum asymmetric delay portions

Three different types of values are considered in the following calculation:

Table 17 defines the types of values used in the following calculations.

Table 17 — Types of values used in the following calculations

Type	Description
Specified values	Values are required by this specification.
Educated guess	Values are estimated based on best engineers practice.
Derived values	Values are based on calculations by using specified boundary conditions.

To keep the description simple the portions of the asymmetric delay budget are noted by values only. Parameters with names and test conditions are introduced inside the corresponding subclauses.

FlexRay offers several possibilities for building robust networks. Also the active star network example in this subclause offers some alternative approaches.

An active star can be built in two ways:

- a) The active star is a monolithic device.
- b) The active star is non-monolithic and consists of more than one device.

Finally the asymmetric delay is considered on the following pages from two different point of views:

- a) influence to the shortening of a single bit
- b) influence to the sampling and synchronization of the decoder

The asymmetric delay in the active star network consists of several portions:

Table 18 defines the asymmetric delay budget TP0 to TP2.

Table 18 — Asymmetric delay budget TP0 to TP2

Amount ns	Portion	Description
$N \times 0,05$	Clock source	The specified tolerance of 500 ppm generates this portion regarding the duration of N bits at 10 Mbit/s. Lower datarates lead to bigger portions.
2,45	CC	The transmitting CC is allowed to vary the duration of a single nominal 100 ns bit by $\pm 2,45$ ns as specified in 14.2.3.
4,0	BD	The transmitting BD is allowed to vary the duration between two consecutive edges up to $\pm 4,0$ ns (TP1_BD $\rightarrow$ TP1) when the CC drives 25 pF load on its TxD pin as specified in 12.9.2. The 4 ns portion may be separated for further theoretical considerations into two portions: a) 1,5 ns represents the BD's digital detection of the CC's output signal caused by edge to pass the specified logical level thresholds. b) 2,5 ns represents the BD's analog output stage asymmetry.
0,5	Connection network	The connection network is estimated to change the duration between two consecutive edges by at most $\pm 0,5$ ns. A test set-up to measure this portion is not specified.
NOTE The worst case asymmetry from TP0 to TP2 sums up to 7,0 ns for one bit and to 7,45 ns for a period of ten bits at 10 Mbit/s at a load of 25 pF on TxD.		

Figure 25 depicts the asymmetric delay budget (TP0 to TP2).

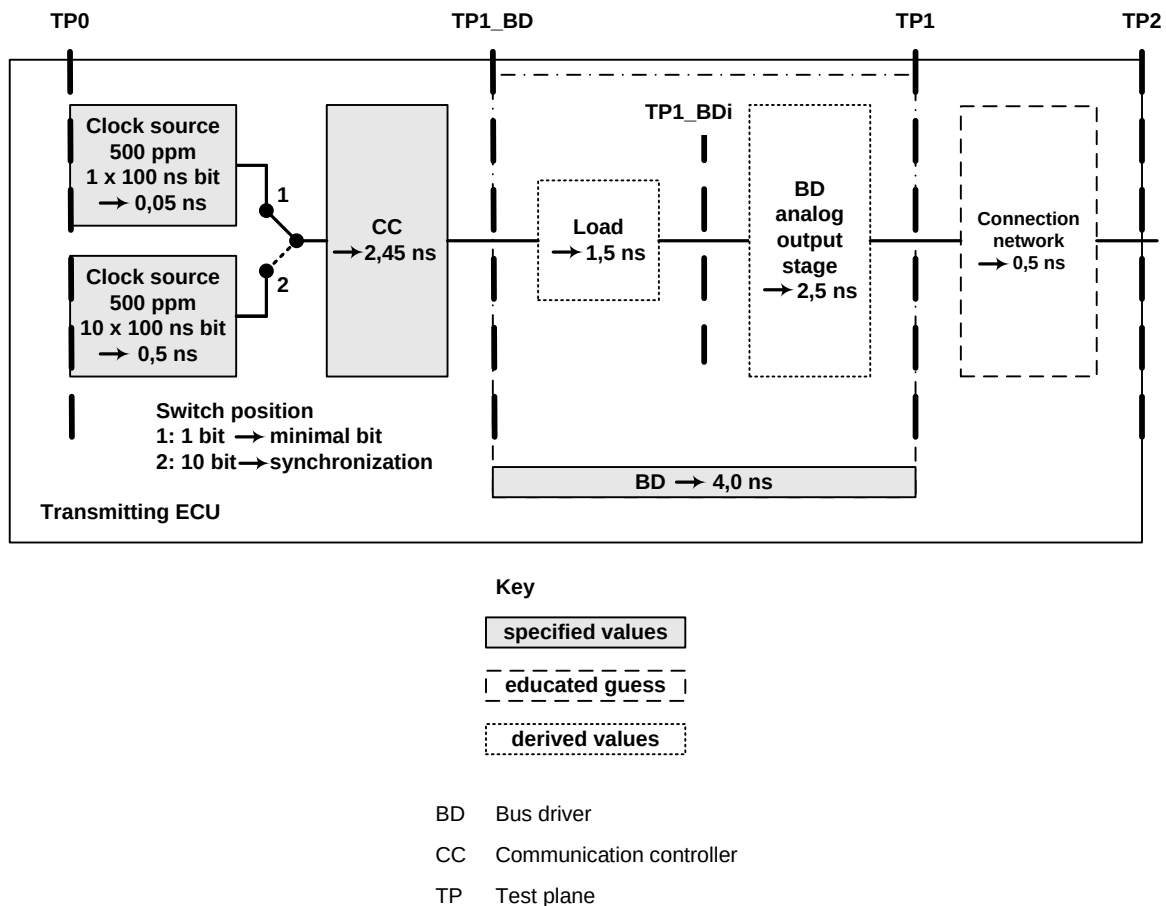


Figure 25 — Asymmetric delay budget (TP0 to TP2)

Table 19 defines the asymmetric delay budget (TP13 to TP12).

Table 19 — Asymmetric delay budget (TP13 to TP12)

Amount	Portion	Description
0,5 ns	Connection network	The connection network is estimated to change the duration between two consecutive edges by at most $\pm 0,5$ ns. A test set-up to measure this portion is not specified.
8,0 n (10,0 ns)	AS device	The AS is allowed to vary the duration between two consecutive edges up to $\pm 8,0$ ns (monolithic implementation) or $\pm 10,0$ ns (non-monolithic implementation) (TP14 → TP11): as specified in 13.3.2.
0,5 ns	Connection network	The connection network is estimated to change the duration between two consecutive edges by at most $\pm 0,5$ ns. A test set-up to measure this portion is not specified.
NOTE The worst case asymmetry from TP13 to TP12 sums up to 9,0 ns (11,0 ns).		

Figure 26 depicts the asymmetric delay budget (TP13 to TP12).

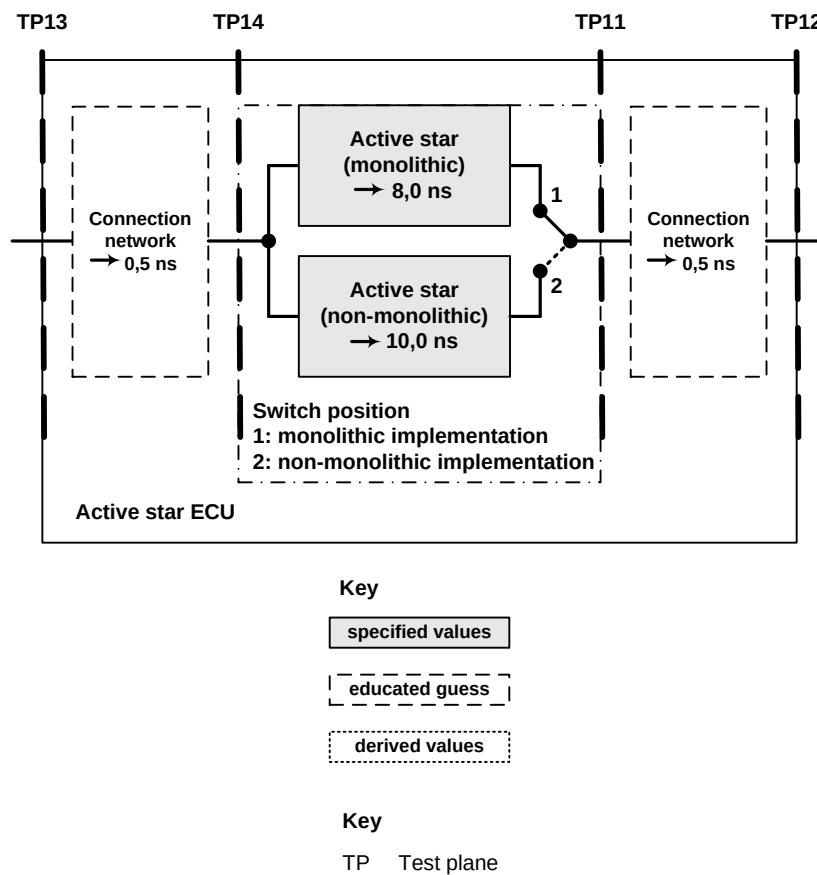


Figure 26 — Asymmetric delay budget (TP13 to TP12)