BS ISO 17987-7:2016

BSI Standards Publication

Road vehicles — Local Interconnect Network (LIN)

Part 7: Electrical Physical Layer (EPL) conformance test specification

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National foreword

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Part 7: Electrical Physical Layer (EPL) conformance test specification

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Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO shall not be held responsible for identifying any or all such patent rights. Details of any patent rights identified during the development of the document will be in the Introduction and/or on the ISO list of patent declarations received (see www.iso.org/patents).

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For an explanation on the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT) see the following URL: www.iso.org/iso/foreword.html.

The committee responsible for this document is ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Electrical and electronic equipment*.

A list of all parts in the ISO 17987 series can be found on the ISO website.

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Introduction

The LIN protocol as proposed is an automotive focused low-speed universal asynchronous receiver transmitter (UART)-based network. Some of the key characteristics of the Local Interconnect Network (LIN) protocol are signal-based communication, schedule table-based frame transfer, master/slave communication with error detection, node configuration and diagnostic service transportation.

The LIN protocol is for low-cost automotive control applications, for example, door module and air condition systems. It serves as a communication infrastructure for low-speed control applications in vehicles by providing

— signal-based communication to exchange information between applications in different nodes,

— bitrate support from 1 kbit/s to 20 kbit/s,

— deterministic schedule table-based frame communication,

— network management that wakes up and puts the LIN cluster into sleep mode in a controlled manner,

— status management that provides error handling and error signalling,

— transport layer that allows large amount of data to be transported (such as diagnostic services),

— specification of how to handle diagnostic services,

— electrical physical layer specifications,

— node description language describing properties of slave nodes,

— network description file describing behaviour of communication, and

— application programmer's interface.

ISO 17987 (all parts) is based on the open systems interconnection (OSI) basic reference model as specified in ISO/IEC 7498–1 which structures communication systems into seven layers.

The OSI model structures data communication into seven layers called (top down) *application layer* (layer 7), *presentation layer*, *session layer*, *transport layer*, *network layer*, *data link layer* and *physical layer* (layer 1). A subset of these layers is used in ISO 17987 (all parts).

ISO 17987 (all parts) distinguishes between the services provided by a layer to the layer above it and the protocol used by the layer to send a message between the peer entities of that layer. The reason for this distinction is to make the services, especially the application layer services and the transport layer services, reusable also for other types of networks than LIN. In this way, the protocol is hidden from the service user and it is possible to change the protocol if special system requirements demand it.

ISO 17987 (all parts) provides all documents and references required to support the implementation of the requirements related to the following:

— ISO 17987–1: This part provides an overview of the ISO 17987 (all parts) and structure along with the use case definitions and a common set of resources (definitions, references) for use by all subsequent parts.

— ISO 17987–2: This part specifies the requirements related to the transport protocol and the network layer requirements to transport the PDU of a message between LIN nodes.

— ISO 17987–3: This part specifies the requirements for implementations of the LIN protocol on the logical level of abstraction. Hardware related properties are hidden in the defined constraints.

— ISO 17987–4: This part specifies the requirements for implementations of active hardware components which are necessary to interconnect the protocol implementation.

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— ISO/TR 17987–5: This part specifies the LIN application programmers interface (API) and the node configuration and identification services. The node configuration and identification services are specified in the API and define how a slave node is configured and how a slave node uses the identification service.

— ISO 17987–6: This part specifies tests to check the conformance of the LIN protocol implementation according to ISO 17987–2 and ISO 17987–3. This comprises tests for the data link layer, the network layer and the transport layer.

— ISO 17987–7: This part specifies tests to check the conformance of the LIN electrical physical layer implementation (logical level of abstraction) according to ISO 17987–4.

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Road vehicles — Local Interconnect Network (LIN) —

Part 7: Electrical Physical Layer (EPL) conformance test specification

1 Scope

This document specifies the conformance test for the electrical physical layer (EPL) of the LIN communications system. It is part of this document to define a test that considers ISO 9646 and ISO 17987–4.

The purpose of this document is to provide a standardized way to verify whether a LIN bus driver is compliant to ISO 17987–4. The primary motivation is to ensure a level of interoperability of LIN bus drivers from different sources in a system environment.

This document provides all the necessary technical information to ensure that test results are consistent even on different test systems, provided that the particular test suite and the test system are compliant to the content of this document.

2 Normative references

The following documents are referred to in text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 17987–4:2016, *Road vehicles — Local Interconnect Network (LIN) — Part 4: Electrical Physical Layer (EPL) specification 12V/24V*

3 Terms, definitions, symbols and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the terms and definitions in ISO 17987–4 and ISO 17987–6 apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

NOTE This also includes the device classification of ISO 17987–6:2016, 5.6 into class A/B/C for the different ECU and transceiver types.

3.2 Symbols

%	Percentage
µs	Microsecond
C1/2	capacitance

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C_{COMMON}	capacitance in the communication line
$C`_{LINE}$	line capacitance
C_{BUS}	total bus capacitance
C_{MASTER}	capacitance of master node
C_{REF}	reference capacitance
C_{RXD}	RXD capacitance (LIN receiver, RXD capacitive load condition)
C_{SLAVE}	capacitance of slave node
∈	mathematical symbol: replacement for “is an element of”
d^2V/dt^2	second derivative of Voltage (Volt^2 per second^2)
di/dt	instantaneous rate of current change (amps per second)
D1/2	diode
D_{ser_int}	serial internal diode at transceiver IC
D_{ser_master}	serial master diode
F_{TS}	test system bit rate
I_{BUS}	current into the ECU bus line
I_{BUS_LIM}	current limitation for driver dominant state driver on $V_{BUS} = V_{BAT_max}$ into ECU bus line
$I_{BUS_NO_BAT}$	current at ECU bus line when V_{BAT} is disconnected
$I_{BUS_NO_GND}$	current at ECU bus line when V_{GND_ECU} is disconnected
$I_{BUS_PAS_dom}$	current at ECU bus line when driver off (passive) at dominant LIN-bus-level (12 V LIN devices: V_{BUS} = 0 V and V_{BAT} = 12 V; 24 V LIN devices: V_{BUS} = 0 V and V_{BAT} = 24 V)
$I_{BUS_PAS_rec}$	current at ECU bus line when driver off (passive) at recessive LIN-bus-level (12 V LIN devices: 8 V < V_{BAT} < 18 V; 8 V < V_{BUS} < 18 V; $V_{BUS} \geq V_{BAT}$; 24 V LIN devices: 16 V < V_{BAT} < 36 V; 16 V < V_{BUS} < 36 V; $V_{BUS} \geq V_{BAT}$)
GND_{Device}	GND of ECU
kΩ	kilo ohm
kbit/s	kilo bit per second
LEN_{BUS}	total length of bus line
LIN_{Bus}	LIN network
ms	millisecond
nF	nano farad
pF	pico farad
pF/m	pico farad per meter (line capacitance)

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R1/2	resistor
R_{COMMON}	resistor in the communication line
R_{BUS}	total bus-resistor including all slave and master resistors $R_{BUS} = R_{Master}\|\|R_{Slave1}\|\|R_{Slave2}\|\|to\|\|R_{SlaveN}$
R_{REF}	reference resistor
R_{master}	master resistor
R_{pull_up}	pull-up resistor
R_{slave}	slave resistor
t_{BFS}	byte field synchronization time
t_{BIT}	basic bit times
t_{EBS}	earliest bit sample time
t_{rx_pd}	propagation delay of receiver
t_{rx_sym}	symmetry of receiver propagation delay rising edge propagation delay of receiver
t_{LBS}	latest bit sample time
$t_{rx_pdf(1)}$	propagation delay time of receiving node 1 at falling (recessive to dominant) LIN bus edge
$t_{rx_pdf(2)}$	propagation delay time of receiving node 2 at falling (recessive to dominant) LIN bus edge
$t_{rx_pdr(1)}$	propagation delay time of receiving node 1 at rising (dominant to recessive) LIN bus edge
$t_{rx_pdr(2)}$	propagation delay time of receiving node 2 at rising (dominant to recessive) LIN bus edge
t_{SR}	sample window repetition time
$TH_{Dom(max)}$	maximum dominant threshold of receiving node (volt)
$TH_{Dom(min)}$	minimum dominant threshold of receiving node (volt)
$TH_{Rec(max)}$	maximum recessive threshold of receiving node (volt)
$TH_{Rec(min)}$	minimum recessive threshold of receiving node (volt)
V	voltage
V_{ANODE}	voltage at the anode of the diode
V_{BAT}	voltage across the ECU supply connectors
$V_{BATTERY}$	voltage across the vehicle battery connectors
$V_{BS1/2}$	battery shift
V_{BUS}	voltage on the LIN bus
V_{BUS_CNT}	centre point of receiver threshold
V_{BUS_dom}	receiver dominant voltage
V_{BUS_rec}	receiver recessive voltage

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$V_{CATHODE}$ voltage at the cathode of the diode

$V_{CC1/2}$ positive power supply voltage (e.g. 5 V)

$V_{D1/2}$ voltage at diode between anode and cathode

V_{Dom} dominant voltage

$V_{GND1/2}$ ground shift

$V_{GND_BATTERY}$ battery ground voltage

V_{GND_ECU} voltage on the local ECU ground connector with respect to vehicle battery ground connector ($V_{GND_BATTERY}$)

V_{HYS} receiver hysteresis voltage

V_{IUT} voltage at IUT supply pins

$V_{PS1/2}$ voltage at remote power supply no. 1/no. 2

V_{Rec} recessive voltage

$V_{SerDiode}$ voltage drop at the serial diodes

V_{Shift_BAT} battery shift

$V_{Shift_Difference}$ difference between battery shift and GND shift

V_{Shift_GND} GND shift

V_{SUP} voltage at transceiver supply pins

$V_{SUP_NON_OP}$ voltage which the device is not destroyed; no guarantee of correct operation

V_{th_dom} receiver threshold voltage of the recessive to dominant LIN bus edge

V_{th_rec} receiver threshold voltage of the dominant to recessive LIN bus edge

$\Delta F/F_{Nom}$ deviation from nominal bit rate

τ time constant

Ω ohm

3.3 Abbreviated terms

AC alternate current

API application programmers interface

ASIC application specific integrated circuit

BFS byte field synchronization

DC direct current

EBS earliest bit sample

EMC electromagnetic compatibility

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EMI	electromagnetic interference
EPL	electrical physical layer
ESD	electrostatic discharge
GND	ground
IUT	implementation under test
LBS	latest bit sample
Max.	maximum
Min.	minimum
no.	number
OSI	open systems interconnection
PDU	protocol data unit
RC	RC time constant τ ($\tau = C_{BUS} \times R_{BUS}$)
RX	RX pin of the transceiver
RXD	receive data
SBC	system basis chip
SR	sample window repetition
TRX	transceiver
TX	TX pin of the transceiver
TXD	transmit data
Typ	typical
UART	universal asynchronous receiver transmitter

4 Conventions

ISO 17987 (all parts) is based on the conventions specified in the OSI Service Conventions (ISO/IEC 10731) as they apply for physical layer, data link layer, network and transport protocol and diagnostic services.

5 EPL 12 V LIN devices with RX and TX access

This clause addresses class A and class B devices.

5.1 Test specification overview

5.1.1 Test case organization

The intention of each test case is described at first, with a short textual explanation. Before tests are executed, the test system shall be set to its initial state as described in 5.2.

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The test procedure and the expected results are described in the form of a chart for each test case. Table 1 is a typical test description and defines the test case organization.

Table 1 — Test case organization

IUT node as	Class A/B/C device as master or slave or both	Corresponding test number TC x, TC y, where x, y are the test case number
Initial state	**Parameters:**	
	Number of nodes	Number of node in the test implementation
	Bus loads	In order to simulate a LIN network
	Operational conditions:	
	IUT mode	Operation mode for the IUT (e.g. normal mode, low power mode, ...).
	TX signal	State of TX pin at the beginning of the test.
	RX signal	Logical output voltages of the Rx pin corresponding to recessive/dominant level at the LIN pin are taken from the datasheet of the IUT.
	V_{BAT}, V_{SUP}, V_{IUT}, V_{CC}, $V_{PS1/2}$, V_{BUS}	Value in volt
	Failure	In order to set failure at
	GND Shift	Value in volt
Test steps	Describe the test stages.	
Response	Describe the result expected in order to decide if the test passed or failed.	
Reference	Corresponding number in ISO 17987–4.	

IUT may be a master or slave ECU or an individual transceiver chip. The RX, TX and V_{SUP} signals shall be accessible for proper test execution. It is recommended to test with RX/TX access, if not possible, testing according the specification without RX/TX access (see Clause 6) is accepted. Depending on the type of IUT, the supply voltage is V_{BAT} for ECU or V_{SUP} for a chip, referred to as V_{IUT} in this description.

5.1.2 Measurement and signal generation requirements

Table 2 defines the requirements in measurement and signal generation.

Table 2 — Measurement and signal generation requirements

Signal generation:	Rise/Fall time		<20 ns (square wave) <40 ns (triangle)
	Frequency		20 ppm
	Jitter		<25 ns
Signal measurement:	Dynamic signals:		Oscilloscope 100 MHz rise time ≤3,5 ns
	Static signals:	DC voltage	0,5 %
		DC current	0,6 %
		Resistance	0,5 %
Power Supply (V_{BAT}, V_{SUP}, V_{IUT}, V_{CC}, $V_{PS1/2}$, V_{BUS})	Resolution		10 mV/1 mA
	Accuracy		0,2 % of value

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5.2 Operational conditions — Calibration

5.2.1 Electrical input/output, LIN protocol

The initial configuration for each test case is defined here. Any requirements for individual tests are specified with the test case.

Table 3 defines the initial state of electrical input/output.

Table 3 — Initial state of electrical input/output

Initial state	**Parameters:**	
	Number of nodes	1
	Bus loads	—
	Operational conditions:	
	IUT mode	Set to normal/active mode
	TX signal	Recessive
	V_{BAT}, V_{SUP}, V_{IUT}, V_{CC}, $V_{PS1/2}$, V_{BUS}	Specified for each test
	Failure	No failure
	GND shift	0 V

5.2.2 [EPL–CT 1] Operating voltage range

This test shall ensure the correct operation in the valid supply voltage ranges, by correct reception of dominant bits. The IUT is therefore supplied with an increasing/decreasing voltage ramp.

Figure 1 shows the test configuration of the test system "Operating voltage range with RX and TX access".

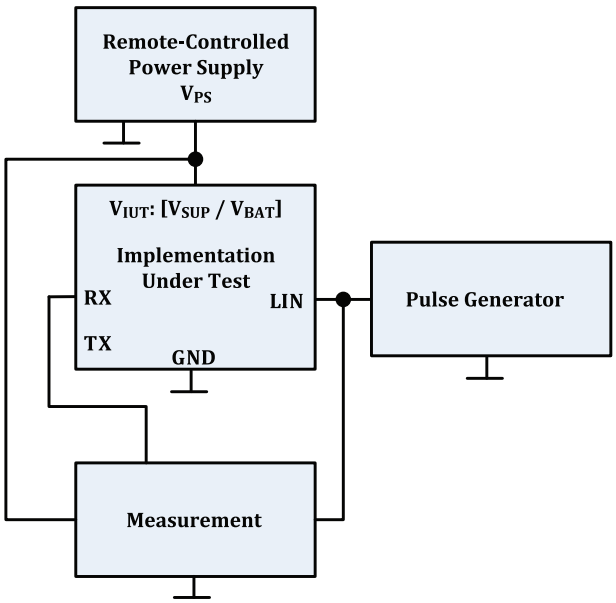

Figure 1 — Test system: Operating voltage range with RX and TX access

Table 4 defines the test system "Operating voltage range with RX and TX access".

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Table 4 — Test system: Operating voltage range with RX and TX access

IUT node as	Class B device as master or slave Class A device	[EPL–CT 1].1, [EPL–CT 1].2
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}]	Table 5
Test steps	A voltage ramp is set on the V_{SUP}/V_{BAT} as defined in Table 5. The LIN signal is driven with a 10 kHz rectangular signal with a duty cycle of 50 % and a voltage swing of 18 V. The IUT shall be in operational/active mode	
Response	The RX pin of the IUT shall show the 10 kHz signal. A maximum deviation of 10 % (time, voltage) is allowed (see Figure 2).	
Reference	ISO 17987–4:2016, Table 10, Param 9, Param 10	

Figure 2 shows the RX response of the test system "Operating voltage range".

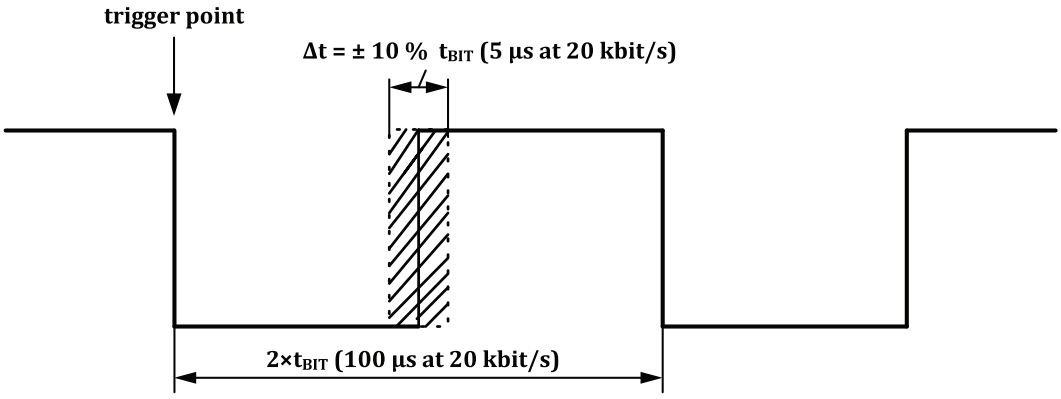

Figure 2 — RX response of test system: Operating voltage range

Table 5 defines the test cases for "Operating voltage ramp".

Table 5 — Test cases: Operating voltage ramp

EPL–CT–TC	**V_{IUT} range: [V_{SUP} range/V_{BAT} range]**	**Signal ramp**
[EPL–CT 1].1	[7,0 V to 18 V]/[8,0 V to 18 V]	0,1 V/s
[EPL–CT 1].2	[18 V to 7,0 V]/[18 V to 8,0 V]	0,1 V/s

5.2.3 Threshold voltages

5.2.3.1 General

This group of tests checks whether the receiver threshold voltages of the IUT are implemented correctly within the entire specified operating supply voltage range. The LIN bus voltage is driven with a voltage ramp checking the entire dominant and recessive signal area with respect to the applied supply voltage. In 5.2.3.2 and 5.2.3.3, the signal shall stay continuously on recessive or dominant level depending on the test case. In 5.2.3.4, the RX output transition is detected. Figure 3 shows the triangle signal on the LIN bus.

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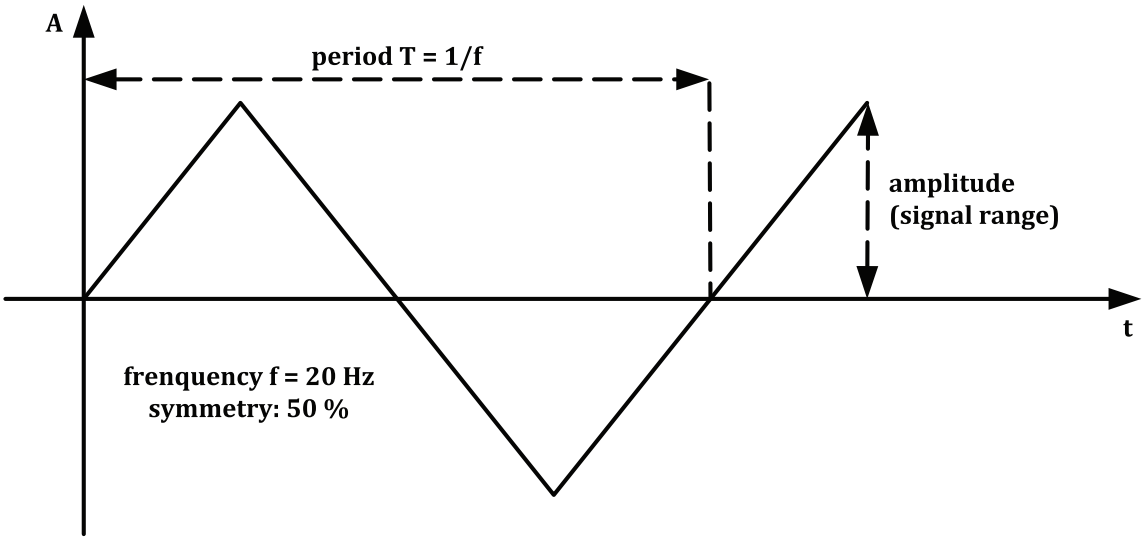

Figure 3 — Triangle signal on the LIN bus

5.2.3.2 [EPL–CT 2] IUT as receiver: V_{SUP} at V_{BUS_dom} (down)

Figure 4 shows the test configuration of the test system "IUT as receiver V_{SUP} at V_{BUS_dom} (down)".

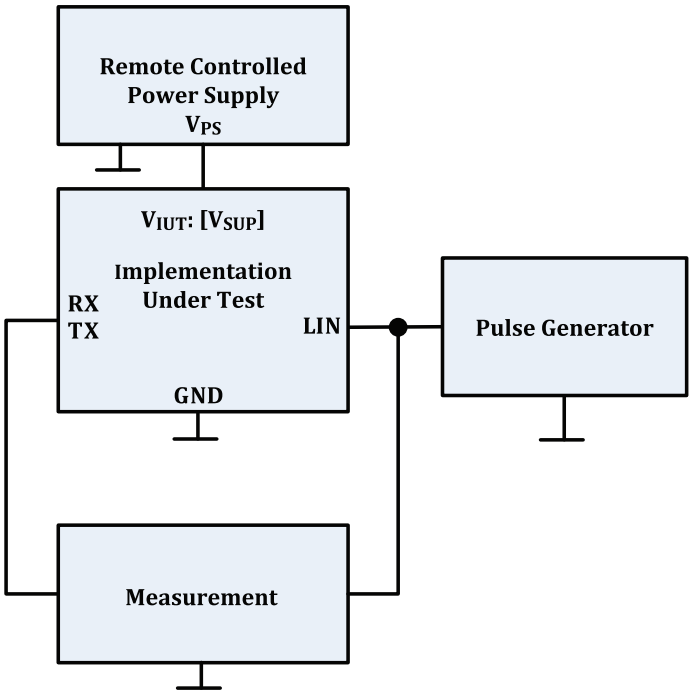

Figure 4 — Test system: IUT as receiver V_{SUP} at V_{BUS_dom} (down)

Table 6 defines the test system "IUT as receiver V_{SUP} at V_{BUS_dom} (down)".

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Table 6 — Test system: IUT as receiver V_{SUP} at V_{BUS_dom} (down)

IUT node as	Class A device	[EPL–CT 2].1, [EPL–CT 2].2, [EPL–CT 2].3
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}]	Table 7
Test steps	A triangle signal with f = 20 Hz and symmetry of 50 % is set on the LIN Bus (see Figure 3).	
Response	The IUT shall generate a dominant or recessive value on RX as defined on Table 7 during the falling slope of the triangle signal.	
Reference	ISO 17987–4:2016, Table 10, Param 17, Param 18 ISO 17987–4:2016, Figure 4	

Table 7 defines the test cases for the falling slope of the triangle signal on the LIN bus.

Table 7 — Test cases: Falling slope of the triangle signal on the LIN bus

EPL–CT–TC	V_{IUT}: [V_{SUP}]	Signal range	Expected RX signal
[EPL–CT 2].1	7 V	[18 V to 4,2 V]	Recessive
		[2,8 V to –1,05 V]	Dominant
[EPL–CT 2].2	14 V	[18 V to 8,4 V]	Recessive
		[5,6 V to –2,1 V]	Dominant
[EPL–CT 2].3	18 V	[20,7 V to 10,8 V]	Recessive
		[7,2 V to –2,7 V]	Dominant

5.2.3.3 [EPL–CT 3] IUT as receiver: V_{SUP} at V_{BUS_rec} (up)

Figure 5 shows the test configuration of the test system "IUT as receiver V_{SUP} at V_{BUS_rec} (up)".

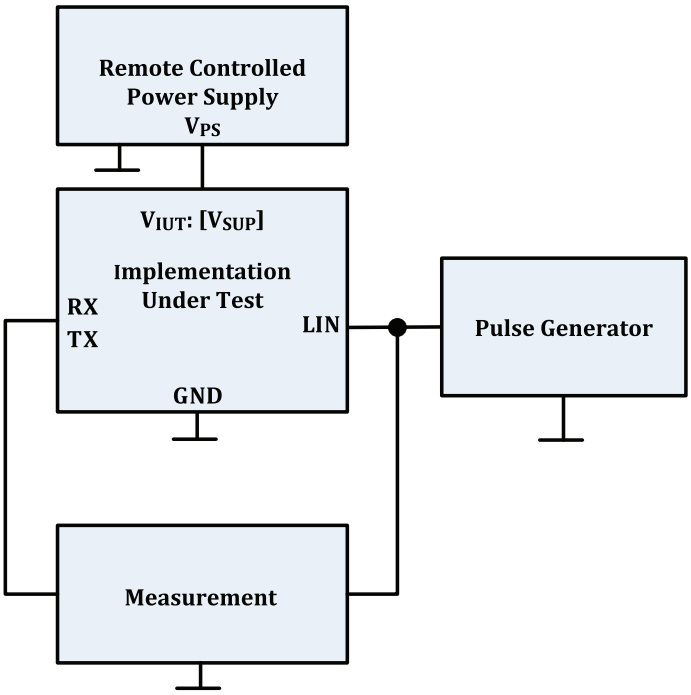

Figure 5 — Test system: IUT as receiver V_{SUP} at V_{BUS_rec} (up)

Table 8 defines the test system "IUT as receiver V_{SUP} at V_{BUS_rec} (up)".

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Table 8 — Test system: IUT as receiver V_{SUP} at V_{BUS_rec} (up)

IUT node as	Class A device	[EPL–CT 3].1, [EPL–CT 3].2, [EPL–CT 3].3
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}]	Table 9
Test steps	A triangle signal with f = 20 Hz and symmetry of 50 % is set on the LIN Bus (see Figure 3).	
Response	The IUT shall generate a dominant or recessive value on RX as defined on Table 9 during the rising slope of the triangle signal.	
Reference	ISO 17987–4:2016, Table 10, Param 17, Param 18 ISO 17987–4:2016, Figure 4	

Table 9 defines the test cases for the rising slope of the triangle signal on the LIN bus.

Table 9 — Test cases: Rising slope of the triangle signal on the LIN bus

EPL–CT–TC	V_{IUT}: [V_{SUP}]	Signal range	Expected RX signal
[EPL–CT 3].1	7 V	[–1,05 V to 2,8 V]	Dominant
		[4,2 V to 18 V]	Recessive
[EPL–CT 3].2	14 V	[–2,1 V to 5,2 V]	Dominant
		[7,8 V to 18 V]	Recessive
[EPL–CT 3].3	18 V	[–2,7 V to 7,2 V]	Dominant
		[10,8 V to 20,7 V]	Recessive

5.2.3.4 [EPL–CT 4] IUT as receiver: V_{SUP} at V_{BUS}

This test shall verify the symmetry of the receiver thresholds. For this purpose a voltage ramp on V_{BUS} shows the required threshold values.

Figure 6 shows the test configuration of the test system "IUT as receiver V_{SUP} at V_{BUS}".

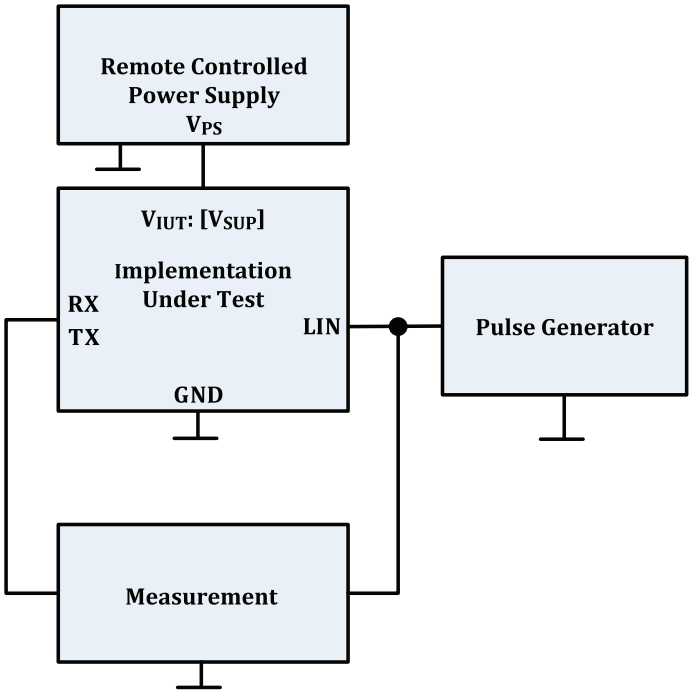

Figure 6 — Test system: IUT as receiver V_{SUP} at V_{BUS}

Table 10 defines the test system "IUT as receiver V_{SUP} at V_{BUS}".

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Table 10 — Test system: IUT as receiver V_{SUP} at V_{BUS}

IUT node as	Class A device	[EPL–CT 4].1, [EPL–CT 4].2, [EPL–CT 4].3
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}]	Table 11
Test steps	A triangle signal with f = 20 Hz and symmetry of 50 % is set on the LIN Bus (see Figure 3).	
Response	The RX output of the IUT shall switch from dominant to recessive when the LIN bus voltage ramps up and it shall switch from recessive to dominant when the LIN bus voltage ramps down. The RX output transition shall meet the following conditions: — $V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2$ in the range of (0,475 to 0,525) × V_{SUP} — $V_{HYS} = V_{th_rec} - V_{th_dom}$ shall be less than 0,175 × V_{SUP}	
Reference	ISO 17987–4:2016, Table 10, Param 19, Param 20	

Table 11 defines the test cases for "IUT as receiver V_{SUP} at V_{BUS}".

Table 11 — Test cases: IUT as receiver V_{SUP} at V_{BUS}

EPL–CT–TC	V_{IUT}: [V_{SUP}]	**Signal range**
[EPL–CT 4].1	7 V	[–1,05 V to 8,05 V] up [8,05 V to –1,05 V] down
[EPL–CT 4].2	14 V	[–2,1 V to 16,1 V] up [16,1 V to –2,1 V] down
[EPL–CT 4].3	18 V	[–2,7 V to 20,7 V] up [20,7 V to –2,7 V] down

5.2.4 [EPL–CT 5] Variation of $V_{SUP_NON_OP}$

Variation of $V_{SUP_NON_OP}$ shall be checked within this test, whether the IUT influences the bus during under voltage and over voltage conditions.

Figure 7 shows the test configuration of the test system "Variation of $V_{SUP_NON_OP}$".

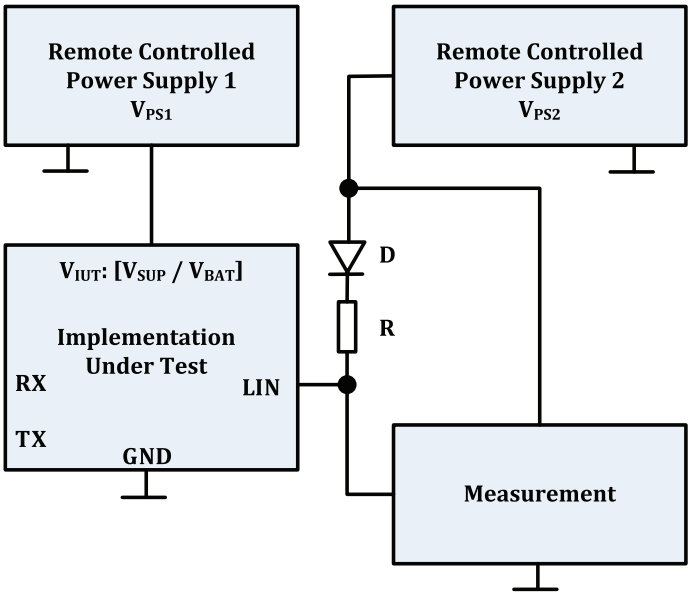

Figure 7 — Test system: Variation of $V_{SUP_NON_OP}$

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Table 12 defines the test system "Variation of $V_{SUP_NON_OP}$".

Table 12 — Test system: Variation of $V_{SUP_NON_OP}$

IUT node as	Class B device as master	[EPL–CT 5].1
	Class B device as slave	[EPL–CT 5].2
	Class A device	[EPL–CT 5].3
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}]	V_{IUT} Signal with a 1 V/s ramp in the range see Table 13
	V_{IUT}; V_{PS2}	See Table 13
	Bus load	See Table 13
Test steps	A voltage ramp (up and down) is set on V_{IUT1}. The stimulus stays for t = 30 s at V_{IUT1} = 40 V. The TX signal shall be left open if an internal pull-up is provided or applied with a recessive level.	
Response	No dominant state on LIN shall occur. The IUT shall not be destroyed during the test. The afterward recessive voltage shall have a maximum deviation of ±5 % from the before recessive voltage.	
Reference	ISO 17987–4:2016, Table 10, Param 11	

Table 13 defines the test cases "Variation of $V_{SUP_NON_OP}$".

Table 13 — Test cases: Variation of $V_{SUP_NON_OP}$

EPL–CT–TC	**V_{IUT} range: [V_{SUP} range/V_{BAT} range]**	V_{PS2}	**Bus load**
[EPL–CT 5].1	[–0,3 V to 8 V], [18 V to 40 V]	18 V	60 k + diode (1N4148)
[EPL–CT 5].2	[–0,3 V to 8 V], [18 V to 40 V]	18 V	1,1 k + diode (1N4148)
[EPL–CT 5].3	[–0,3 V to 7 V], [18 V to 40 V]	18 V	1,1 k + diode (1N4148)

5.2.5 I_{BUS} under several conditions

5.2.5.1 [EPL–CT 6] I_{BUS_LIM} at dominant state (driver on)

This test checks the drive capability of the output stage. A LIN driver shall pull the LIN bus below a certain voltage according to the LIN standard. The current limitation is measured indirectly.

Figure 8 shows the test configuration of the test system "I_{BUS_LIM} at dominant state (driver on)".

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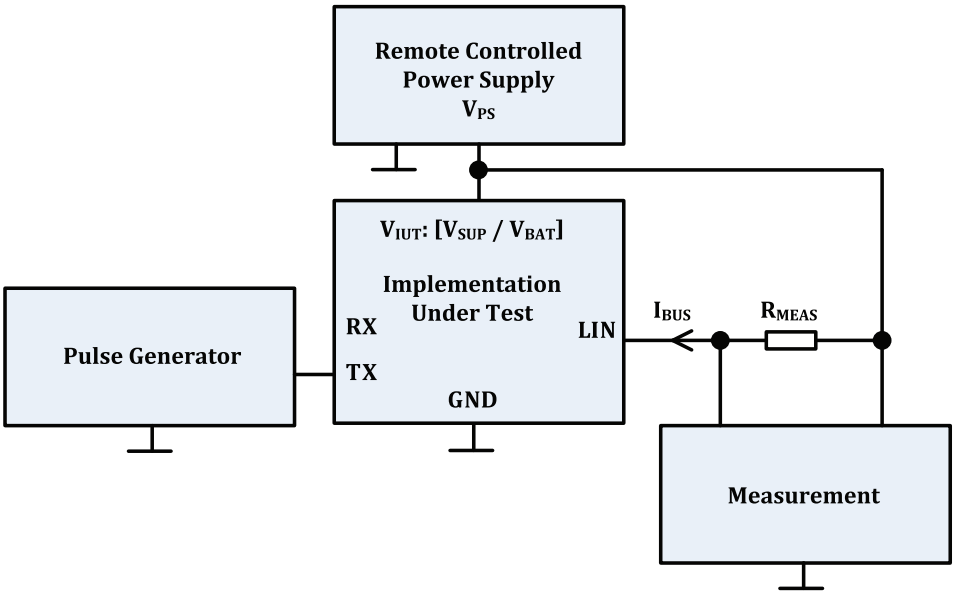

Figure 8 — Test system: I_{BUS_LIM} at dominant state (driver on)

Table 14 defines the test system "I_{BUS_LIM} at dominant state (driver on)".

Table 14 — Test system: I_{BUS_LIM} at dominant state (driver on)

IUT node as	Class B device as master Class B device as slave Class A device	[EPL–CT 6].1
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}] R_{MEAS}	See Table 15
Test steps	The LIN pin is connected via R_{MEAS} to V_{IUT}. The TX signal is driven with a rectangular signal (T = 10 ms) with a duty cycle of 50 %.	
Response	LIN shall show the rectangular signal. The dominant state bus level shall be lower than TH_DOM = 0,251 × V_{IUT} = 4,518 V for transceiver. The dominant state bus level shall be lower than TH_DOM = 0,251 × (V_{IUT} – 1 V) = 4,267 V for ECU's.	
Reference	ISO 17987–4:2016, Table 10, Param 12	

Table 15 defines the test cases "I_{BUS_LIM} at dominant state (driver on)".

Table 15 — Test cases: I_{BUS_LIM} at dominant state (driver on)

EPL–CT–TC	V_{IUT}: [V_{SUP}/V_{BAT}]	R_{MEAS}
[EPL–CT 6].1	18 V	440 Ω (0,1 %)

5.2.5.2 [EPL–CT 7] $I_{BUS_PAS_dom}$: IUT in recessive state: V_{BUS} = 0 V

This test case is intended to test the input leakage current $I_{BUS_PAS_dom}$ into a node during dominant state of the LIN bus.

Figure 9 shows the test configuration of the test system "$I_{BUS_PAS_dom}$ IUT in recessive state V_{BUS} = 0 V".

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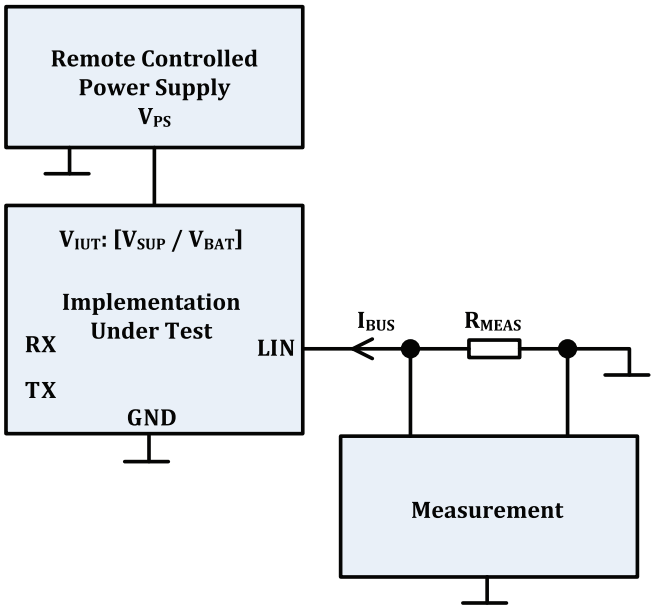

Figure 9 — Test system: $I_{BUS_PAS_dom}$ IUT in recessive state V_{BUS} = 0 V

Table 16 defines the test system "$I_{BUS_PAS_dom}$ IUT in recessive state V_{BUS} = 0 V".

Table 16 — Test system: $I_{BUS_PAS_dom}$ IUT in recessive state V_{BUS} = 0 V

IUT node as	Class B device as slave Class A device	[EPL–CT 7].1
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}] R_{MEAS}	See Table 17
Test steps	The TX signal is set recessive.	
Response	The maximum value of voltage drop shall be higher than –500 mV.	
Reference	ISO 17987–4:2016, Table 10, Param 13	

Table 17 defines the test cases "$I_{BUS_PAS_dom}$ IUT in recessive state V_{BUS} = 0 V".

Table 17 — Test cases: $I_{BUS_PAS_dom}$ IUT in recessive state V_{BUS} = 0 V

EPL–CT–TC	V_{IUT}: [V_{SUP}/V_{BAT}]	R_{MEAS}
[EPL–CT 7].1	12 V	499 Ω (0,1 %)

5.2.5.3 [EPL–CT 8] $I_{BUS_PAS_rec}$: IUT in recessive state: V_{SUP} = 7,0 V with variation of V_{BUS} ∈ [8,0 V to 18 V]

This test checks whether there is a diode implementation within the termination path of the IUT. The reverse current should be limited to $I_{BUS_PAS_rec(max)}$ from the LIN wire into the IUT even if V_{BUS} is higher than the IUTs supply voltage V_{IUT}.

Figure 10 shows the test configuration of the test system "$I_{BUS_PAS_rec}$ IUT in recessive state".

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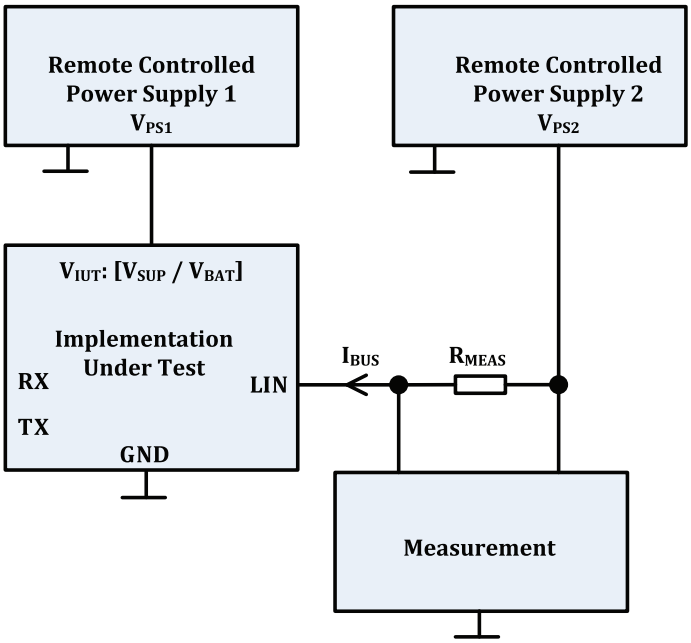

Figure 10 — Test system: $I_{BUS_PAS_rec}$ IUT in recessive state

Table 18 defines the test system "$I_{BUS_PAS_rec}$ IUT in recessive state".

Table 18 — Test system: $I_{BUS_PAS_rec}$ IUT in recessive state

IUT node as	Class B device as master Class B device as slave Class A device	[EPL–CT 8].1
Initial State	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}] R_{MEAS}	See Table 19
Test steps	V_{PS2} = Signal with a 2 V/s ramp in the range [8 V to 18 V] up and down. The TX signal is set recessive.	
Response	The maximum value of voltage drop shall be less than or equal to 20 mV.	
Reference	ISO 17987–4:2016, Table 10, Param 14	

Table 19 defines the test cases "$I_{BUS_PAS_rec}$ IUT in recessive state".

Table 19 — Test cases: $I_{BUS_PAS_rec}$ IUT in recessive state

EPL–CT–TC	V_{IUT}: [V_{SUP}/V_{BAT}]	R_{MEAS}
[EPL–CT 8].1	7,0 V/8,0 V	1 000 Ω (0,1 %)

5.2.6 Slope control

5.2.6.1 Purpose

The purpose of this test is to check the duty cycle of the driver stage.

5.2.6.2 [EPL–CT 9] Measuring the duty cycle at 10,417 kbit/s — IUT as transmitter

Figure 11 shows the test configuration of the test system "Slope control".

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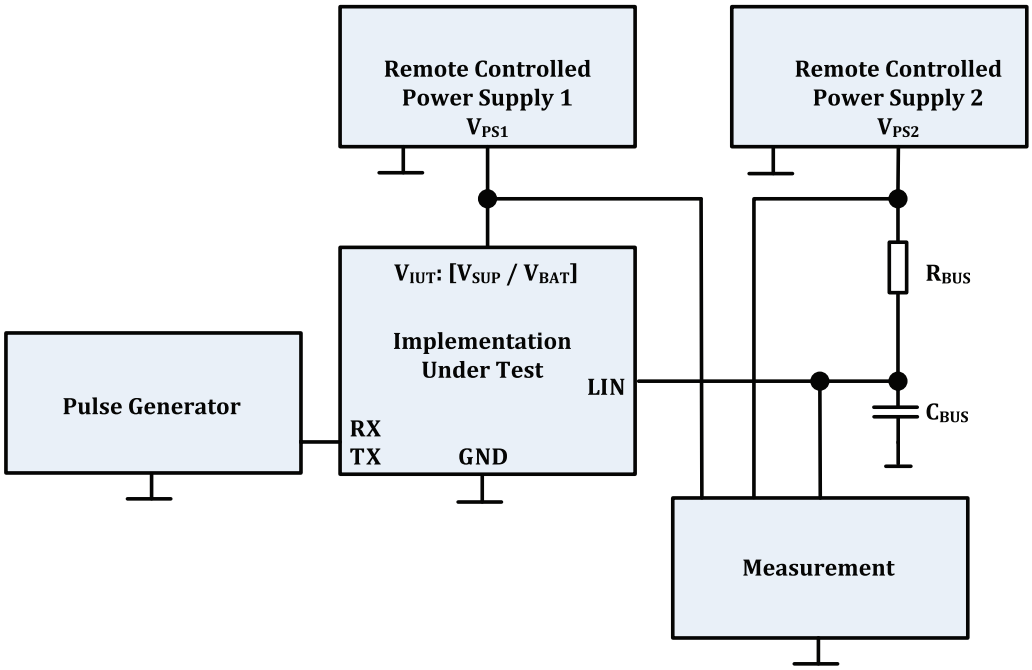

Figure 11 — Test system: Slope control

Table 20 defines the test system "Slope control".

Table 20 — Test system: Slope control

IUT node as	Class B device as master or slave Class A device	[EPL–CT 9].1 to [EPL–CT 9].18
Initial state	**Operational conditions:**	
	Bus loads V_{IUT}: [V_{SUP}/V_{BAT}] V_{PS2}	See Table 21 See Table 21 See Table 21
Test steps	TXD is driven with a rectangular signal (T = 192 µs) with a duty cycle of 50 %. TXD slope time <500 ns, 100 % voltage swing.	
Response	The measured duty cycle D3 shall be greater or equal than 0,417 for V_{SUP} = [7,0 V to 18 V], the measured duty cycle D4 shall be less than or equal to 0,590 for V_{SUP} = [7,6 V to 18 V]. If V_{SUP} is not accessible, then V_{BAT} – 0,7 V shall be used for calculation of the duty cycle.	
Reference	ISO 17987–4:2016, Table 12, Param 29, Param 30 ISO 17987–4:2016, Figure 5	

Table 21 defines the test cases "Slope control".

Table 21 — Test cases: Slope control

EPL–CT–TC	V_{IUT}: [V_{SUP}/V_{BAT}] (PS 1)	V_{PS2} (PS 2)	Bus loads (C_{BUS}; R_{BUS})	Duty cycle	
				D3 Min.	D4 Max.
[EPL–CT 9].1	7,0 V/8,0 V	6,0 V	1 nF (1 %); 1 kΩ (0,1 %)	0,417	—
[EPL–CT 9].2	7,0 V/8,0 V	6,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,417	—
[EPL–CT 9].3	7,0 V/8,0 V	6,0 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,417	—
[EPL–CT 9].4	7,0 V/8,0 V	6,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,417	—
[EPL–CT 9].5	7,0 V/8,0 V	6,0 V	10 nF (1 %); 500 Ω (0,1 %)	0,417	—

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Table 21 *(continued)*

EPL–CT–TC	V_{IUT}: [V_{SUP}/V_{BAT}] (PS 1)	V_{PS2} (PS 2)	Bus loads (C_{BUS}; R_{BUS})	Duty cycle	
				D3 Min.	D4 Max.
[EPL–CT 9].6	7,0 V/8,0 V	6,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,417	—
[EPL–CT 9].7	7,6 V/8,6 V	6,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,417	0,590
[EPL–CT 9].8	7,6 V/8,6 V	7,2 V	1 nF (1 %); 1 kΩ (0,1 %)	0,417	0,590
[EPL–CT 9].9	7,6 V/8,6 V	6,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,417	0,590
[EPL–CT 9].10	7,6 V/8,6 V	7,2 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,417	0,590
[EPL–CT 9].11	7,6 V/8,6 V	6,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,417	0,590
[EPL–CT 9].12	7,6 V/8,6 V	7,2 V	10 nF (1 %); 500 Ω (0,1 %)	0,417	0,590
[EPL–CT 9].13	18 V/18,6 V	17,0 V	1 nF (1 %); 1 kΩ (0,1 %)	0,417	0,590
[EPL–CT 9].14	18 V/18,6 V	17,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,417	0,590
[EPL–CT 9].15	18 V/18,6 V	17,0 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,417	0,590
[EPL–CT 9].16	18 V/18,6 V	17,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,417	0,590
[EPL–CT 9].17	18 V/18,6 V	17,0 V	10 nF (1 %); 500 Ω (0,1 %)	0,417	0,590
[EPL–CT 9].18	18 V/18,6 V	17,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,417	0,590

5.2.6.3 [EPL–CT 10] Measuring the duty cycle at 20,0 kbit/s — IUT as transmitter

Figure 12 shows the test configuration of the test system “Measuring the duty cycle”.

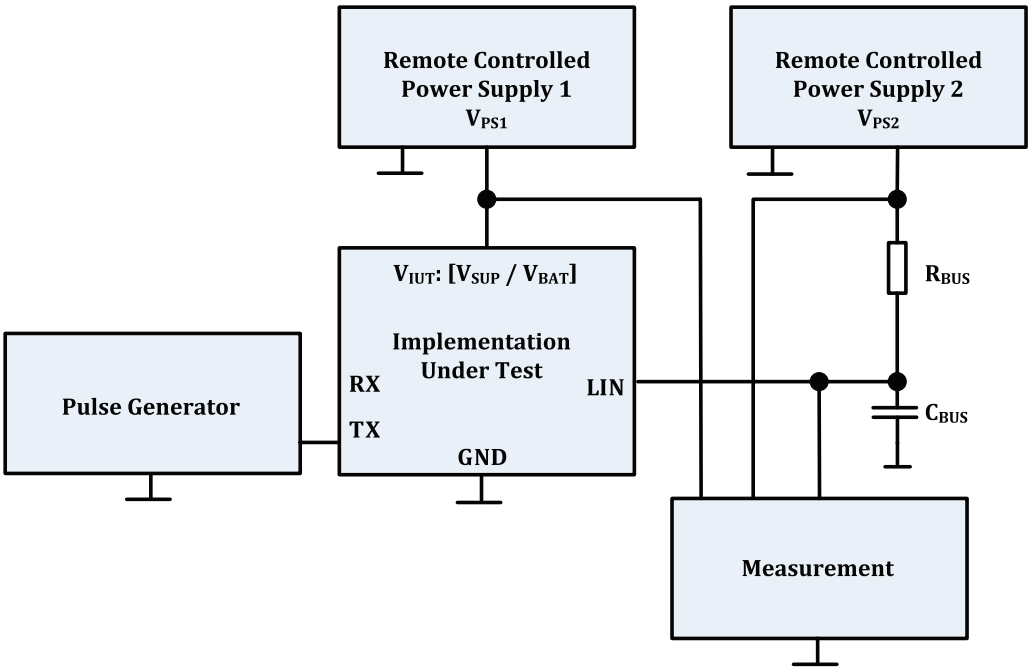

Figure 12 — Test system: Measuring the duty cycle

Table 22 defines the test system “Measuring the duty cycle”.

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Table 22 — Test system: Measuring the duty cycle

IUT node as	Class B device as master or slave Class A device	[EPL–CT 10].1 to [EPL–CT 10].18
Initial state	**Operational conditions:**	
	Bus loads V_{IUT}: [V_{SUP}/V_{BAT}] V_{PS2}	See Table 23 See Table 23 See Table 23
Test steps	TXD is driven with a rectangular signal (T = 100 µs) with a duty cycle of 50 %. TXD slope time <500 ns, 100 % voltage swing.	
Response	The measured duty cycle D1 shall be greater or equal than 0,396 for V_{SUP} = [7,0 V to 18 V], the measured duty cycle D2 shall be less than or equal to 0,581 for V_{SUP} = [7,6 V to 18 V]. If V_{SUP} is not accessible, then V_{BAT} – 0,7 V shall be used for calculation of the duty cycle.	
Reference	ISO 17987–4:2016, Table 12, Param 27, Param 28 ISO 17987–4:2016, Figure 5	

Table 23 defines the test cases “Measuring the duty cycle”.

Table 23 — Test cases: Measuring the duty cycle

EPL–CT–TC	V_{IUT}: [V_{SUP}/V_{BAT}] (PS 1)	V_{PS2} (PS 2)	Bus loads (C_{BUS}; R_{BUS})	Duty cycle	
				D1 Min.	D2 Max.
[EPL–CT 10].1	7,0 V/8,0 V	6,0 V	1 nF (1 %); 1 kΩ (0,1 %)	0,396	—
[EPL–CT 10].2	7,0 V/8,0 V	6,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,396	—
[EPL–CT 10].3	7,0 V/8,0 V	6,0 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,396	—
[EPL–CT 10].4	7,0 V/8,0 V	6,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,396	—
[EPL–CT 10].5	7,0 V/8,0 V	6,0 V	10 nF (1 %); 500 Ω (0,1 %)	0,396	—
[EPL–CT 10].6	7,0 V/8,0 V	6,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,396	—
[EPL–CT 10].7	7,6 V/8,6 V	6,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,396	0,581
[EPL–CT 10].8	7,6 V/8,6 V	7,2 V	1 nF (1 %); 1 kΩ (0,1 %)	0,396	0,581
[EPL–CT 10].9	7,6 V/8,6 V	6,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,396	0,581
[EPL–CT 10].10	7,6 V/8,6 V	7,2 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,396	0,581
[EPL–CT 10].11	7,6 V/8,6 V	6,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,396	0,581
[EPL–CT 10].12	7,6 V/8,6 V	7,2 V	10 nF (1 %); 500 Ω (0,1 %)	0,396	0,581
[EPL–CT 10].13	18 V/18,6 V	17,0 V	1 nF (1 %); 1 kΩ (0,1 %)	0,396	0,581
[EPL–CT 10].14	18 V/18,6 V	17,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,396	0,581
[EPL–CT 10].15	18 V/18,6 V	17,0 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,396	0,581
[EPL–CT 10].16	18 V/18,6 V	17,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,396	0,581
[EPL–CT 10].17	18 V/18,6 V	17,0 V	10 nF (1 %); 500 Ω (0,1 %)	0,396	0,581
[EPL–CT 10].18	18 V/18,6 V	17,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,396	0,581

5.2.7 Propagation delay

5.2.7.1 Overview

The following test checks the receiver’s internal delay and its symmetry. The method for measuring the values is shown in ISO 17987–4:2016, Figure 5.

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5.2.7.2 [EPL–CT 11] Propagation delay of the receiver

Figure 13 shows the test configuration of the test system "Propagation delay".

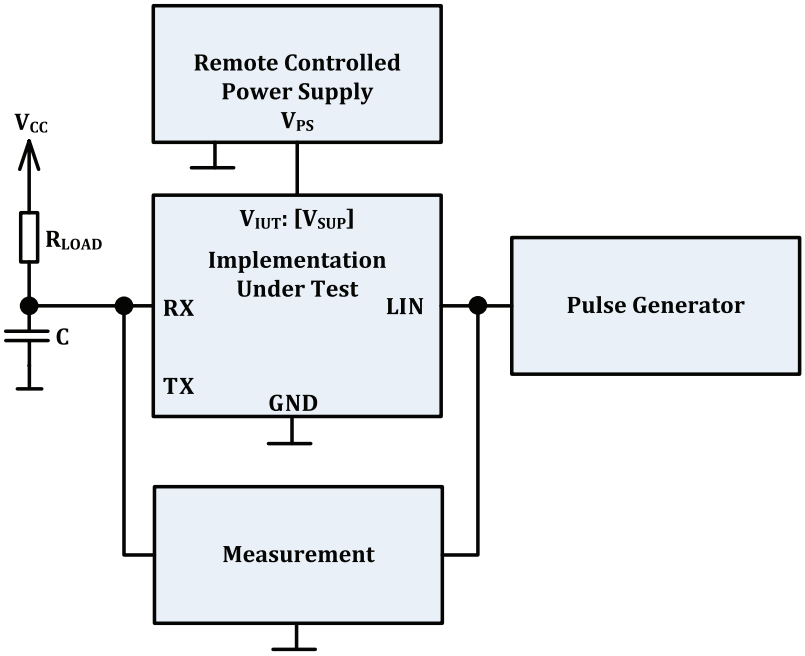

Figure 13 — Test system: Propagation delay

Table 24 defines the test system "Propagation delay".

Table 24 — Test system: Propagation delay

IUT node as	Class A device	[EPL–CT 11].1, [EPL–CT 11].2, [EPL–CT 11].3
Initial state	**Operational conditions:**	
	RXD	C = 20 pF (5 %)
	V_{IUT}: [V_{SUP}]	R_{LOAD} = 2,4 kΩ (0,1 %): pull-up resistor for "open drain" transceiver only; see Table 25
	V_{CC}	Value depends on the tested device (5 V or 3,3V)
Test steps	LIN bus is driven with a 10 kHz rectangular signal with a duty cycle of 50 %, V_{BUS} starts at V_{SUP} and ramps down to 0 V within 20 ns and vice versa.	
Response	The measured time t_{rx_pd} shall be less than 6 µs. $t_{rx_sym} = t_{rx_pdf} - t_{rx_pdr}$ shall be in the range –2 to +2 µs.	
Reference	ISO 17987–4:2016, Table 14, Param 31, 32 ISO 17987–4:2016, Figure 5	

Table 25 defines the test cases "Propagation delay".

Table 25 — Test cases: Propagation delay

EPL–CT–TC	V_{IUT}: [V_{SUP}]
[EPL–CT 11].1	7,0 V
[EPL–CT 11].2	14 V
[EPL–CT 11].3	18 V

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5.2.8 Supply voltage offset

5.2.8.1 Purpose

The purpose of this test is to check the robustness in case of V_{BAT} and ground shift.

5.2.8.2 GND/V_{BAT} shift test — Dynamic

Figure 14 shows the test configuration of the test system "GND — V_{BAT} shift test — Dynamic".

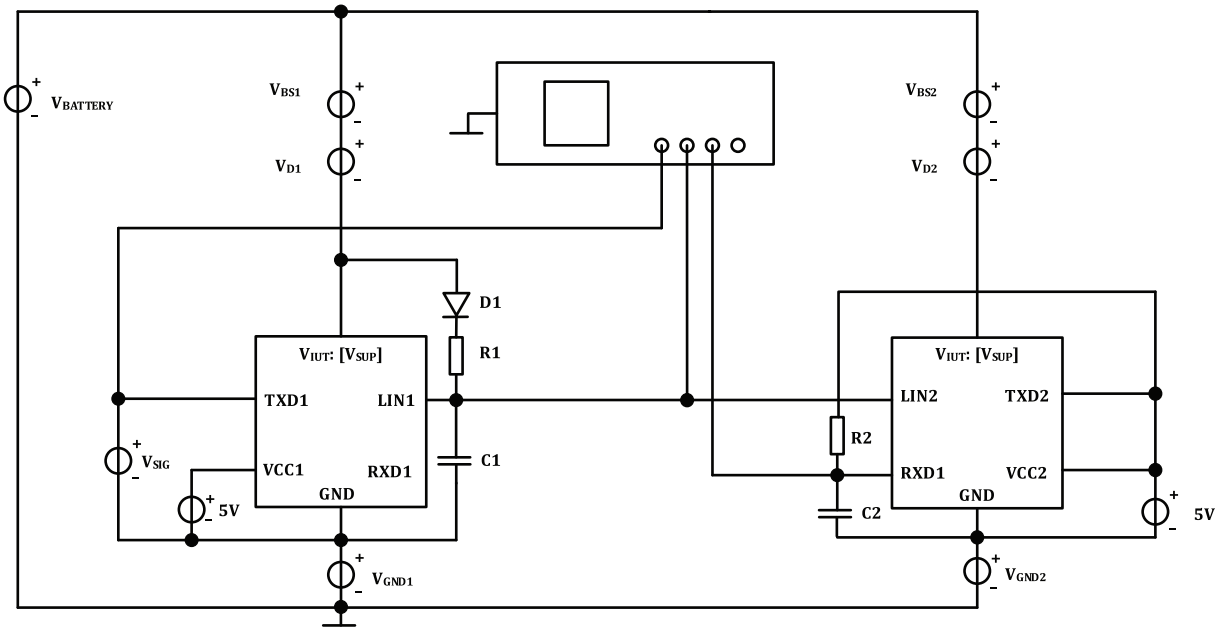

Figure 14 — Test system: GND — V_{BAT} shift test — Dynamic

As a concept, the two operating voltages (V_{CC} and V_{SUP}) are ground-free and completely decoupled from each other; and with that, a superposition with each of these voltages with low frequency and high frequency may be realized independently.

The operating voltages V_{CC} depends on the specific part (3,3 V or 5 V). However, they may be varied indirectly through suitable triggering. The two voltages need independent, ground-free direct current supplies, in order to exclude interconnections.

5.2.8.3 [EPL–CT 12] GND shift test — Dynamic — IUT as a class A device

Table 26 defines the test system "IUT as a class A device".

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Table 26 — Test system: Dynamic — IUT as a class A device

IUT node as	Class A device	[EPL–CT 12].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	0,1 × $V_{BATTERY}$
	V_{D1}	1 V
	V_{GND1}	0,03 × $V_{BATTERY}$
	V_{BS2}	0,03 × $V_{BATTERY}$
	V_{D2}	0,4 V
	V_{GND2}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,376 to 0,601 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987–4:2016, Table 10, Param 23 ISO 17987–4:2016, Table 12, Param 27, 28	

5.2.8.4 [EPL–CT 13] GND shift test — Dynamic — IUT as a class A device

Table 27 defines the test system “Dynamic — IUT as a class A device”.

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Table 27 — Test system: Dynamic — IUT as a class A device

IUT node as	Class A device	[EPL–CT 13].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	0,03 × $V_{BATTERY}$
	V_{D1}	0,4 V
	V_{GND1}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{BS2}	0,1 × $V_{BATTERY}$
	V_{D2}	1 V
	V_{GND2}	0,03 × $V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,376 to 0,601 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987–4:2016, Table 10, Param 23 ISO 17987–4:2016, Table 12, Param 27, 28	

5.2.8.5 [EPL–CT 14] V_{BAT} shift test — Dynamic — IUT as a class A device

Table 28 defines the test system “Dynamic — IUT as a class A device”.

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Table 28 — Test system: Dynamic — IUT as a class A device

IUT node as	Class A device	[EPL–CT 14].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	$[0,5 \times \sin(2 \times \pi \times 5 \times t) + 0,5] \times 0,1 \times V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{D1}	1 V
	V_{GND1}	$0,03 \times V_{BATTERY}$
	V_{BS2}	$0,03 \times V_{BATTERY}$
	V_{D2}	0,4 V
	V_{GND2}	$0,1 \times V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,376 to 0,601 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987–4:2016, Table 10, Param 22 ISO 17987–4:2016, Table 12, Param 27, 28	

5.2.8.6 [EPL–CT 15] V_{BAT} shift test — Dynamic — IUT as a class A device

Table 29 defines the test system “Dynamic — IUT as a class A device.

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Table 29 — Test system: Dynamic — IUT as a class A device

IUT node as	Class A device	[EPL–CT 15].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	0,03 × $V_{BATTERY}$
	V_{D1}	0,4 V
	V_{GND1}	0,1 × $V_{BATTERY}$
	V_{BS2}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{D2}	1 V
	V_{GND2}	0,03 × $V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,376 to 0,601 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987–4:2016, Table 10, Param 22 ISO 17987–4:2016, Table 12, Param 27, 28	

5.2.8.7 [EPL–CT 16] GND shift test — Dynamic — IUT as a class B device

Table 30 defines the test system “IUT as a class B device”.

Table 30 — Test system: Dynamic — IUT as a class B device

IUT node as	Class B device	[EPL-CT 16].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	0,1 × $V_{BATTERY}$
	V_{GND1}	0,03 × $V_{BATTERY}$
	V_{BS2}	0,03 × $V_{BATTERY}$
	V_{D1}	0 V
	V_{D2}	0 V
	V_{GND2}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,376 to 0,601 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987–4:2016, Table 10, Param 23 ISO 17987–4:2016, Table 12, Param 27, 28	

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5.2.8.8 [EPL–CT 17] GND shift test — Dynamic — IUT as a class B device

Table 31 defines the test system "Dynamic — IUT as a class B device".

Table 31 — Test system: Dynamic — IUT as a class B device

IUT node as	Class B device	[EPL-CT 17].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	0,03 × $V_{BATTERY}$
	V_{GND1}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{BS2}	0,1 × $V_{BATTERY}$
	V_{GND2}	0,03 × $V_{BATTERY}$
	V_{D1}	0 V
	V_{D2}	0 V
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,376 to 0,601 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987–4:2016, Table 10, Param 23 ISO 17987–4:2016, Table 12, Param 27, 28	

5.2.8.9 [EPL–CT 18] V_{BAT} shift test — Dynamic — IUT as a class B device

Table 32 defines the test system "Dynamic — IUT as a class B device".

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Table 32 — Test system: Dynamic — IUT as a class B device

IUT node as	Class B device	[EPL-CT 18].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	sinus voltage with 0,1 × $V_{BATTERY}$ amplitude and 0,5 × 0,1 × $V_{BATTERY}$ offset and a frequency of 5 Hz
	V_{GND1}	0,03 × $V_{BATTERY}$
	V_{BS2}	0,03 × $V_{BATTERY}$
	V_{D1}	0 V
	V_{D2}	0 V
	V_{GND2}	0,1 × $V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,376 to 0,601 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987–4:2016, Table 10, Param 22 ISO 17987–4:2016, Table 12, Param 27, 28	

5.2.8.10 [EPL–CT 19] V_{BAT} shift test — Dynamic — IUT as a class B device

Table 33 defines the test system “Dynamic — IUT as a class B device”.

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Table 33 — Test system: Dynamic — IUT as a class B device

IUT node as	Class B device	[EPL-CT 19].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	0,03 × $V_{BATTERY}$
	V_{GND1}	0,1 × $V_{BATTERY}$
	V_{BS2}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{GND2}	0,03 × $V_{BATTERY}$
	V_{D1}	0 V
	V_{D2}	0 V
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,376 to 0,601 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987–4:2016, Table 10, Param 22 ISO 17987–4:2016, Table 12, Param 27, 28	

5.2.9 Failure

5.2.9.1 Purpose

The purpose of this test is to check whether some parasitic reverse currents are flowing into the IUT.

5.2.9.2 [EPL–CT 20] Loss of battery

Figure 15 shows the test configuration of the test system “Loss of battery”.

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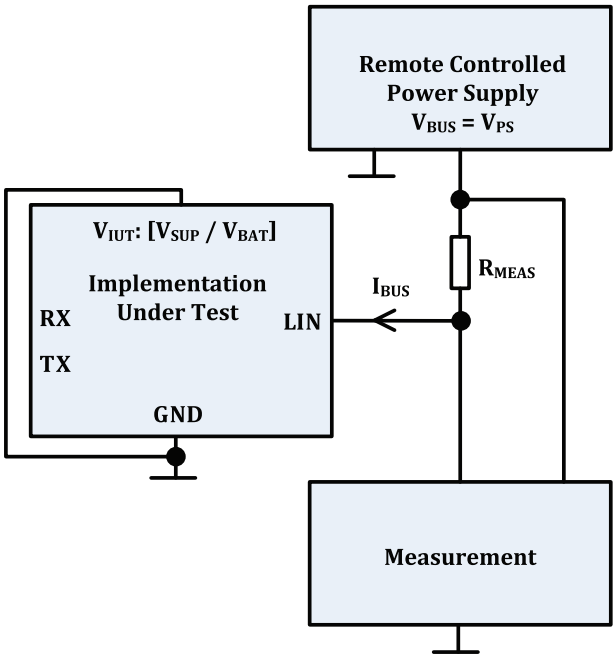

Figure 15 — Test system: Loss of battery

Table 34 defines the test system "Loss of battery".

Table 34 — Test system: Loss of battery

IUT node as	Class B device as master or slave Class A device	[EPL–CT 20].1
Initial state	**Operational conditions:**	
	V_{IUT} = GND Failure $0 < V_{BUS} < 18$ V R_{MEAS}	V_{IUT}: [V_{SUP}/V_{BAT}] Loss of Battery 10 kΩ (0,1 %)
Test steps	The power supply is disconnected from the IUT V_{IUT} PIN. V_{BUS} = Signal with a 2 V/s ramp in the range [0 V to 18 V] up and down.	
Response	During all test, no parasitic current paths shall be formed between the bus line and the IUT. I_{BUS} shall be less than 100 µA, means 1 V voltage drop over R = 10 kΩ. After reconnecting battery line, the IUT shall restart after failure recovery.	
Reference	ISO 17987–4:2016, Table 10, Param 16	

5.2.9.3 [EPL–CT 21] Loss of GND

Figure 16 shows the test configuration of the test system "Loss of GND".

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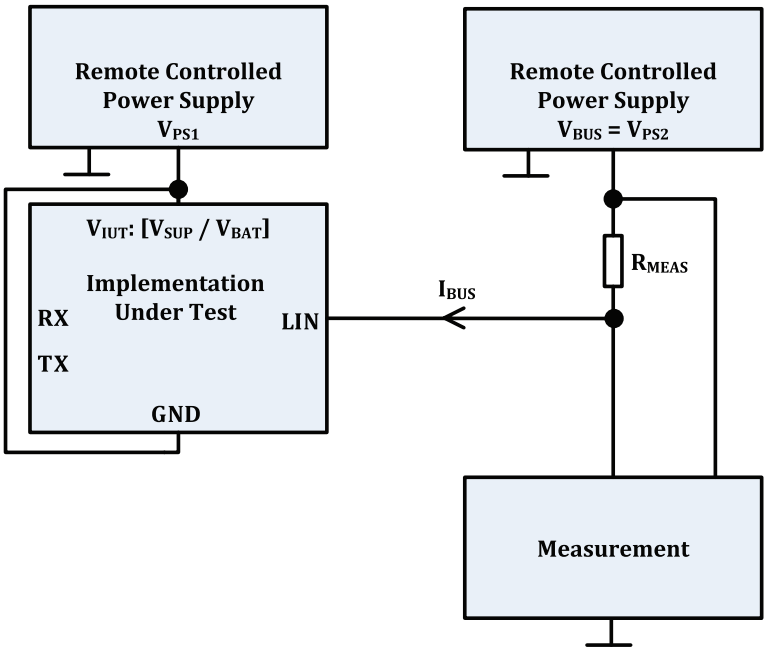

Figure 16 — Test system: Loss of GND

Table 35 defines the test system "Loss of GND".

Table 35 — Test system: Loss of GND

IUT node as	Class B device as slave Class A device	[EPL–CT 21].1
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}] GND_{SUP}/GND_{BAT} = V_{IUT} Failure R_{MEAS}	V_{IUT} = V_{PS1} = 12 V Local GND shorted to V_{IUT} Loss of ground 1 kΩ (0,1 %)
Test steps	The ground is disconnected from the IUT. V_{BUS} = Signal with a 2 V/s ramp in the range [0 V to 18 V] up and down.	
Response	During all test, no parasitic current paths shall be formed between the bus line and the IUT. I_{BUS} shall be included in ±1 mA, means 1 V voltage drop over R = 1 kΩ. After reconnecting ground line, the IUT shall restart after failure recovery.	
Reference	ISO 17987–4:2016, Table 10, Param 15	

5.2.10 [EPL–CT 22] Verifying internal capacitance and dynamic interference — IUT as slave

The purpose of this test is to check the internal capacitance of the IUT under normal and fault conditions.

The IUT shall not interfere dynamically with bus signals when it is in passive (non-transmitting) or unpowered state.

In case of a switchable internal pull-up resistor, the internal pull-up resistor shall be active.

Figure 17 shows the test configuration of the test system "Verifying internal capacitance and dynamic interference — IUT as slave".

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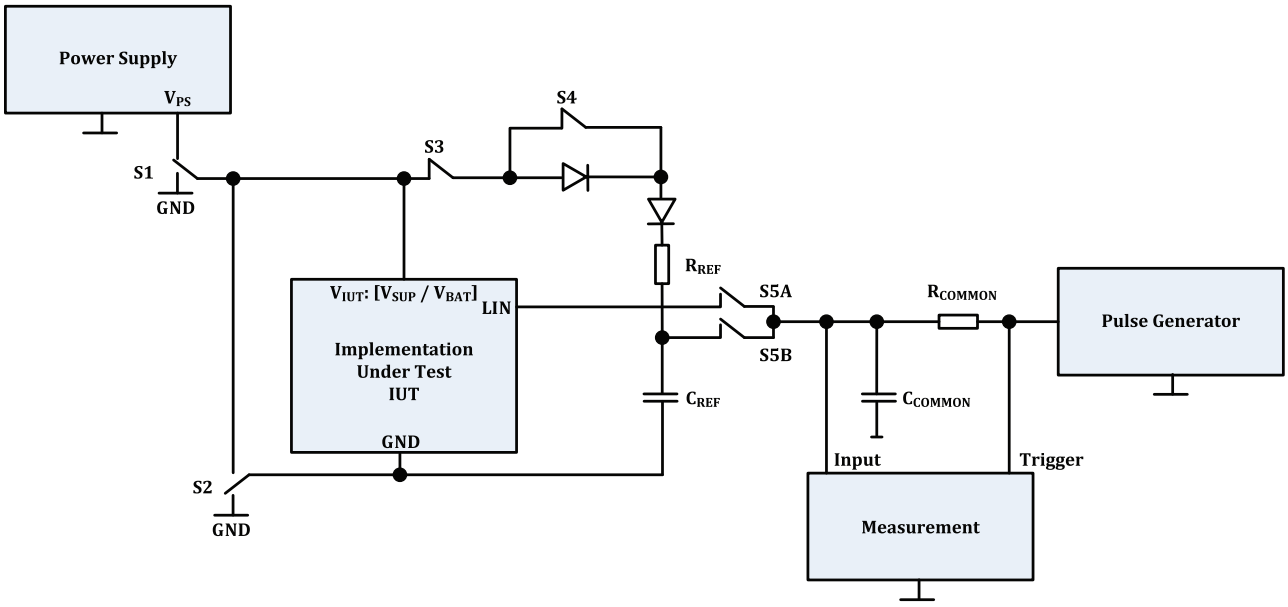

Figure 17 — Test system: Verifying internal capacitance and dynamic interference — IUT as slave

Table 36 defines the test system "Switch settings depending on IUT configuration".

Table 36 — Test system: Switch settings depending on IUT configuration

Switch	Setting
S3	Normally closed. In case where IUT has switchable and deactivated internal pull-up (e.g. in power loss conditions), open S3.
S4	Normally closed. In case where IUT is a 3-pin node or ECU, where reverse polarity protection is included in IUT, open S4.
S5A/B	In case where IUT is connected by a wire harness: During reference measurement, close both S5A and S5B and disconnect IUT from harness. So the harness capacitance is accounted for in the reference.

Table 37 defines the test system "Verifying internal capacitance and dynamic interference — IUT as slave".

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Table 37 — Test system: Verifying internal capacitance and dynamic interference — IUT as slave

IUT node as	Class B device as slave Class A device	[EPL–CT 22].1, [EPL–CT 22].2, [EPL–CT 22].3
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}]	14 V
	R_{COMMON}	1 kΩ (0,1 %)
	C_{COMMON}	750 pF (1,5 nF + 1,5 nF in series) (1 %)
	R_{REF}	30 kΩ (0,1 %)
	C_{REF}	250 pF (100 pF || 150 pF parallel) (1 %)
Test steps	The LIN Bus is driven with a 10 kHz rectangular signal with a duty cycle of 50 %. Rise time ≤20 ns. Slope time measurements are done at 10 %, 90 % of slope voltage. S5B closed: Measuring rise time T_{REF} on a known capacitance of 250 pF + 750 pF. S5A closed: Measuring rise time T_{int} with the IUT internal capacitance + 750 pF.	
Response	C_{SLAVE} shall be less than or equal to 250 pF: $T_{int} \leq T_{REF}$. The IUT shall not interfere with the dynamic stimulus.	
Reference	ISO 17987–4:2016, 5.3.6, Param 37 ISO 17987–4:2016, 5.3.9.2.	

Table 38 defines the test cases “Verifying internal capacitance and dynamic interference — IUT as slave”.

Table 38 — Test cases: Verifying internal capacitance and dynamic interference — IUT as slave

EPL–CT–TC	Condition	S1	S2
[EPL–CT 22].1	Normal power supply IUT shall be in normal mode.	V_{PS}	GND
[EPL–CT 22].2	IUT loss of GND (IUT GND shorted to power supply).	V_{PS}	V_{PS}
[EPL–CT 22].3	IUT loss of V_{PS} (IUT V_{IUT}: [V_{SUP}/V_{BAT}] shorted to GND).	GND	GND

5.3 Operation mode termination

5.3.1 General

An external resistor R_{meas} is switched to the LIN pin. To get the value of the internal resistor, current and voltage shall be measured. These values are gathered for two different settings, and the internal resistance is calculated with Formulae (1), (2), (3) and (4).

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Voltage at R_{int} (with R_{meas1})

$$V_{Rint_meas1} = V_{IUT} - V_{diode} - V_{meas1} = (I_{meas1} - I_{leak1}) \times R_{int} \quad (1)$$

Voltage at R_{int} (with R_{meas2})

$$V_{Rint_meas2} = V_{IUT} - V_{diode} - V_{meas2} = (I_{meas2} - I_{leak2}) \times R_{int} \quad (2)$$

Formula (1) – Formula (2) = Formula (3):

$$\left(V_{IUT} - V_{diode} - V_{meas1}\right) - \left(V_{IUT} - V_{diode} - V_{meas2}\right) = (I_{meas1} - I_{leak1}) \times R_{int} - (I_{meas2} - I_{leak2}) \times R_{int}$$
$$V_{meas2} - V_{meas1} = (I_{meas1} - I_{meas2}) \times R_{int} - (I_{leak1} - I_{leak2}) \times R_{int} \quad (3)$$

with the assumption

$$I_{leak} \sim \text{const} \rightarrow I_{leak1} = I_{leak2}$$

The internal resistor is calculated:

$$R_{int} = \frac{V_{meas2} - V_{meas1}}{I_{meas1} - I_{meas2}} \quad (4)$$

Figure 18 shows the test configuration of the test system "Operation mode".

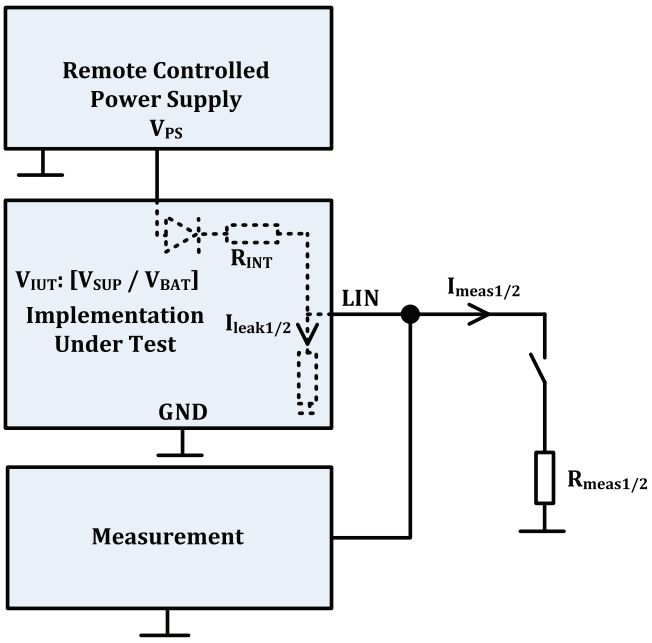

Figure 18 — Test system: Operation mode

5.3.2 [EPL–CT 23] Measuring internal resistor — IUT as slave

Table 39 defines the test system "Measuring internal resistor — IUT as slave".

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Table 39 — Test system: Measuring internal resistor — IUT as slave

IUT node as	Class A device Class B device as slave	
Initial state	**Parameters:**	
	R_{meas1} R_{meas2}	10 kΩ (0,1 %) 20 kΩ (0,1 %)
	Operational conditions:	
	V_{IUT}: [V_{SUP}/V_{BAT}]	14 V
Test steps	The IUT shall be in operational/active mode. There is no communication on the LIN bus. If the IUT incorporates a bus dominant state timeout detection, which disables the IUT's pull-up resistor, the measurement shall take place before a timeout is detected.	
Response	R_{int} value shall be included in the range [20 kΩ; 60 kΩ]; see Formula (4).	
Reference	ISO 17987–4:2016, Table 11, Param 26	

5.3.3 [EPL–CT 24] Measuring internal resistor — IUT as master

Table 40 defines the test system "Measuring internal resistor — IUT as master".

Table 40 — Test system: Measuring internal resistor — IUT as master

IUT node as	Class B device as master	
Initial state	**Parameters:**	
	R_{meas1} R_{meas2}	1 kΩ (0,1 %) 2 kΩ (0,1 %)
	Operational conditions:	
	V_{IUT}: [V_{SUP}/V_{BAT}]	14 V
Test steps	The IUT shall be in operational/active mode. There is no communication on the LIN bus. If the IUT incorporates a bus-dominant state timeout detection, which disables the IUT's pull-up resistor, the measurement shall take place before a timeout is detected.	
Response	R_{int} value shall be included in the range [900 Ω; 1 100 kΩ]; see Formula (4). R_{meas1} = 1 kΩ (0,1 %); R_{meas2} = 2 kΩ (0,1 %).	
Reference	ISO 17987–4:2016, Table 11, Param 25	

5.4 Static test cases

The motivation of static test cases is to check the availability and the boundaries in the datasheet of the IUT. For all integrated circuits, every related parameter in Table 41 shall be part of the datasheet and fulfil the specified boundaries in terms of physical worst case condition. Datasheet parameter names may deviate from the names in Table 41, but in this case, a cross-reference list (datasheet versus Table 41) shall be provided for this test. Parameter conditions may deviate from the conditions in Table 41, if the datasheet conditions are according to the physical worst case context in Table 41 at least.

If one parameter does not pass this test, the result of the whole conformance test is "Failed". See ISO 17987–4:2016, Table 10 and Table 20.

Table 41 defines the test system "LIN static test parameters for datasheets of integrated circuits".

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Table 41 — Test system: LIN static test parameters for datasheets of integrated circuits

No	Reference	Parameter	Min.	Max.	Unit	Comment/ condition	Valid for	Conformance test is passed if value is	
								≤	≥
1.	Param 9	V_{BAT}[a]	8,0	18,0	V	ECU operating voltage range	All devices with integrated reverse polarity diode	Min.	Max.
2.	Param 10	V_{SUP}[b]	7,0	18,0	V	Supply voltage range	All devices without integrated reverse polarity diode	Min.	Max.
3.	Param 11	$V_{SUP_NON_OP}$	−0,3	40,0	V	Voltage range within which the device is not destroyed. An optional time limit for the maximum value shall be at least 400 ms. No guarantee of correct operation.	All devices	Min.	Max.
4.	Param 82	$V_{BUS_MAX_RATINGS}$	−27,0	40,0	V	Voltage range within which the device is not destroyed. An optional time limit for the maximum value shall be at least 400 ms. No guarantee of correct operation.	All devices	Min.	Max.
5.	Param 12	I_{BUS_LIM}[c]	40	200	mA	Current Limitation for Driver dominant state driver on $V_{BUS} = V_{BAT_max}$[d]	All devices with integrated LIN transmitter	Min.	Max.
6.	Param 13	$I_{BUS_PAS_dom}$	−1	—	mA	Input leakage current at the receiver incl. slave pull-up resistor as specified in Param 26 driver off $V_{BUS} = 0$ V $V_{BAT} = 12$ V	All devices with integrated slave pull-up resistor	—	Min.
7.	Param 14	$I_{BUS_PAS_rec}$	—	20	µA	Driver off $8\ V < V_{BAT} < 18\ V$ $8\ V < V_{BUS} < 18\ V$ $V_{BUS} > V_{BAT}$	All devices	Max.	—
8.	Param 15	$I_{BUS_NO_GND}$	−1	1	mA	Control unit disconnected from ground $GND_{Device} = V_{SUP}$ $0\ V < V_{BUS} < 18\ V$ $V_{BAT} = 12$ V Loss of local ground shall not affect communication in the residual network.	All devices	Max.	Min.

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Table 41 *(continued)*

No	Reference	Parameter	Min.	Max.	Unit	Comment/ condition	Valid for	Conformance test is passed if value is	
								≤	≥
9.	Param 16	$I_{BUS_NO_BAT}$	—	100	µA	V_{BAT} disconnected V_{SUP} = GND 0 V < V_{BUS} < 18 V Node shall sustain the current that can flow under this condition. Bus shall remain operational under this condition.	All devices	Max.	—
10.	Param 17	V_{BUS_dom}	—	0,4	V_{SUP}	Receiver dominant state	All devices with integrated LIN receiver	—	Max.
11.	Param 18	V_{BUS_rec}	0,6	—	V_{SUP}	Receiver recessive state	All devices with integrated LIN receiver	Min.	—
12.	Param 19	V_{BUS_CNT}	0,475	0,525	V_{SUP}	$V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2$[e]	All devices with integrated LIN receiver	Max.	Min.
13.	Param 20	V_{HYS}	—	0,175	V_{SUP}	$V_{HYS} = V_{th_rec} - V_{th_dom}$	All devices with integrated LIN receiver	Max.	—
14.	Param 27	D1 (Duty Cycle 1)	0,396	—	—	$TH_{Rec(max)}$ = 0,744 × V_{SUP}; $TH_{Dom(max)}$ = 0,581 × V_{SUP}; V_{SUP} = 7,0 V to 18 V; t_{BIT} = 50 µs; D1 = $t_{Bus_rec(min)}$/(2 × t_{BIT})	All devices with integrated LIN transmitter D1 valid for 20 kbit/s	—	Min.
15.	Param 28	D2 (Duty Cycle 2)	—	0,581	—	$TH_{Rec(min)}$ = 0,422 × V_{SUP}; $TH_{Dom(min)}$ = 0,284 × V_{SUP}; V_{SUP} = 7,6 V to 18 V; t_{BIT} = 50 µs; D2 = $t_{Bus_rec(max)}$/(2 × t_{BIT})	All devices with integrated LIN transmitter D2 valid for 20 kbit/s	Max.	—
16.	Param 29	D3 (Duty Cycle 3)	0,417	—	—	$TH_{Rec(max)}$ = 0,778 × V_{SUP}; $TH_{Dom(max)}$ = 0,616 × V_{SUP}; V_{SUP} = 7,0 V to 18 V; t_{BIT} = 96 µs; D3 = $t_{Bus_rec(min)}$/(2 × t_{BIT})	All devices with integrated LIN transmitter D3 valid for 10,417 kbit/s	—	Min.

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Table 41 *(continued)*

No	Reference	Parameter	Min.	Max.	Unit	Comment/ condition	Valid for	Conformance test is passed if value is	
								≤	≥
17.	Param 30	D4 (Duty Cycle 4)	—	0,590	—	$TH_{Rec(min)}$ = 0,389 × V_{SUP}; $TH_{Dom(min)}$ = 0,251 × V_{SUP}; V_{SUP} = 7,6 V to 18 V; t_{BIT} = 96 µs; D4 = $t_{Bus_rec(max)}$/(2 × t_{BIT})	All devices with integrated LIN transmitter D4 valid for 10,417 kbit/s	Max.	—
18.	Param 31	t_{rx_pd}	—	6	µs	Propagation delay of receiver	All devices with integrated LIN receiver	Max.	—
19.	Param 32	t_{rx_sym}	–2	2	µs	Symmetry of receiver propagation delay rising edge with respect to falling edge	All devices with integrated LIN receiver	Max.	Min.
20.	Param 26	R_{SLAVE}	20	60	kΩ	—	All devices with integrated slave pull-up resistor	Max.	Min.
21.	Param 25	R_{MASTER}	900	1 100	Ω	The serial diode is mandatory. Only for valid for transceiver with integrated master pull-up resistor.	All devices with integrated master pull-up resistor	Max.	Min.
22.	Param 37	C_{SLAVE}	—	250	pF	Capacitance of slave node	All LIN slave devices	Max.	—

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Table 41 *(continued)*

No	Reference	Parameter	Min.	Max.	Unit	Comment/ condition	Valid for	Conformance test is passed if value is	
								≤	≥
23.	6.3.7.1	LIN device states changes	—	—	—	All LIN device state changes on conditional events (e.g. temperature shut–down) shall be specified in the LIN device datasheet.	All devices	—	—
24.	—	LIN transceiver input capacitance	—	—	—	A maximum LIN transceiver input capacitance shall be specified in the LIN device datasheet. Please consider the datasheet limits (e.g. voltage, temperature). The value should be as low as possible.	All devices	—	—

[a] V_{BAT} denotes the supply voltage at the connector of the control unit and may be different from the internal supply V_{SUP} for electronic components (see ISO 17987–4:2016, 5.3.2).

[b] V_{SUP} denotes the supply voltage at the transceiver inside the control unit and may be different from the external supply V_{BAT} for control units (see ISO 17987–4:2016, 5.3.2).

[c] I_{BUS}: Current flowing into the node.

[d] A transceiver shall be capable to sink at least 40 mA. The maximum current flowing into the node shall not exceed 200 mA under DC conditions to avoid possible damage.

[e] V_{th_dom}: receiver threshold of the recessive to dominant LIN bus edge. V_{th_rec}: receiver threshold of the dominant to recessive LIN bus edge.

6 EPL 12 V LIN devices without RX and TX access

This clause addresses class C devices.

6.1 Test specification overview

This test specification is intended for LIN conformance tests of the electrical physical layer of ECUs (see ISO 17987–4) with inaccessible TX and RX pin. This may be the case for integrated devices.

Lacking access to the TX pin, the IUT is stimulated to transmit LIN frames to the bus to test the transmit functions of the device. The LIN frames transmitted by the IUT can then be evaluated by the test system.

Lacking access to the RX pin, the reception of the IUT is tested by establishing a communication between the test system and the IUT.

6.2 Communication scheme

6.2.1 General

Depending on the IUT type (class C device as master/slave), several different communication schemes are used for conformance testing; see 6.2.2 to 6.2.4.

6.2.2 IUT as slave

The following (mandatory) test frames named in concordance with ISO 17987–3 are used for slave tests.

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Table 42 defines the test frames used for slave tests.

Table 42 — Test frames used for slave tests

Test Frame	Requirements for the test frame
TST_FRM_RDBI_0	ReadByIdentifier (Identifier = 0). All other parameters shall be filled with default values according to the IUT specification and according to the test case specification.
TST_HDR_SR_3D	Slave response header, Identifier = $3D_{16}$.

The test system as master, cyclically transmits a TST_FRM_RDBI_0 followed by TST_HDR_SR_3D with a maximum supported bit rate unless defined otherwise by the test case.

One TST_FRM_RDBI_0 followed by a TST_HDR_SR_3D is referred to as one communication cycle. A communication cycle is considered successful if the IUT as slave responds correctly to TST_HDR_SR_3D (with positive or negative response, depending on TST_FRM_RDBI_0).

6.2.3 IUT as master

If possible, a test application is installed on the IUT as master. The test application shall support the following test schemes:

— Bit rate: maximum bit rate supported by master application, unless specified otherwise by test case;

— Checksum model: Enhanced checksum.

The communication between the test system and the IUT shall be implemented as follows:

1) Counter = 0;

2) IUT as master: Transmit a frame header (ID 01_{16}), followed by response of one data byte (counter [00]) and check sum;

3) Test system as slave: If frame is received without errors, store received counter and set transmit flag;

4) IUT as master: Transmit frame header (ID 02_{16});

5) Test system as slave: If transmit flag is set, respond with one data byte (stored counter [00]) and check sum, and clear transmit flag;

6) IUT as master: If test system has answered without errors and received counter value == transmitted counter value, increment counter by 1;

7) Go to step 2).

One sequence of steps 2) to 7) is referred to as one communication cycle. A communication cycle is considered successful if the counter is incremented in step 6) verified by the test system in consecutive communication cycle).

There shall be a possibility to deactivate transmission of LIN headers by the IUT (e.g. by setting an input pin), so that the LIN bus remains recessive.

If bit rates of both higher than 10,417 kbit/s and lower than or equal to 10,417 kbit/s are supported by the application, there shall be a possibility to select between maximum bit rate and 10,417 kbit/s or lower (e.g. by setting an input pin).

If no test software can be installed on the IUT as a master (e.g. integrated device), a device-specific communication scheme is used which allows verification if the IUT as master correctly receives responses from the test system.

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6.2.4 IUT class C device

6.2.4.1 General

For class C devices (e.g. microcontrollers with integrated transceiver or SBCs with integrated UART and transceiver), a test application is required.

The type of test application depends on the type of integrated device.

6.2.4.2 IUT class C device as slave

This device type only supports slave applications.

For conformance testing, the IUT class C device as slave is supplied with a test application which shall support the following test schemes:

— Application can adapt to all bit rates supported by the device;

— Checksum model: Enhanced checksum.

The communication between the test system and the IUT shall be implemented as follows:

1) Counter = 0;

2) Test System as master: Transmit a frame header (ID 01_{16}), followed by response of one data byte (counter [00]) and checksum;

3) IUT as slave: If frame is received without errors, store received counter and set transmit flag;

4) Test System as master: Transmit frame header (ID 02_{16});

5) IUT as slave: If transmit flag is set, respond with one data byte (stored counter [00]) and check sum, and clear transmit flag;

6) Test System as master: If IUT as slave has answered without errors and received counter value == transmitted counter value, increment counter by 1;

7) Go to step 2).

One sequence of steps 2) to 7) is referred to as one communication cycle. A communication cycle is considered successful, if the counter is incremented in step 6).

6.2.4.3 IUT as a class C device as master

This device type only supports master applications.

If the IUT does not have an integrated master pull-up resistor, it shall be equipped with an external pull-up circuitry as specified in the IUT's datasheet. If the IUT's datasheet does not specify a pull-up circuitry, the circuitry as described in Figure 19 is used.

Figure 19 shows the default master pull-up circuitry.

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