BS ISO 18257:2016

BSI Standards Publication

Space systems — Semiconductor integrated circuits for space applications — Design requirements

Documents
Document Sharing Hub

Full document details: BS ISO 18257:2016

National foreword

This British Standard is the UK implementation of ISO 18257:2016.

The UK participation in its preparation was entrusted to Technical Committee ACE/68, Space systems and operations.

A list of organizations represented on this committee can be obtained on request to its secretary.

This publication does not purport to include all the necessary provisions of a contract. Users are responsible for its correct application.

© The British Standards Institution 2016.
Published by BSI Standards Limited 2016

ISBN 978 0 580 87096 5

ICS 49.140

Compliance with a British Standard cannot confer immunity from legal obligations.

This British Standard was published under the authority of the Standards Policy and Strategy Committee on 30 November 2016.

Amendments/corrigenda issued since publication

Date	Text affected

Documents
Document Sharing Hub

Full document details: BS ISO 18257:2016

INTERNATIONAL STANDARD

ISO 18257

First edition
2016-11-15

Space systems — Semiconductor integrated circuits for space applications — Design requirements

Systèmes spatiaux — Circuits intégrés semi-conducteurs d'applications spatiales — Exigences de conception

Reference number
ISO 18257:2016(E)

Documents
Document Sharing Hub

© ISO 2016

Full document details: BS ISO 18257:2016

COPYRIGHT PROTECTED DOCUMENT

© ISO 2016, Published in Switzerland

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized otherwise in any form or by any means, electronic or mechanical, including photocopying, or posting on the internet or an intranet, without prior written permission. Permission can be requested from either ISO at the address below or ISO's member body in the country of the requester.

ISO copyright office
Ch. de Blandonnet 8 • CP 401
CH-1214 Vernier, Geneva, Switzerland
Tel. +41 22 749 01 11
Fax +41 22 749 09 47
copyright@iso.org
www.iso.org

© ISO 2016 – All rights reserved

Documents
Document Sharing Hub

Full document details: BS ISO 18257:2016

Contents

Page

Foreword ... **iv**
Introduction ... **v**
1 Scope ... **1**
2 Normative references ... **1**
3 Terms and definitions ... **1**
4 Abbreviated terms ... **2**
5 General requirements ... **2**
6 Design process ... **3**
6.1 Overview ... 3
6.2 Design input ... 5
6.3 Design phases and tasks ... 6
6.3.1 Architecture design ... 6
6.3.2 Logic design and circuit design ... 7
6.3.3 Layout design ... 8
6.4 Mask making, package and testing ... 10
7 Detailed requirements ... **10**
7.1 Architectural design requirements ... 10
7.2 Logic design and circuit design requirements ... 10
7.3 Layout design requirements ... 11
7.4 Package design requirements ... 11
7.4.1 Package structure design requirements ... 11
7.4.2 Packaging technology design requirements ... 12
7.4.3 Packaging electrical simulation analysis requirements ... 12
7.4.4 Packaging thermal simulation analysis ... 12
7.5 Reliability design requirements ... 12
7.5.1 Overview ... 12
7.5.2 Reliability design requirements ... 13
7.5.3 Antistatic design requirements ... 13
7.5.4 Low-power design requirements ... 13
7.5.5 Parameter modification and design margin optimization requirements ... 14
7.5.6 Electromagnetic compatibility design requirements ... 14
7.5.7 Radiation-hardened design requirements ... 14
7.6 Testability design requirements ... 15
Annex A (normative) **Datasheet** ... **16**
Annex B (informative) **Guidance** ... **17**
Bibliography ... **24**

© ISO 2016 – All rights reserved

Documents
Document Sharing Hub
Full document details: BS ISO 18257:2016

Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO shall not be held responsible for identifying any or all such patent rights. Details of any patent rights identified during the development of the document will be in the Introduction and/or on the ISO list of patent declarations received (see www.iso.org/patents).

Any trade name used in this document is information given for the convenience of users and does not constitute an endorsement.

For an explanation on the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT) see the following URL: www.iso.org/iso/foreword.html.

The committee responsible for this document is ISO/TC 20, *Aircraft and space vehicles*, Subcommittee SC 14, *Space systems and operations*.

© ISO 2016 – All rights reserved
Documents
Document Sharing Hub
Full document details: BS ISO 18257:2016

Introduction

Normative design requirements of semiconductor integrated circuits for space applications largely determine the reliability of an integrated circuit (IC) and its adaptability to space environment, thereby affecting the reliability of space systems. IC tests and experiments based on product specification only can provide a comprehensive evaluation of its reliability. Once applied to space systems, the design flaws will directly affect the implementation of aerospace engineering. The development of design requirements for semiconductor ICs for space applications can ensure its reliability and space suitability from its very source to meet the space application requirements.

© ISO 2016 – All rights reserved

Documents
Document Sharing Hub
Full document details: BS ISO 18257:2016

Documents
Document Sharing Hub

INTERNATIONAL STANDARD ISO 18257:2016(E)

Space systems — Semiconductor integrated circuits for space applications — Design requirements

1 Scope

This document specifies the basic design requirements for semiconductor ICs for space applications, including its design process, as well as required tasks and requirements of each stage. Requirements of specific circuit design are not included.

2 Normative references

The following documents are referred to in text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61967-2, *Integrated circuits — Measurement of electromagnetic emissions*

IEC 62132, *Integrated circuits — Measurement of electromagnetic immunity*

IEC 62215-3:2013, *Integrated circuits — Measurement of impulse immunity — Part 3: Non-synchronous transient injection method*

IEEE 1149.1, *IEEE standard for test access port and boundary — Scan architecture*

3 Terms and definitions

For the purposes of this document, the terms defined in ISO 10795 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— IEC Electropedia: available at http://www.electropedia.org/

— ISO Online browsing platform: available at http://www.iso.org/obp

3.1
programmable logic device
PLD
hardware-programmable device

EXAMPLE FPGA, CPLD, etc.

3.2
suitability
degree to which a product meets its requirements

3.3
environment adaptability
ability to achieve the entire product's intended functions, performance and (or) capacity for protecting itself under various environments within its life cycle

3.4
testability
ability to perform function and performance testing of the circuit, position the failure of the circuit and select qualified circuit chip as soon as possible

© ISO 2016 – All rights reserved

Documents
Document Sharing Hub
Full document details: BS ISO 18257:2016

4 Abbreviated terms

ASIC	application specific integrated circuit
BIST	built-in self test
CMOS	complementary metal oxide semiconductor
DFT	design for test
DRC	design rule checking
EMC	electro-magnetic compatibility
ERC	electrical rule checking
ESD	electrostatic discharge
FPGA	field programmable gate array
IC	integrated circuit
I/O	input/output
IP	intellectual property
JFET	junction field effect transistor
MOSFET	metallic oxide semiconductor field effect transistor
NMOS	N-channel metal oxide semiconductor
RAM	random access memory
RC	resistance capacitance
ROM	read only memory
RTL	register transfer level
SAR ADC	successive approximation register analogue digital converter
SCR	silicon controlled rectifier
SEL	single event latch-up
SET	single event transient
SEU	single event upset
SOI	silicon on insulator
SOS	silicon on sapphire

5 General requirements

General requirements in designing semiconductor ICs for space applications include:

a) process conducted under a fault-tolerant system with design requirements;

NOTE 1 Special implements are allowed for different types of ICs for space applications.

© ISO 2016 – All rights reserved
Documents
Document Sharing Hub
Full document details: BS ISO 18257:2016

b) adherence to existing standards and regulations during the design process;

c) feasibility and risk analysis of requirements from aerospace customer to validate the rationality of its functional and performance requirements;

d) conversion of users' requirements into design input, which may involve the following steps:

   1) derating the design criteria;

   NOTE 2 Derate on the basis of nominal stress according to the stress of the circuit. The key is the level and effects. Derating can improve reliability, but takes into consideration issues such as reliability, size, weight and cost.

   2) applying fault-tolerant design and adopting rational use of redundant technology;

   3) ensuring the characteristics of the orbit thermal environment for reliable thermal design;

   4) considering radiation hardness to ensure grade requirements, if necessary;

   5) taking note of the life of customer's requirements (mean time to failure);

e) decomposition of the design input requirements to each design stage according to its tasks.

   NOTE 3 Implement and validate each step until all objectives and requirements of a semiconductor IC for space applications are achieved.

6 Design process

6.1 Overview

IC designs generally include architecture design, logic design, circuit design and layout design. In order to ensure the validity of the design, computer simulation and verification of its results at each stage are necessary. Figure 1 illustrates the IC design flow.

© ISO 2016 – All rights reserved

Documents
Document Sharing Hub
Full document details: BS ISO 18257:2016