BS ISO/IEC 10373-6:2016+A3:2018

BSI Standards Publication

Identification cards — Test methods

Part 6: Proximity cards

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National foreword

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The start and finish of text introduced or altered by amendment is indicated in the text by tags. Tags indicating changes to ISO/IEC text carry the number of the ISO/IEC amendment. For example, text altered by ISO/IEC amendment 3 is indicated by A3〉 〈A3.

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Third edition
2016-07-15

Identification cards — Test methods —

Part 6: Proximity cards

Cartes d'identification — Méthodes d'essai —

Partie 6: Cartes de proximité

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Contents

Page

Foreword v

1 Scope 1

2 Normative references 1

3 Terms, definitions, symbols and abbreviated terms 2
3.1 Terms and definitions 2
3.2 Symbols and abbreviated terms 3

4 Default items applicable to the test methods 5
4.1 Test environment 5
4.2 Pre-conditioning 5
4.3 Default tolerance 5
4.4 Spurious inductance 6
4.5 Total measurement uncertainty 6

5 Apparatus and circuits for test of ISO/IEC 14443-1 and ISO/IEC 14443-2 parameters 6
5.1 Minimum requirements for measurement instruments 6
5.1.1 Oscilloscope 6
5.2 Calibration coils 6
5.2.1 Size of the calibration coil card 6
5.2.2 Thickness and material of the calibration coil card 7
5.2.3 Coil characteristics 7
5.3 Test PCD assembly 7
5.3.1 Test PCD antenna 8
5.3.2 Sense coils 9
5.3.3 Assembly of Test PCD 9
5.4 Reference PICC 10
5.4.1 Dimensions of the Reference PICC 10
5.4.2 Reference PICC construction 10
5.4.3 Reference PICC resonance frequency tuning 12
5.5 EMD test setup 13
5.5.1 General description 13
5.5.2 Computation of power versus time 13
5.5.3 Noise floor precondition test 14

6 Test of ISO/IEC 14443-1 parameters 14
6.1 PCD tests 14
6.1.1 Alternating magnetic field 14
6.2 PICC tests 15
6.2.1 Alternating magnetic field 15
6.2.2 Static electricity test 16
6.3 PXD tests 17

7 Test of ISO/IEC 14443-2 parameters 18
7.1 PCD tests 18
7.1.1 PCD field strength 18
7.1.2 Void 19
7.1.3 Void 19
7.1.4 Modulation index and waveform 19
7.1.5 Load modulation reception 20
7.1.6 PCD EMD immunity test 21
7.1.7 PCD EMD recovery test 22
7.2 PICC tests 23

Documents
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Full document details: BS ISO/IEC 10373-6:2016+A3:2018

7.2.1 PICC transmission 23
7.2.2 PICC EMD level and low EMD time test 25
7.2.3 PICC reception 26
7.2.4 PICC resonance frequency (informative) 27
7.2.5 PICC maximum loading effect 28
7.3 Test methods for bit rates of 3*fc*/4, *fc*, 3*fc*/2 and 2*fc* from PCD to PICC 29
7.4 PXD tests 29

8 Test of ISO/IEC 14443-3 and ISO/IEC 14443-4 parameters 29
8.1 PCD tests 29
8.2 PICC tests 29
8.3 PXD tests 30
8.3.1 PCD and PICC Modes 30
8.3.2 Automatic mode alternation 30

Annex A (normative) Test PCD antennas 34

Annex B (informative) Test PCD Antenna tuning 43

Annex C (normative) Sense coil 45

Annex D (normative) Reference PICCs 48

Annex E (normative) Modulation index and waveform analysis tool 56

Annex F (informative) Program for the evaluation of the spectrum 111

Annex G (normative) Additional PICC test methods 117

Annex H (normative) Additional PCD test methods 179

Annex I (normative) High bit rate selection test methods for PCD 218

Annex J (informative) Program for EMD level measurements 232

Annex K (normative) Test methods for bit rates of 3*fc*/4, *fc*, 3*fc*/2 and 2*fc* from PCD to PICC 245

Annex L (normative) Frame with error correction test methods 331

Bibliography 340

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Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work. In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular the different approval criteria needed for the different types of document should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

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The committee responsible for this document is ISO/IEC JTC 1, *Information technology*, Subcommittee SC 17, *Cards and personal identification*.

This third edition cancels and replaces the second edition (ISO/IEC 10373-6:2011), which has been technically revised.

It also incorporates the Amendments ISO/IEC 10373-6:2011/Amd 1:2012, ISO/IEC 10373-6:2011/Amd 2:2012, ISO/IEC 10373-6:2011/Amd 3:2012, ISO/IEC 10373-6:2011/Amd 4:2012, and the Technical Corrigendum ISO/IEC 10373-6:2011/Cor 1:2013.

ISO/IEC 10373 consists of the following parts, under the general title Identification cards — Test methods:

— *Part 1: General characteristics*

— *Part 2: Cards with magnetic stripes*

— *Part 3: Integrated circuit cards with contacts and related interface devices*

— *Part 5: Optical memory cards*

— *Part 6: Proximity cards*

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— *Part 7: Vicinity cards*

— *Part 8: USB-ICC*

— *Part 9: Optical memory cards — Holographic recording method*

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Identification cards — Test methods — Part 6: Proximity cards

1 Scope

ISO/IEC 10373 defines test methods for characteristics of identification cards according to the definition given in ISO/IEC 7810. Each test method is cross-referenced to one or more base standards, which can be ISO/IEC 7810 or one or more of the supplementary standards that define the information storage technologies employed in identification card applications.

NOTE 1 Criteria for acceptability do not form part of ISO/IEC 10373, but will be found in the International Standards mentioned above.

NOTE 2 Test methods defined in this part of ISO/IEC 10373 are intended to be performed separately. A given proximity card or object, or proximity coupling device, is not required to pass through all the tests sequentially.

This part of ISO/IEC 10373 defines test methods which are specific to proximity cards and objects, and proximity coupling devices and proximity extended devices, defined in ISO/IEC 14443-1, ISO/IEC 14443-2, ISO/IEC 14443-3, and ISO/IEC 14443-4.

ISO/IEC 10373-1 defines test methods which are common to one or more integrated circuit card technologies and other parts deal with other technology-specific tests.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 7810, *Identification cards — Physical characteristics*

ISO/IEC 14443-1:2016, *Identification cards — Contactless integrated circuit cards — Proximity cards — Part 1: Physical characteristics*

ISO/IEC 14443-2:2016, *Identification cards — Contactless integrated circuit cards — Proximity cards — Part 2: Radio frequency power and signal interface*

ISO/IEC 14443-3:2016, *Identification cards — Contactless integrated circuit cards — Proximity cards — Part 3: Initialization and anticollision*

ISO/IEC 14443-4:2016, *Identification cards — Contactless integrated circuit cards — Proximity cards — Part 4: Transmission protocol*

IEC 61000-4-2:2008, *Electromagnetic compatibility (EMC) — Part 4-2: Testing and measurement techniques — Electrostatic discharge immunity test*

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3 Terms, definitions, symbols and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO/IEC 14443-1, ISO/IEC 14443-2, ISO/IEC 14443-3, and ISO/IEC 14443-4, and the following apply.

NOTE Elements in bold square brackets **[ ]** are optional definitions.

3.1.1
base standard
standard which the test method is used to verify conformance to

3.1.2
CascadeLevels
number of cascade levels of the PICC

3.1.3
Command Set
set describing the PICC commands during initialization and anticollision

Note 1 to entry: See ISO/IEC 14443-3:2016, 6.4 for PICC Type A and ISO/IEC 14443-3:2016, 7.5 for PICC Type B.

3.1.4
loading effect
change in PCD antenna current caused by the presence of PICC(s) in the field due to the mutual coupling modifying the PCD antenna resonance and quality factor

3.1.5
mute
no response within a specified timeout, e.g. expiration of FWT

3.1.6
PICC states
different PICC states during initialization and anticollision

Note 1 to entry: See ISO/IEC 14443-3:2016, 6.3 for PICC Type A and ISO/IEC 14443-3:2016, 7.4 for PICC Type B.

3.1.7
scenario
defined typical protocol and application specific communication to be used with the test methods defined in this part of ISO/IEC 10373

3.1.8
Test Initial State
TIS
element from PICC states that is the PICC state before performing a specific PICC command from Command Set

3.1.9
test method
method for testing characteristics of identification cards for the purpose of confirming their compliance with International Standards

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3.1.10
Test Target State
TTS
element from PICC states that is the PICC state after performing a specific PICC command from Command Set

3.2 Symbols and abbreviated terms

(xxxxx)b	Data bit representations
'XY'	Hexadecimal notation, equal to XY in base 16
ATA(cid)	Answer to ATTRIB, i.e. (mbli+cid CRC_B), with mbli an arbitrary hex value (see ISO/IEC 14443-3:2016, 7.11)
ATTRIB(cid, fsdi)	Default ATTRIB command with PUPI from ATQB, CID = cid and Maximum Frame Size Code value = fsdi, i.e. ('1D' PUPI cid fsdi '01 00' CRC_B)
DUT	Device under test
ESD	Electrostatic Discharge
$I(c)_n$**(**inf **[**,CID = cid**]** **[**,NAD = nad**]** **[**,~CRC**])**	ISO/IEC 14443-4 I-block with chaining bit c∈{1,0}, block number n∈{1,0} and information field inf. By default no CID and no NAD will be transmitted. If CID = cid∈{0...15} is specified, it will be transmitted as second parameter. If NAD = nad∈{0...'FF'} is specified, it will be transmitted as third parameter (or second parameter if no CID is transmitted). If the literal '~CRC' is not specified, a valid CRC corresponding to the type of the PICC will be transmitted by default (i.e. CRC_A or CRC_B)
IUT	Implementation Under Test (ISO/IEC 9646); within the scope of this part of ISO/IEC 10373, IUT represents the PCD under the test
LT	Lower Tester (ISO/IEC 9646), the PICC-emulation part of the PCD-test-apparatus
m	Modulation index
Mute	No response within a specified timeout
N/A	Not applicable
PPS(cid, dri, dsi)	Default PPS request with CID = cid, DRI = dri and DSI = dsi, i.e. ('D' + cid '11' dsi × 4 + dri CRC_A)
$R(ACK$ **[**,CID = cid**]** **[**,~CRC**])**$_n$	ISO/IEC 14443-4 R(ACK) block with block number n. The definition of the optional CID and ~CRC symbols is as described in the $I(c)_n$ block above
$R(NAK$ **[**,CID = cid**][**,~CRC**])**$_n$	ISO/IEC 14443-4 R(NAK) block with block number n. The definition of the optional CID and ~CRC symbols is as described in the $I(c)_n$ block above
RATS(cid, fsdi)	Default RATS command with CID = cid and FSDI value = fsdi i.e. ('E0' fsdi × 16 + cid CRC_A)
READY(I)	READY state in cascade level I, I ∈ {1, 2, 3}; e.g. READY(2) is a PICC cascade level 2

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READY*(I)	READY* state in cascade level I, I ∈ {1, 2, 3}; e.g. READY*(2) is a PICC cascade level 2
REQB(N)	REQB command with N as defined in ISO/IEC 14443-3:2016, 7.7
S(WTX)(WTXM [,CID = cid][,~CRC])	ISO/IEC 14443-4 S(WTX) block with parameter WTXM. The definition of the optional CID and ~CRC symbols is as described in the $I(c)_n$ block above
S(DESELECT **[**,CID = cid**]** **[**,~CRC**]**)	ISO/IEC 14443-4 S(DESELECT) block. The definition of the optional CID and ~CRC symbols is as described in the $I(c)_n$ block above
SAK(cascade)	the SELECT(I) answer with the cascade bit (bit 3) set to (1)b
SAK(complete)	the SELECT(I) answer with the cascade bit (bit 3) set to (0)b
SEL(c)	Select code of level c (i.e. SEL(1) = '93', SEL(2) = '95', SEL(3) = '97')
SELECT(I)	SELECT command of cascade level I, i.e. SELECT(1) = ('93 70' $UIDTX_1$ BCC CRC_A) SELECT(2) = ('95 70' $UIDTX_2$ BCC CRC_A) SELECT(3) = ('97 70' $UIDTX_3$ BCC CRC_A)
SLOTMARKER(n)	Slot-MARKER command with slot number n, i.e. (16 × (n − 1) + 5 CRC_B)
TB-PDU	Transmission Block Protocol Data Unit, which consists of either I-block, R-block or S-block
TEST_COMMAND1(1)	Default test command consisting of one unchained I-block NOTE This command depends on the negotiated maximum frame size value of the PICC.
TEST_COMMAND1(n), n > 1	Default test command consisting of n chained I-blocks (PCD chaining) NOTE This command depends on the negotiated maximum frame size value of the PICC.
$TEST_COMMAND1(n)_k$	INF field of k'th I-block chain of TEST_COMMAND1(n) NOTE This command depends on the negotiated maximum frame size value of the PICC.
TEST_COMMAND2(n), n > 1	Default test command which expects a response consisting of n chained I-blocks NOTE This command depends on the negotiated maximum frame size value of the PCD.
TEST_COMMAND3	Default test command consisting of one I-block which needs more than FWT time for execution
TEST_RESPONSE1(n)	INF field of the response to TEST_COMMAND1(n) NOTE This response is assumed to be always unchained.
TEST_RESPONSE2(n)	Response to TEST_COMMAND2(n) NOTE This response depends on the negotiated maximum frame size value of the PCD.

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$TEST_RESPONSE2(n)_k$	INF field of k'th I-block chain of TEST_RESPONSE2(n) NOTE This response depends on the negotiated maximum frame size value of the PCD.
TEST_RESPONSE3	Response I-block to TEST_COMMAND3 NOTE This response is always assumed to be unchained.
TM-PDU	Test Management Protocol Data Unit (ISO/IEC 9646-1, PDU)
t_{START}	Start of PICC transmission
$UIDTX_I$	Transmitted UID 32-bit data at cascade level I (see Table 1)
UT	Upper Tester (ISO/IEC 9646), the master part of the PCD-test-apparatus
UT_APDU	Upper Tester Application Protocol Data Unit: a packet of data to be sent by the PCD to the LT through the RF interface
V_{load}	DC voltage measured at connector CON3 of the Reference PICC
WUPB(N)	WUPB command with N as defined in ISO/IEC 14443-3:2016, 7.7
~X	Bit sequence consisting of the inverted bits of bit sequence X or any other bit sequence different from X
X[[a...b]]	Bit subsequence of bit sequence X consisting of the bits between position a and b included. If a > b then the sequence is empty
X[[n]]	Bit at position n of bit sequence X. First bit is at position 1
X[n]	Byte at position n of bit sequence X. First byte is at position 1 (i.e. X[n] = X[[(n − 1) × 8 + 1...n × 8]])

Table 1 — Mapping from UID to UIDTX

Cascade level	Single UID PICC	Double UID PICC	Triple UID PICC
$UIDTX_1$	UID0 UID1 UID2 UID3	'88' UID0 UID1 UID2	'88' UID0 UID1 UID2
$UIDTX_2$	—	UID3 UID4 UID5 UID6	'88' UID3 UID4 UID5
$UIDTX_3$	—	—	UID6 UID7 UID8 UID9

4 Default items applicable to the test methods

4.1 Test environment

Unless otherwise specified, testing shall take place in an environment of temperature 23 °C ± 3 °C (73 °F ± 5 °F) and of relative humidity 40 % to 60 %.

4.2 Pre-conditioning

No environmental pre-conditioning of PICCs or PCDs is required by the test methods in this part of ISO/IEC 10373.

4.3 Default tolerance

Unless otherwise specified, a default tolerance of ±5 % shall be applied to the quantity values given to specify the characteristics of the test equipment (e.g. linear dimensions) and the test method procedures (e.g. test equipment adjustments).

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4.4 Spurious inductance

Resistors and capacitors should have negligible inductance.

4.5 Total measurement uncertainty

The total measurement uncertainty for each quantity determined by these test methods shall be stated in the test report.

Basic information is given in ISO/IEC Guide 98-3.

5 Apparatus and circuits for test of ISO/IEC 14443-1 and ISO/IEC 14443-2 parameters

This Clause defines the test apparatus and test circuits for verifying the operation of a PICC or a PCD according to ISO/IEC 14443-1 and ISO/IEC 14443-2. The test apparatus includes the following:

— measurement instruments (see 5.1);

— calibration coil (see 5.2);

— Test PCD assembly (see 5.3);

— Reference PICC (see 5.4);

— EMD test setup (see 5.5).

These are described in the following clauses.

5.1 Minimum requirements for measurement instruments

5.1.1 Oscilloscope

The digital sampling oscilloscope shall be capable of sampling at a rate of at least 500 million samples per second with a resolution of at least 8 bits at optimum scaling and shall have an overall minimum bandwidth of 250 MHz. The oscilloscope should have the capability to output the sampled data as a text file to facilitate mathematical and other operations such as windowing on the sampled data using software programs (see Annex E and Annex F).

NOTE The overall bandwidth is the combination of oscilloscope and probing system bandwidth.

5.2 Calibration coils

This subclause defines the size, thickness and characteristics of the calibration coils 1 and 2.

Calibration coil 1 shall be used only in Test PCD assembly 1 and calibration coil 2 shall be used only in Test PCD assembly 2.

5.2.1 Size of the calibration coil card

The calibration coil card shall consist of an area which has the height and width of an ID-1 type defined in ISO/IEC 7810 containing a single turn coil concentric with the card outline (see Figure 1).

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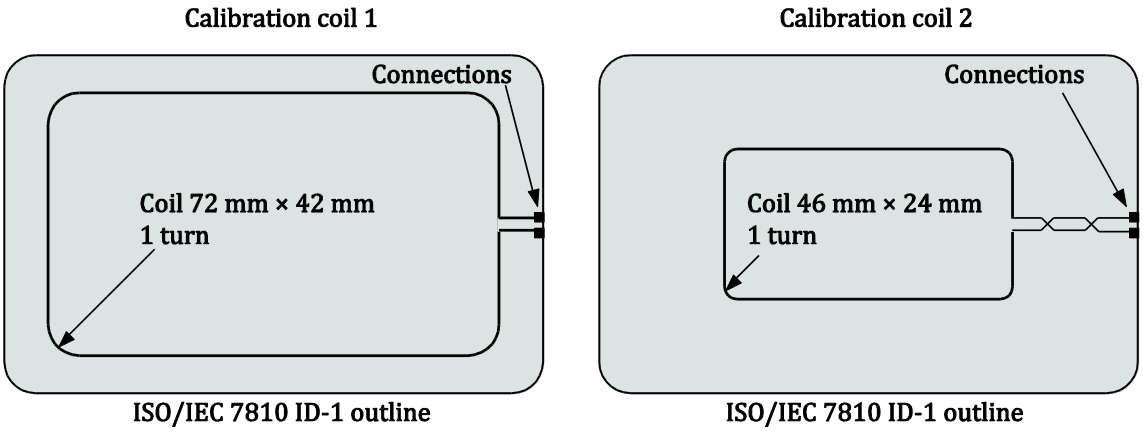

Figure 1 — Calibration coils 1 and 2

5.2.2 Thickness and material of the calibration coil card

The thickness of the calibration coil card shall be less than that of an ID-1 card. It shall be constructed of a suitable insulating material.

5.2.3 Coil characteristics

The coil on the calibration coil card shall have one turn. Relative dimensional tolerance shall be ±2 %.

The outer size of the calibration coil 1 shall be 72 mm × 42 mm with corner radius 5 mm.

NOTE 1 The area over which the field is integrated is approximately 3 000 mm^2.

NOTE 2 At 13,56 MHz the approximate inductance is 250 nH and the approximate resistance is 0,4 Ω.

The open circuit calibration factor for the calibration coil 1 is 0,318 V (rms) per A/m (rms) [Equivalent to 900 mV (peak-to-peak) per A/m (rms)].

The outer size of the calibration coil 2 shall be 46 mm × 24 mm with corner radius 2 mm.

NOTE 3 The area over which the field is integrated is approximately 1 100 mm^2.

NOTE 4 At 13,56 MHz the approximate inductance is 140 nH and the approximate resistance is 0,3 Ω.

The open circuit calibration factor for the calibration coil 2 is 0,118 V (rms) per A/m (rms) [Equivalent to 333 mV (peak-to-peak) per A/m (rms)].

The coil shall be made as a printed coil on printed circuit board (PCB) plated with 35 µm copper. Track width shall be 500 µm with a relative tolerance of ±20 %. The size of the connection pads shall be 1,5 mm × 1,5 mm.

A high impedance oscilloscope probe with an input admittance equivalent to a parallel capacitance $C_p < 14$ pF and a parallel resistance $R_p > 9$ kΩ at 13,56 MHz shall be used to measure the (open circuit) voltage induced in the coil.

The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.

5.3 Test PCD assembly

Two Test PCD assemblies are defined:

— Test PCD assembly 1 for PICCs of "Class 1", "Class 2" and "Class 3" and for PICCs which do not claim compliance with a class;

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— Test PCD assembly 2 for PICCs of "Class 4", "Class 5" and "Class 6".

Each Test PCD assembly shall consist of a circular Test PCD antenna and two parallel sense coils, sense coil a and sense coil b, as shown in principle by Figure 2. The sense coils shall be connected such that the signal from one coil is in opposite phase to the other. The 10 Ω potentiometer P1 serves to fine adjust the balance point when the sense coils are not loaded by a PICC or any magnetically coupled circuit. The capacitive load of the probe including its parasitic capacitance shall be less than 14 pF.

The capacitance of the connections and of the oscilloscope probe should be kept to a minimum for reproducibility.

In order to avoid any unintended misalignment in case of an unsymmetrical set-up the tuning range of the potentiometer P1 is only 10 Ω. If the set-up cannot be compensated by the 10 Ω potentiometer P1, the overall symmetry of the set-up should be checked.

The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.

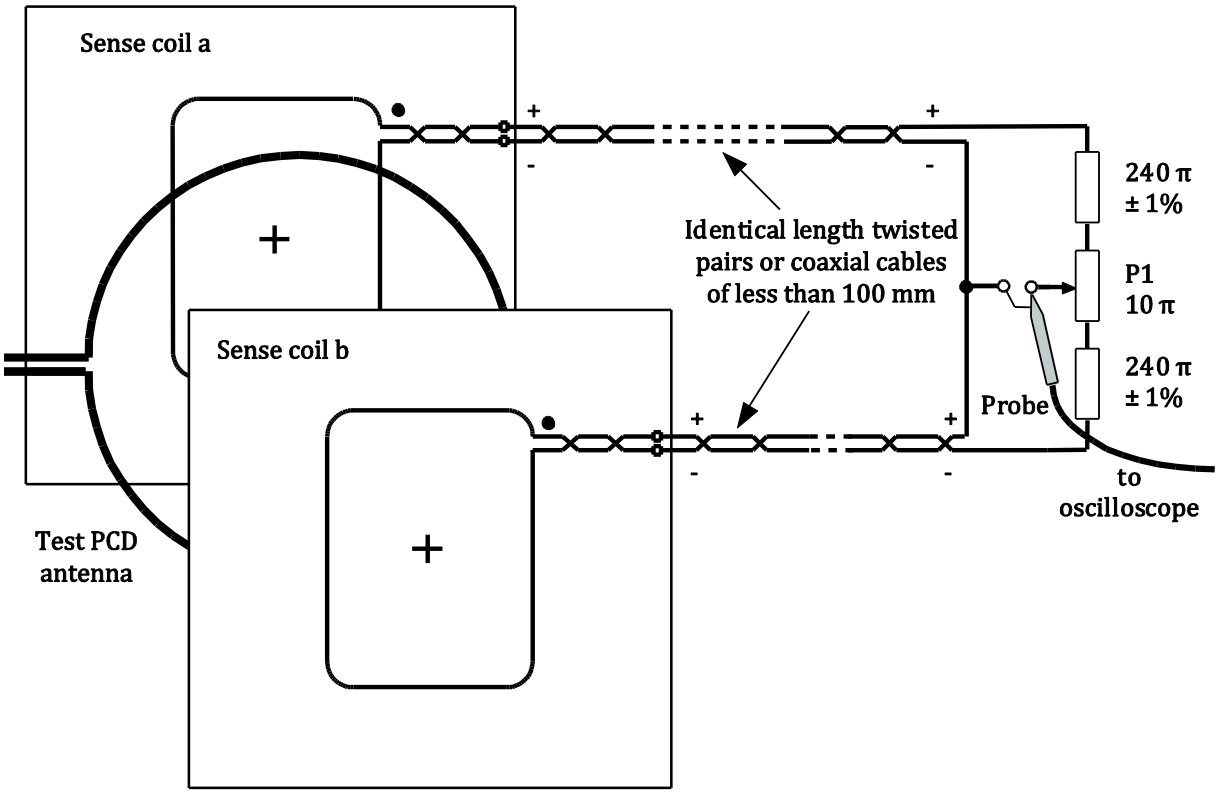

Figure 2 — Test set-up (principle)

5.3.1 Test PCD antenna

In Test PCD assembly 1 the Test PCD antenna 1 shall have a diameter of 150 mm.

In Test PCD assembly 2 the Test PCD antenna 2 shall have a diameter of 100 mm.

Each Test PCD antenna construction shall conform to the corresponding drawings in Annex A.

The matching of each Test PCD antenna should be accomplished by using an impedance analyzer or a network analyzer or an LCR meter. If either an impedance analyzer or a network analyzer or an LCR meter is not available, then the matching may be accomplished with the procedure given in Annex B.

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5.3.2 Sense coils

In Test PCD assembly 1 the size of the sense coils 1 shall be 100 mm × 70 mm with corner radius 10 mm.

In Test PCD assembly 2 the size of the sense coils 2 shall be 60 mm × 47 mm with corner radius 10 mm.

Each sense coil construction shall conform to the corresponding drawings in Annex C.

5.3.3 Assembly of Test PCD

The sense coils 1 and Test PCD antenna 1 shall be assembled parallel and with the sense and antenna coils coaxial and such that the distance between the active conductors is 37,5 mm as shown in Figure 3, Test PCD assembly 1.

The sense coils 2 and Test PCD antenna 2 shall be assembled parallel and with the sense and antenna coils coaxial and such that the distance between the active conductors is 23 mm as shown in Figure 3, Test PCD assembly 2.

The dimensional tolerance shall be better than ± 0,5 mm. The distance between the coil in the DUT and the calibration coil shall be equal with respect to the coil of the Test PCD antenna.

NOTE These distances are chosen to offer a strong and homogenous magnetic field in the DUT position.

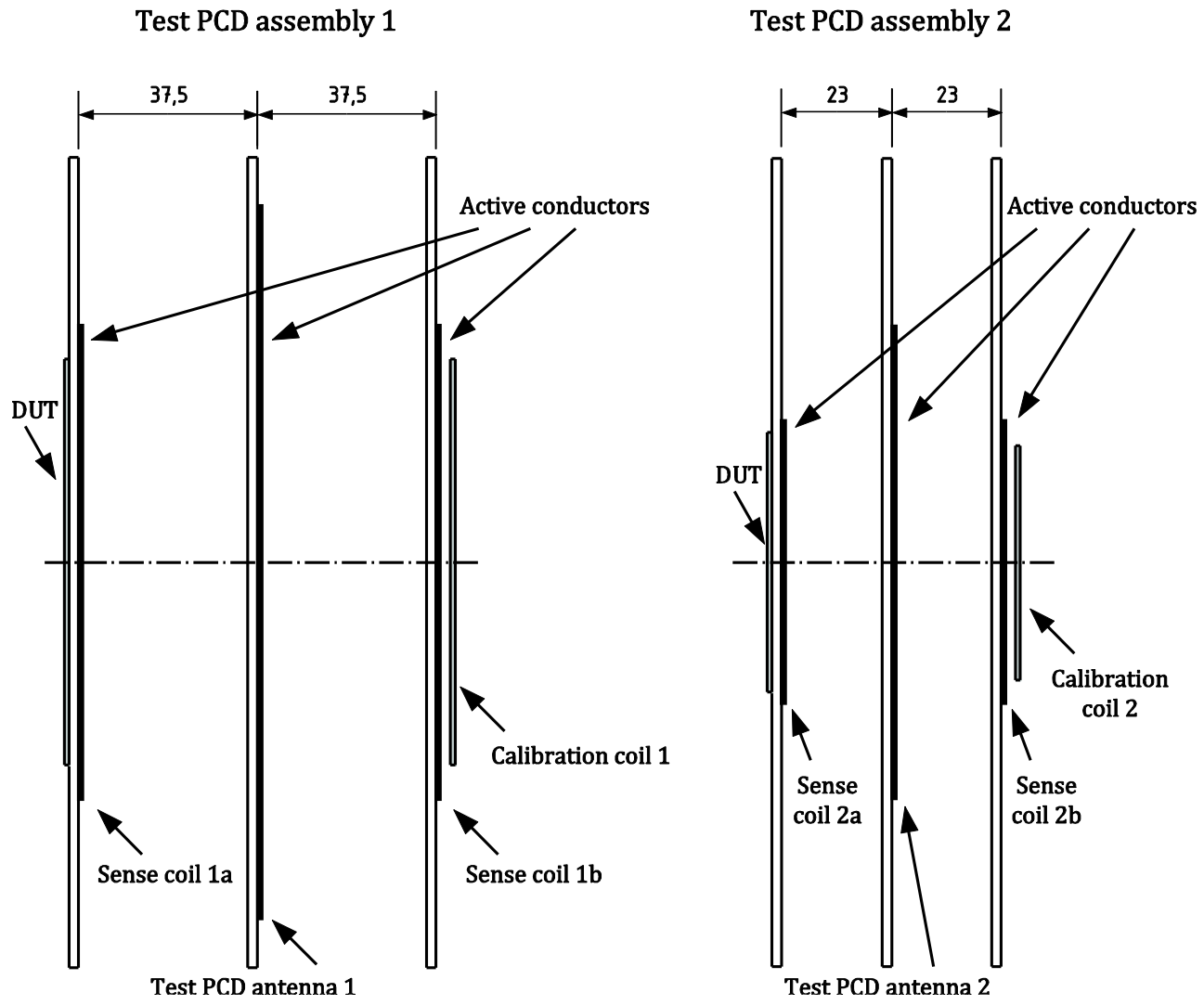

Figure 3 — Test PCD assembly 1 and Test PCD assembly 2

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5.4 Reference PICC

A Reference PICC is defined to test the ability of a PCD to

— generate a field strength of at least H_{min} and not exceeding H_{max},

— transfer power to a PICC,

— transmit a modulated signal to a PICC,

— receive a load modulation signal from the PICC,

in its operating volume.

5.4.1 Dimensions of the Reference PICC

The Reference PICC shall consist of an area containing the coils which has the height and width defined in ISO/IEC 7810 for ID-1 type. An area external to this, containing the circuitry which emulates the required PICC functions, shall be appended in such a way as to allow insertion into the test set-ups and so as to cause no interference to the tests. The dimensions shall be as shown in Figure 4.

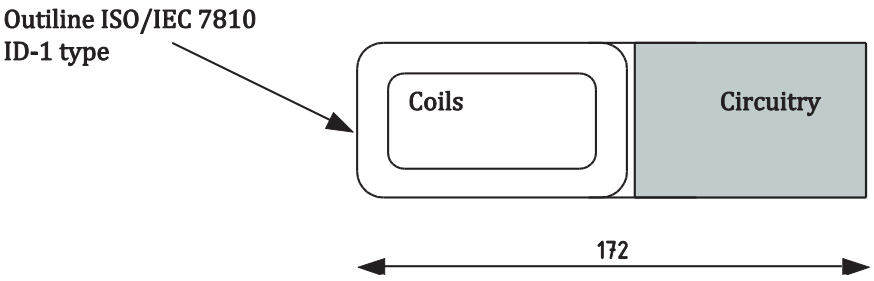

Figure 4 — Reference PICC dimensions

5.4.2 Reference PICC construction

The Reference PICCs coils layouts are defined in Annex D. If connectors are used between the coils and the circuitry, those connectors shall have minimal, if any, effect on the RF measurements.

The Reference PICC shall have a circuit diagram as defined in Figure 5 and component values as defined in Table 2.

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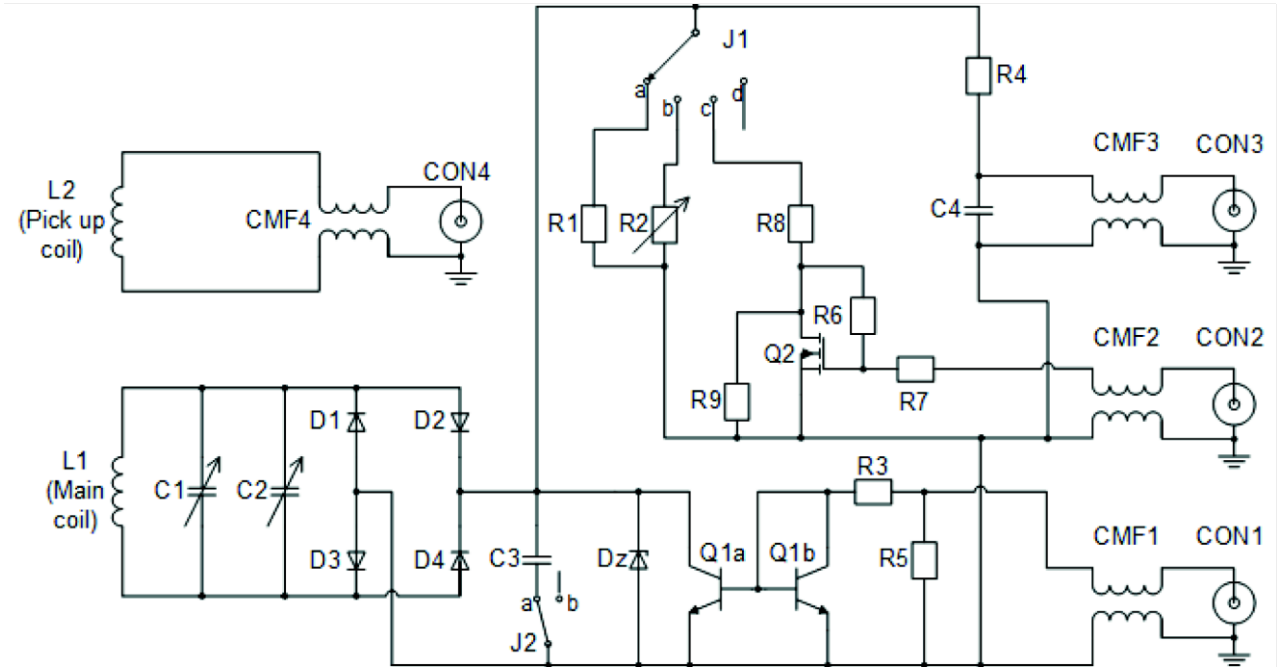

Figure 5 — Reference PICC circuit diagram

NOTE Position 'd' of jumper J1 is RFU.

Table 2 — Reference PICC components list

Component	Value	Component	Value
L1	See Annex D	C1	7 pF – 50 pF [b]
L2	See Annex D	C2	3 pF – 10 pF [b]
R1	1,8 kΩ	C3	27 pF
R2	0 kΩ – 2 kΩ [a]	C4	1 nF
R3	220 Ω	D1, D2, D3, D4	BAR43S or equivalent [c]
R4	51 kΩ	Dz	BZX84, 15 V or equivalent [c]
R5	51 Ω	Q1a, Q1b	BCV61A or equivalent
R6	500 kΩ	Q2	BSS83 or equivalent
R7	110 kΩ	CMF1, CMF2, CMF3, CMF4	ACM3225 -102-2P or equivalent
R8	51 Ω	CON1, CON2, CON3, CON4	RF connector
R9	1,5 kΩ		

[a] A multi-turn potentiometer (turns ≥10) should be used.

[b] Q - factor shall be higher than 100 at 13,56 MHz.

[c] Care should be taken on parameters Cj (Junction capacitance), Cp (Package capacitance), Ls (Series inductance) and Rs (Series resistance) of equivalent diodes. Note that these values may not be available in the datasheet.

At CON1 the load modulation signal shall be applied. The load modulation can be determined in Test PCD assembly. When not used, the load modulation signal generator shall be disconnected or set to 0 V.

With the voltage at CON2 the Reference PICC load can be adjusted until the required DC voltage shows at CON3.

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The Reference PICC DC voltage shall be measured at CON3 using a high impedance voltmeter and the connection wires should be twisted or coaxial.

The PCD waveform parameters are picked up at CON4 using a high impedance oscilloscope probe. The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.

Position 'a' of J2 shall be used for testing bit rates of $fc/128$, $fc/64$, $fc/32$ and $fc/16$.

Position 'b' of J2 shall be used for testing bit rates of $fc/8$, $fc/4$ and $fc/2$.

5.4.3 Reference PICC resonance frequency tuning

The Reference PICC resonance frequency shall be calibrated with the following procedure.

a) Set jumper J1 to position 'a'.

b) Connect the calibration coil directly to a signal generator and the Reference PICC connector CON3 to a high impedance voltmeter. Connect all the other connectors to the same equipment as used for the tests.

c) Locate the Reference PICC at a distance d = 10 mm above the calibration coil with the axes of the two coils (calibration coil and Reference PICC main coil) being congruent (see Figure 6).

d) Drive the calibration coil with a sine wave set to the desired resonance frequency.

e) Adjust the Reference PICC capacitors C1 and C2 to get maximum DC voltage at CON3.

f) Adjust the signal generator drive level to obtain a DC voltage at CON3 of V_{load} as defined in Table 3.

g) Repeat steps e) and f) until the maximum voltage after step e) is V_{load}.

h) Calibrate the Test PCD assembly to produce the H_{min} operating condition on the calibration coil.

i) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'b' and adjust R2 to obtain a DC voltage of V_{load} measured at connector CON3. The operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.

j) Repeat steps b) to g) with the obtained value of R2.

NOTE Instead of a signal generator, a vector network analyzer may be used if sufficient power is provided to produce V_{load} at CON3 while reaching the maximum resistive part of the measured complex impedance of the calibration coil.

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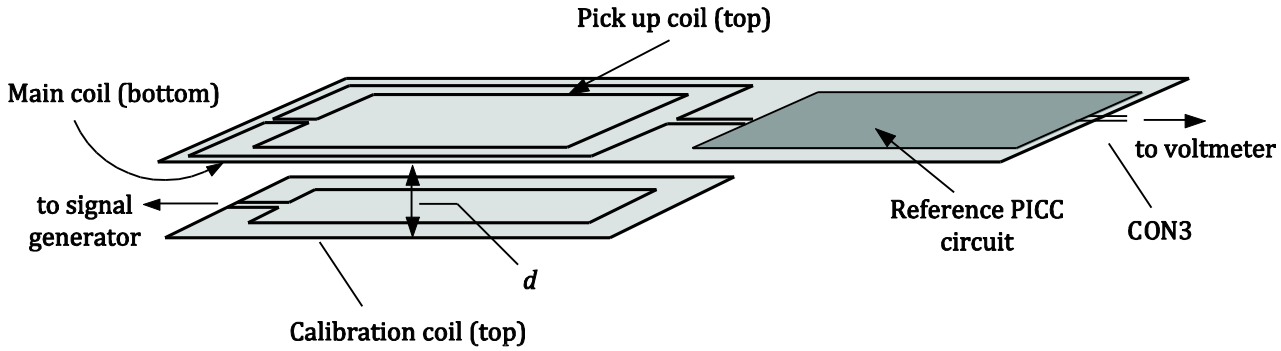

Figure 6 — Reference PICC frequency tuning set-up (principle)

5.5 EMD test setup

5.5.1 General description

The EMD test setup contains the following:

— a signal generator with low phase noise, which is used to synthesize both an EMD test pattern and PCD test commands sent to the PICC under test;

— the Test PCD assembly;

— a signal amplitude analyzing device:

  — either a signal acquiring device (e.g. oscilloscope) and appropriate computation software;

  — or a spectrum analyzer (see additional constraints in 5.5.2).

The signal amplitude analyzing device shall be able to carry out power versus time measurements with fixed frequency, fixed bandwidth, high dynamic range, low measurement uncertainty and high time resolution.

NOTE The PICC EMD tests may be performed using the RF output signal of a commercial PCD. The PCD EMD test may use a PICC emulator to generate the EMD test pattern.

5.5.2 Computation of power versus time

The beginning of the captured signal shall be windowed by a Bartlett window of exactly two subcarrier cycles. Fourier transformation of these windowed samples produces one power value. By shifting the Bartlett window by steps of $1/fc$ from the beginning to the end of the captured signal, the desired power versus time result is finally computed.

NOTE The resulting 3 dB bandwidth of the above described window is 531 kHz and its noise equivalent bandwidth amounts to 843 kHz.

The computation of the power versus time shall be performed at $fc + fs$ and $fc - fs$, using a scaling such that a pure sinusoidal signal results in its peak magnitude. An example of computation is provided in Annex J.

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In case of using a spectrum analyzer, the analyzer shall have at least an equivalent analysis bandwidth. It shall pass the noise floor precondition test, as defined in 5.5.3, and there shall be some additional margin of $10/fc$ on $t_{E,\,PICC}$ requirement and no spikes above the EMD limit.

5.5.3 Noise floor precondition test

5.5.3.1 Purpose

In order to ensure a high dynamic range and sufficient sensitivity, a noise floor measurement shall be performed and passed successfully by the EMD test setup. The aim of this precondition test is to verify that the test apparatus used for EMD level measurement satisfies a minimum noise requirement.

The noise floor test is passed if the noise standard deviation is at least three times smaller than the EMD limit $V_{E,\,PICC}$, when measured as described in 5.5.3.2.

The noise standard deviation is determined by calculating the root-mean-square value of the results of the Fourier transformation, as described in 5.5.2.

NOTE This noise floor can be obtained either with a 14-bit digitizer at a sampling rate of 100 million samples per second or with an 8-bit digital oscilloscope at sampling rate of 1 000 million samples per second.

5.5.3.2 Procedure

Perform the following steps to assess the noise floor at least at H_{min} and H_{max}.

a) Tune the Reference PICC to 13,56 MHz.

b) Adjust the RF power delivered by the signal generator to the Test PCD antenna to the required field strength as measured by the calibration coil.

c) Place the Reference PICC into the DUT position on the Test PCD assembly, set jumper J1 to position 'b' and adjust R2 to obtain a voltage of V_{load} at CON3. Alternatively, jumper J1 may be set to position 'c' and the applied voltage on CON2 is adjusted to obtain a voltage of V_{load} at CON3. In both cases the operating field condition shall be verified by monitoring the voltage in the calibration coil and adjusted if necessary.

d) Record the signal of the sense coils for a time period of at least 250 µs.

e) Compute the noise standard deviations at $fc + fs$ and $fc - fs$ using suitable computer software, as e.g. the one given in Annex J. Check if these noise standard deviations are three times smaller than $V_{E,\,PICC}$.

5.5.3.3 Test report

The test report shall state the noise standard deviations at $fc + fs$ and $fc - fs$ and shall state whether the requirements have been fulfilled.

6 Test of ISO/IEC 14443-1 parameters

6.1 PCD tests

6.1.1 Alternating magnetic field

6.1.1.1 Purpose

This test determines that the PCD generates a field not higher than the average value specified in ISO/IEC 14443-1, in any possible PICC position.

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6.1.1.2 Procedure

a) Tune the Reference PICC 1 to 19 MHz as described in 5.4.3 steps a) to g).

b) Calibrate the Test PCD assembly 1 to produce the average field value specified in ISO/IEC 14443-1:2016, 4.4 on the calibration coil.

c) Place the Reference PICC 1 into the DUT position on the Test PCD assembly 1. Switch the jumper J1 to position 'b' and adjust R2 to obtain a DC voltage of 3 V measured at connector CON3. The operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.

   WARNING — R2 value should be between 55 and 65 Ω.

d) Position the Reference PICC 1 in any possible PICC position. The DC voltage at CON3 shall not exceed 3 V.

e) If exceeded, use the same conversion factor to measure the maximum and average DC voltage and convert in field strength to check the maximum and the average field values specified in ISO/IEC 14443-1:2016, 4.4 in 30 s period.

6.1.1.3 Test report

The test report shall give the DC voltage measured at CON3.

6.2 PICC tests

6.2.1 Alternating magnetic field

6.2.1.1 Purpose

The purpose of this test is to check the behavior of the PICC in relation to alternating magnetic field exposure at 13,56 MHz.

6.2.1.2 Apparatus

The Test PCD assembly shall be used to produce the alternating magnetic field.

6.2.1.3 Procedure

The procedure is as follows.

a) In accordance with the PICC class, adjust the RF power delivered by the signal generator to the Test PCD antenna to a field strength of the average level specified in ISO/IEC 14443-1:2016, 4.4 as measured by the calibration coil.

b) Place the PICC under test in the DUT position and readjust immediately the RF drive into the Test PCD antenna to the required field strength if necessary.

c) After 5 min, remove the PICC from the DUT position for at least 5 s.

d) In accordance with the PICC class, adjust the RF power delivered by the signal generator to the Test PCD antenna to a field strength of the maximum level specified in ISO/IEC 14443-1:2016, 4.4 as measured by the calibration coil.

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e) Place the PICC under test in the DUT position and readjust immediately the RF drive into the Test PCD antenna to the required field strength if necessary.

f) Apply for 5 min an ASK 100 % modulation to this field with the following duty cycle:

1) 5 s at 0 A/m (rms);

2) 25 s at the maximum level specified in ISO/IEC 14443-1:2016, 4.4, in accordance with the PICC class.

g) Check that the PICC operates as intended.

6.2.1.4 Test report

The test report shall state whether or not the PICC operates as intended.

6.2.2 Static electricity test

6.2.2.1 Purpose

The purpose of this test is to check the behavior of the card IC in relation to electrostatic discharge (ESD) exposure in the test sample. The PICC under test is exposed to a simulated electrostatic discharge (ESD, human body model) and its basic operation checked following the exposure (see Figure 7).

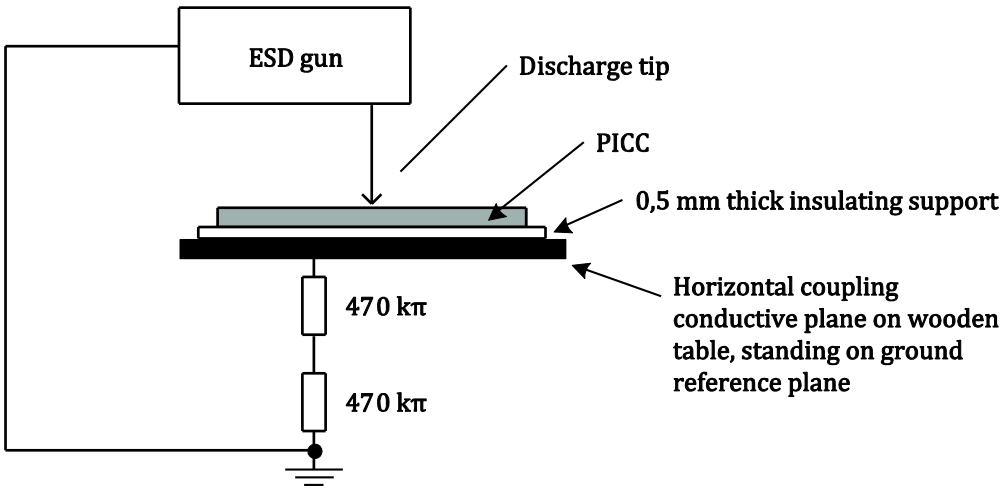

Figure 7 — ESD test circuit

6.2.2.2 Apparatus

Refer to IEC 61000-4-2:2008.

a) Main specifications of the ESD generator:

— energy storage capacitance: 150 pF ± 10 %;

— discharge resistance: 330 Ω ± 10 %;

— charging resistance: between 50 MΩ and 100 MΩ;

— rise time: 0,7 ns to 1 ns.

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b) Selected specifications from the optional items:

— type of equipment: table top equipment;

— discharge method: direct application of air discharge to the equipment under test;

— discharge electrodes of the ESD generator: round tip probe of 8 mm diameter.

6.2.2.3 Procedure

Connect the ground pin of the apparatus to the conductive plate upon which the PICC is placed.

Apply the discharge successively in normal polarity to each of the 20 test zones as defined in Figure 8. Then repeat the same procedure with reversed polarity. Allow a cool-down period between successive pulses of at least 10 s.

WARNING — If the PICC includes contacts, the contacts should face up and the zone which includes contacts should not be exposed to this discharge.

Check that the PICC operates as intended at the end of the test.

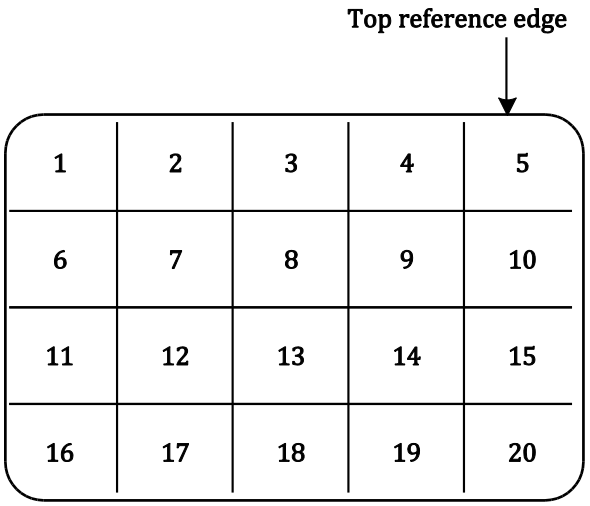

Figure 8 — Test zones on PICC for ESD test

6.2.2.4 Test report

The test report shall state whether or not the PICC operates as intended.

6.3 PXD tests

PCD and PICC tests shall be applied as follows:

— when the PXD is in PCD Mode, tests defined in 6.1 shall be applied;

— when the PXD is in PICC Mode, tests defined in 6.2 shall be applied.

In automatic mode alternation, the PXD may be forced into the required mode.

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7 Test of ISO/IEC 14443-2 parameters

7.1 PCD tests

All the PCD tests described below will be done in the operating volumes as defined by the PCD manufacturer for each supported class.

All PCD tests of ISO/IEC 14443-2 parameters shall be performed using Reference PICCs 1, 2 and 3 and optionally other Reference PICCs corresponding to the optional classes supported by the PCD, with the relevant parameters and Test PCD assembly as defined in Table 3.

〈A3〉 Table 3 — Class parameters

Class	Reference PICC	V_{load}	$R2_{min}$	$R2_{max}$	Test PCD assembly
1	1	4,5 V	647 Ω	791 Ω	Test PCD assembly 1
2	2	4,5 V	1 030 Ω	1 260 Ω	Test PCD assembly 1
3	3	4,5 V	1 080 Ω	1 320 Ω	Test PCD assembly 1
4	4	4,5 V	990 Ω	1 210 Ω	Test PCD assembly 2
5	5	4,5 V	960 Ω	1 170 Ω	Test PCD assembly 2
6	6	4,5 V	700 Ω	900 Ω	Test PCD assembly 2

The PCD should be tested with a V_{load} of 6 V for Reference PICC 1 to ensure interoperability with PICCs compliant with the V_{load} requirement of ISO/IEC 10373-6:2016. 〈A3〉

7.1.1 PCD field strength

7.1.1.1 Purpose

This test measures the field strength produced by a PCD in its operating volume. The maximum and minimum field strength values to be used with each Reference PICC are given in ISO/IEC 14443-2:2016, Table 1.

NOTE The test takes account of PICC loading of the PCD.

7.1.1.2 Procedure

7.1.1.2.1 Procedure for H_{max} test

a) Tune the Reference PICC to 19 MHz as described in 5.4.3 steps a) to g).

b) Calibrate the Test PCD assembly to produce the H_{max} operating condition on the calibration coil.

c) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'b' and adjust R2 to obtain a DC voltage of 3 V measured at connector CON3. Alternatively, jumper J1 may be set to position 'c' and the applied voltage on CON2 is adjusted to obtain a DC voltage of 3 V at connector CON3. In both cases, the operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.

   WARNING — R2 value should be between 75 and 85 Ω. Check this range at least once before using the alternative method.

d) Position the Reference PICC within the defined operating volume of the PCD under test. The DC voltage at CON3 shall not exceed 3 V.

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7.1.1.2.2 Procedure for H_{min} test

a) Tune the Reference PICC to 13,56 MHz as described in 5.4.3.

b) Place the Reference PICC into the DUT position on the Test PCD assembly producing the H_{min} operating condition on the calibration coil. Check that the jumper J1 is set to position 'b' and that a DC voltage of V_{load} as defined in Table 3 is measured at connector CON3. Alternatively, the jumper J1 may be set to position 'c' and the voltage on CON2 is adjusted to obtain a DC voltage of V_{load} as defined in Table 3 at connector CON3. In both cases, the operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.

   WARNING — R2 value should be between $R2_{min}$ and $R2_{max}$ as defined in Table 3. Check this range at least once before using the alternative method.

c) Position the Reference PICC within the defined operating volume of the PCD under test. The DC voltage at CON3 shall exceed V_{load} as defined in Table 3.

A3 d) For Reference PICC 1 repeat:

   1) step b) with a DC voltage V_{load} of 6 V measured at connector CON3 instead of V_{load} as defined in Table 3, and

   2) step c), where the DC voltage at CON3 shall exceed 5,3 V [corresponding to H_{min} – 0,2 A/m(rms)], instead of V_{load} as defined in Table 3. A3

7.1.1.3 Test report

A3 The test report shall confirm the operating volume in which the DC voltage measured at CON3 for R2 or variable load resistor adjusted to H_{min} and H_{max} field strength fulfils the requirements defined in step d) of 7.1.1.2.1 and in step c) of 7.1.1.2.2. A3

7.1.2 Void

PCD field strength supporting operation with "Class 1" PICCs, which was defined in ISO/IEC 10373-6:2011, is deleted.

7.1.3 Void

Power transfer PCD to PICC, which was defined in ISO/IEC 10373-6:2011, is deleted.

7.1.4 Modulation index and waveform

7.1.4.1 Purpose

This test is used to determine the index of modulation of the PCD field as well as the rise and fall times and the overshoot values as defined in ISO/IEC 14443-2 for all supported PCD to PICC bit rates.

7.1.4.2 Procedure

a) Position the calibration coil at an arbitrary position in the defined operating volume and display the induced coil voltage on a suitable oscilloscope. Determine the modulation index and waveform characteristics using the analysis tool defined in Annex E.

b) Tune the Reference PICC to 16,5 MHz as described in 5.4.3 steps a) to g) and switch the jumper J1 to position 'c'.

c) Place the Reference PICC at a particular position in the PCD operating volume.

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d) Apply and adjust a DC voltage at CON2 to obtain a DC voltage at connector CON3 of V_{load} as defined in Table 3. If a DC voltage of V_{load} cannot be reached at the selected position, the maximum achievable voltage should be used for the test.

e) If the unmodulated voltage on CON4, measured with a suitable oscilloscope (requirements see 5.1.1) is below 1 V (peak-to-peak), use an alternative pick up coil to determine the waveform characteristic.

   This alternative pick up coil should have a "figure of 8" shape with 15 mm radius positioned farthest away from the Reference PICC to minimize coupling and as close as possible to the PCD antenna to maximize induced voltage.

f) Determine the modulation index and waveform characteristic from the voltage at CON4 or at the alternative pick up coil using the analysis tool defined in Annex E.

g) Repeat steps c) to f) for various positions within the operating volume and all supported PCD to PICC bit rates.

NOTE 1 The selected position of the calibration coil within the operating volume is not expected to affect the results.

NOTE 2 The Reference PICC load does not represent the worst case loading effect of a PICC. Higher loading effects may be achieved with resonance frequencies closer to carrier frequency (e.g. 15 MHz or 13,56 MHz).

7.1.4.3 Test report

The test report shall give the measured modulation index of the PCD field, the rise and fall times and overshoot values, within the defined operating volume in unloaded and loaded conditions.

7.1.5 Load modulation reception

7.1.5.1 Purpose

This test is used to verify that a PCD correctly detects the load modulation of a PICC which conforms to ISO/IEC 14443-2 for PICC to PCD bit rates of $fc/128$, $fc/8$, $fc/4$ and $fc/2$, if supported.

7.1.5.2 Procedure

The Reference PICC and its calibration procedure allow the sensitivity of a PCD to load modulation to be assessed. The Reference PICC does not emulate the loading effect of all types of PICC.

a) Tune the Reference PICC to 13,56 MHz as described in 5.4.3 and switch the jumper J1 to position 'c'.

b) Place the Reference PICC at a particular position in the PCD operating volume.

c) Apply and adjust a DC voltage at CON2 to obtain a DC voltage at connector CON3 of V_{load} as defined in Table 3.

d) Increase the modulation signal amplitude at CON1 to produce responses until the PCD detects at least 10 of them consecutively.

e) Place the Reference PICC in the DUT position on the Test PCD assembly.

f) Adjust the Test PCD assembly to produce a field strength H which gives the same voltage at CON3 and note the corresponding field strength by reading the calibration coil voltage.

g) Measure the Reference PICC load modulation amplitude V_{LMA} as described in 7.2.1 and compare it with the standard limit $V_{LMA,\,PCD}$ associated with the noted field strength. This measured V_{LMA} level defines the PCD sensitivity criterion in order to compare with the standard limit $V_{LMA,\,PCD}$ to perform these test measurements.

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h) Repeat steps b) to g) for various positions within the operating volume for PICC to PCD bit rates of $fc/128$, $fc/8$, $fc/4$ and $fc/2$, if supported.

i) Repeat steps a) to h) with Reference PICC resonance frequency 15 MHz.

Any position in which the PCD sensitivity is above the standard limit $V_{LMA, PCD}$ shall be considered out of the operating volume.

The test coverage may be expanded by using additional resonance frequencies below 13,56 MHz such as 12 MHz and 10 MHz.

The PCD sensitivity should be below the standard limit $V_{LMA, PCD}$ to ensure good reception of the PICC load modulation.

NOTE This test does not check that the PCD reception is independent of the phase of the PICC load modulation. Consequently, it cannot guarantee the correct reception of any PICC compliant with ISO/IEC 14443-2.

7.1.5.3 Test report

The test report shall give the PCD load modulation sensitivity for the tested positions.

7.1.6 PCD EMD immunity test

7.1.6.1 Purpose

The purpose of this test is to determine whether the PCD is insensitive to any load modulation amplitude below $V_{E, PCD}$.

7.1.6.2 Procedure

a) Tune the Reference PICC to 13,56 MHz as described in 5.4.3 and switch the jumper J1 to position 'c'.

b) Place the Reference PICC at a designated position in the PCD operating volume.

c) Apply and adjust a DC voltage at CON2 to obtain a DC voltage at connector CON3 of V_{load} as defined in Table 3.

d) Send the test pattern as shown in Figure 9. The test pattern is a valid standard frame including one single byte (01011101)b. The initial load modulation amplitude V_{EMD} of the test pattern shall be sufficiently low so that the PCD detects the PICC answer sent in step e).

e) Immediately after this test pattern, applying no gap, send the appropriate PICC answer to the PCD command with a load modulation amplitude V_{LMA}, measured as defined in 7.2.1, of a level higher, e.g. twice, than the minimum value for the applied field strength H.

f) Increase V_{EMD} by adjusting the voltage at CON1 until the PCD does no longer detect the answer correctly. This may be determined by monitoring the next PCD command following the PICC answer; see Figure 9.

g) Place the Reference PICC into the DUT position on the Test PCD assembly.

h) Adjust the Test PCD assembly to produce a field strength H which gives the same voltage at CON3 and note the corresponding field strength by reading the calibration coil voltage.

i) Derive the current value of V_{EMD} on the Reference PICC by applying the power versus time measurement as described in 5.5.2.

j) Compare this measured V_{EMD} value with $V_{E, PCD}$.

Repeat steps b) to j) for other designated positions within the operating volume.

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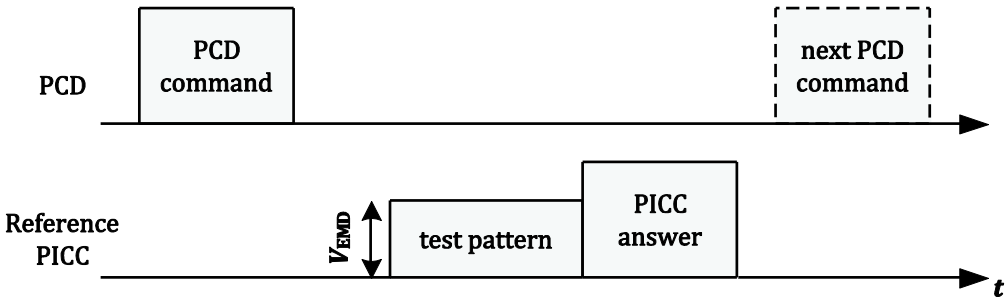

Figure 9 — PCD immunity test (common for Type A and Type B)

7.1.6.3 Test report

The test report shall state whether the PCD was insensitive to any load modulation amplitude below $V_{E,\,PCD}$.

7.1.7 PCD EMD recovery test

7.1.7.1 Purpose

The purpose of this test is to determine whether the PCD is disturbed by a test pattern sent $t_{E,\,PCD}$ before the PICC answer.

7.1.7.2 Procedure

a) Tune the Reference PICC to 13,56 MHz as described in 5.4.3.

b) Calibrate the Test PCD assembly to produce the H_{min} operating condition on the calibration coil.

c) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'c' and adjust the DC voltage at CON2 to obtain a DC voltage at connector CON3 of V_{load} as defined in Table 3. The operating field condition shall be verified by monitoring the voltage on the calibration coil and the voltage adjusted if necessary.

d) Find the appropriate driving voltage at CON1 to produce a load modulation amplitude V_{LMA}, measured as defined in 7.2.1, higher than the limit for H_{min}, defined in ISO/IEC 14443-2.

e) Place the Reference PICC at a position within the operating volume of the PCD where V_{load} is obtained at CON3.

f) Send in sequence, as illustrated in Figure 10 using the $t_{E,\,PCD}$ associated with minimum FDT/TR0,

NOTE 1 The low EMD time $t_{E,\,PCD}$ is a function of FDT/TR0 as defined in ISO/IEC 14443-3:2016, 8.2.

— a test pattern, which starts sending the two data bits b1 = (0)b followed by b2 = (1)b in a valid way to the PCD, but interrupts immediately after the second bit sent, as illustrated in Figure 11 for Type A and Figure 12 for Type B,

NOTE 2 Depending on the FDT/TR0, the test pattern may start before the end of the PCD command.

— a period with no load modulation for a duration of $t_{E,\,PCD}$,

— the appropriate answer to the PCD command.

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g) Check if the PCD behaves in the same way as if there was no test pattern. This may be determined by monitoring the next PCD command following the PICC answer; see Figure 10.

h) Repeat steps f) and g) 10 times.

i) Repeat steps f) to h) replacing minimum FDT/TR0 with maximum FDT/TR0.

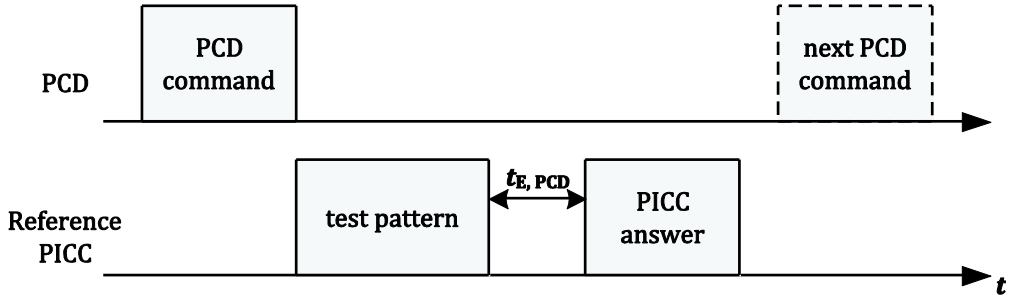

Figure 10 — EMD recovery test sequence (common for Type A and Type B)

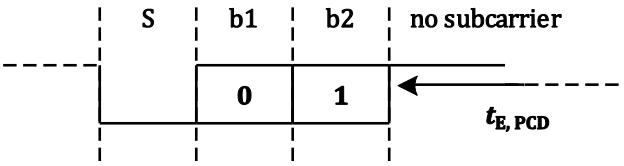

Figure 11 — Test pattern for the EMD recovery test (Type A)

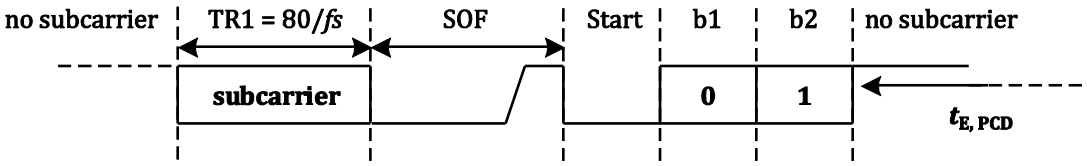

Figure 12 — Test pattern for the EMD recovery test (Type B)

7.1.7.3 Test report

The test report shall report whether the PCD was not disturbed by the test pattern sent $t_{E, PCD}$ before the PICC answer (or was able to recover from the test pattern).

7.2 PICC tests

7.2.1 PICC transmission

7.2.1.1 Purpose

The purpose of this test is to determine the load modulation amplitude V_{LMA} of the PICC within the operating field range [H_{min}, H_{max}] as specified in ISO/IEC 14443-2 for PICC to PCD bit rates of $fc/128$, $fc/8$, $fc/4$ and $fc/2$, if supported. Also the functionality of the PICC for Type A and Type B within their corresponding modulation ranges as defined in ISO/IEC 14443-2 shall be determined.

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7.2.1.2 Procedure

Step 1:

The load modulation test circuit of Figure 2 and the Test PCD assembly of Figure 3 defined for the PICC class (see ISO/IEC 14443-2:2016, 8.2.2) are used. If the PICC does not claim to meet the requirements of one particular class as specified in ISO/IEC 14443-1, then select the Test PCD assembly 1.

Adjust the RF power delivered by the signal generator to the Test PCD antenna to the required field strength as measured by the calibration coil. Connect the output of the load modulation test circuit of Figure 2 to a digital sampling oscilloscope. The 10 Ω potentiometer P1 shall be trimmed to minimize the residual carrier. This signal shall be at least 40 dB lower than the signal obtained by shorting one sense coil.

WARNING — The PICC load modulation amplitude test should be done by increasing the field strength from 0 A/m (rms), thus checking correct PICC operation starting from H_{min}.

Step 2:

The PICC under test shall be placed in the DUT position, concentric with sense coil a**.** The RF drive into the Test PCD antenna shall be re-adjusted to the required field strength.

A REQA or a REQB command sequence as defined in ISO/IEC 14443-3 shall be sent by the Test PCD to obtain a signal or load modulation response from the PICC when testing PICC transmission at a bit rate of *fc*/128. An S(PARAMETERS) sequence as defined in ISO/IEC 14443-4 and an I-block shall be sent by the Test PCD to obtain a signal or load modulation response from the PICC when testing optional PICC transmission bit rates of *fc*/8, *fc*/4 and *fc*/2.

NOTE 1 No load modulation test is required for bit rates of *fc*/64, *fc*/32 and *fc*/16 because these bit rates use the same subcarrier frequency of *fc*/128.

Display a segment of at least six cycles of the waveform of the subcarrier load modulation on the digital sampling oscilloscope and store the sampled data in a file for analysis by a software program (see Annex F).

Care should be taken to apply a proper synchronization method for low amplitude load modulation.

Fourier transform with a Bartlett window exactly six subcarrier cycles of the sampled modulation waveform using suitable computer software (as the one given in Annex F). Use a discrete Fourier transformation with a scaling such that a pure sinusoidal signal results in its peak magnitude. In order to minimize transient effects, avoid analyzing a subcarrier cycle immediately following a non-modulating period or a phase shift of the subcarrier. The discrete Fourier transformation shall be done at the sidebands frequencies generated by the PICC under test, i.e. *fc* + *fs* and *fc* − *fs*.

The resulting peak amplitudes of the upper and lower sidebands at *fc* + *fs* and *fc* − *fs* shall be above the value defined in ISO/IEC 14443-2:2016, 8.2.2.

NOTE 2 For Type B PICC load modulation test, the oscilloscope FFT (Fast Fourier Transform) option may also be used on a large number of subcarrier cycles with neither transient effect nor phase shift (i.e. on a stable part of synchronization time TR1 as defined in ISO/IEC 14443-2:2016, 9.2.5 or on a stable part of SOF as defined in ISO/IEC 14443-3:2016, 7.1.4).

7.2.1.3 Test report

The test report shall give the measured peak amplitudes of the upper and lower sidebands at *fc* + *fs* and *fc* − *fs* and the applied fields and modulations.

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7.2.2 PICC EMD level and low EMD time test

7.2.2.1 Purpose

The purpose of this test is to determine that the PICC does not generate an electromagnetic disturbance amplitude V_{EMD} higher than $V_{E,\,PICC}$ during $t_{E,\,PICC}$ with the exceptions defined in ISO/IEC 14443-2.

NOTE 1 The low EMD time $t_{E,\,PICC}$ is a function of FDT/TR0 as defined in ISO/IEC 14443-3:2016, 8.2.

NOTE 2 The EMD limit $V_{E,\,PICC}$ is a function of the field strength.

7.2.2.2 Noise requirements

In order to ensure a high dynamic range and sufficient sensitivity to EMD, the noise floor precondition test defined in 5.5.3 shall be performed before this test.

7.2.2.3 Test commands

The PICC EMD test shall be performed for ISO/IEC 14443-3 commands. Depending on the PICC application, additional higher layer commands shall be included in the test plan.

7.2.2.4 Procedure

This test shall be done at least applying H_{min} and $H_{max.}$ Using the Test PCD assembly, perform the following steps.

a) Adjust the RF power delivered by the signal generator to the Test PCD antenna to the required field strength as measured by the calibration coil.

b) Place the PICC under test into the DUT position. The RF drive into the Test PCD antenna shall be readjusted to the required field strength if necessary.

c) Reset the PICC by switching the RF field off and on; then if necessary send a transition of sequence commands to put the PICC into the Test Initial State, (see G.3.3.2.1 for PICC Type A and G.4.4.1.1 for PICC Type B).

d) Send the command to be tested.

e) Record the sense coil's signal for a time period of at least 200 µs before the start of PICC subcarrier generation. Additionally, record at least 50 µs after the first detected subcarrier in order to determine precisely the position of the PICC answer.

f) Determine the value of $t_{E,\,PICC}$ from the acquired signal: if the PCD modulation is present on the trace then measure the time between the last rising edge of PCD modulation and the start of PICC subcarrier generation and calculate $t_{E,\,PICC}$ with the formula given in ISO/IEC 14443-3:2016, 8.2; if the PCD modulation is not present on the trace then $t_{E,\,PICC}$ equals its maximum value defined in ISO/IEC 14443-3:2016, 8.2.

g) Compute the signal power at the frequencies $fc + fs$ and $fc - fs$ as a function of time as defined in 5.5.2.

h) Using data obtained in step g), determine the time t_{START} corresponding to half the upper side band amplitude during the rising edge of PICC transmission. Check if the signal amplitude during the time period $[t_{START} - t_{E,\,PICC};\ t_{START} - 1/fs]$ complies with the requirements defined in ISO/IEC 14443-2.

i) Repeat step h) for the lower side band frequency.

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j) Repeat steps d) to i) for the next test command.

7.2.2.5 Test report

The test report shall state whether the PICC EMD level during $t_{E,\,PICC}$ complies with the requirements defined in ISO/IEC 14443-2.

Furthermore the test report shall give the measured maximum electromagnetic disturbance levels of the upper and lower sidebands at $fc + fs$ and $fc - fs$ during $t_{E,\,PICC}$. A graph showing EMD levels during $t_{E,\,PICC}$ should be incorporated in the report in case the test fails.

7.2.3 PICC reception

7.2.3.1 Purpose

The purpose of this test is to verify the ability of the PICC to receive the PCD commands.

7.2.3.2 PICC Type A for PCD to PICC bit rates of *fc*/128, *fc*/64, *fc*/32 and *fc*/16

7.2.3.2.1 Conditions for a PCD to PICC bit rate of *fc*/128

Three test conditions are defined with timings at the border of the Type A PICC modulation waveform timing parameters zone defined in ISO/IEC 14443-2:2016, Figure 4:

— condition 1: maximum $t_1 - t_2$ and maximum t_3, no overshoot;

— condition 2: minimum achievable (with Test PCD assembly) $t_1 - t_2$ and maximum associated t_3, maximum overshoot;

— condition 3: minimum achievable (with Test PCD assembly) t_3 and maximum associated $t_1 - t_2$, maximum overshoot.

The carrier amplitude at the end of t_2 should be less than 4 %.

These 3 test conditions shall be tested at least using H_{min} and H_{max} whereas parameter t_1 is the maximum specified value when condition 1 and condition 3 are used and is the minimum specified value when condition 2 is used.

7.2.3.2.2 Conditions for PCD to PICC bit rates of *fc*/64, *fc*/32 and *fc*/16

Three test conditions are defined with timings at the border of the Type A PICC modulation waveform timing parameters zone defined in ISO/IEC 14443-2:2016, Figures 7, 8 and 9:

— condition 1: maximum $t_1 - t_5$ and maximum t_6, no overshoot;

— condition 2: minimum achievable (with Test PCD assembly) $t_1 - t_5$ and maximum associated t_6, maximum overshoot;

— condition 3: minimum achievable (with Test PCD assembly) t_6 and maximum associated $t_1 - t_5$, maximum overshoot.

These 3 tests conditions shall be tested at least using H_{min} and H_{max} whereas:

— parameter a is the maximum specified value when condition 1 is used and is the minimum achievable value for the Test PCD assembly when condition 2 and condition 3 are used;

— parameter t_1 is the maximum specified value when condition 1 and condition 3 are used and is the minimum specified value when condition 2 is used.

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7.2.3.2.3 Procedure

Under the conditions defined in 7.2.3.2.1 the PICC shall answer to a REQA with ATQA.

For each optional PCD to PICC bit rate supported by the PICC, the PICC shall operate under the conditions defined in 7.2.3.2.2 after selection of that optional bit rate. This PICC shall respond correctly to an I-block transmitted at that optional bit rate.

7.2.3.3 PICC Type B for PCD to PICC bit rates of *fc*/128, *fc*/64, *fc*/32 and *fc*/16

7.2.3.3.1 Conditions

Three test conditions are defined with timings at the border of the Type B PICC modulation waveform timing parameters zone defined in ISO/IEC 14443-2:2016, 9.1.2:

— condition 1: maximum t_f and maximum t_r, no undershoot and overshoot;

— condition 2: minimum achievable (with Test PCD assembly) t_f and maximum associated t_r, maximum undershoot and overshoot;

— condition 3: minimum achievable (with Test PCD assembly) t_r and maximum associated t_f, maximum undershoot and overshoot.

These 3 tests conditions shall be tested at least using:

— H_{min} and H_{max};

— minimum and maximum modulation index *m* for the associated field strength and bit rate applied (see ISO/IEC 14443-2:2016, 9.1.2).

7.2.3.3.2 Procedure

Under the conditions defined in 7.2.3.3.1, the PICC operating at a bit rate of *fc*/128 shall answer to a REQB with ATQB.

For each optional PCD to PICC bit rate supported by the PICC, the PICC shall operate under the conditions defined in 7.2.3.3.1 after selection of that optional bit rate. This PICC shall respond correctly to an I-block transmitted at that optional bit rate.

7.2.3.4 PICC Type A or Type B for PCD to PICC bit rates of *fc*/8, *fc*/4 and *fc*/2

See 7.2.3.3.

7.2.3.5 Test report

The test report shall confirm the intended operation at the mandatory *fc*/128 bit rate. For PICCs supporting one or more of the optional PCD to PICC bit rates, the test report shall confirm the intended operation at the supported bit rates. Used test conditions shall be mentioned in the test report.

7.2.4 PICC resonance frequency (informative)

7.2.4.1 Purpose

The test may be used to measure the resonance frequency of a PICC.

When two or more PICCs are placed in the same PCD energizing field, the resonance frequency of each PICC decreases.

Care should be taken in designing each PICC resonance frequency.

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WARNING — The resonance frequency may depend on the field strength used during the measurement.

7.2.4.2 Procedure

The resonance frequency of a PICC is measured by using an impedance analyzer or a network analyzer or a LCR-meter connected to a calibration coil. The PICC should be placed on the calibration coil at a distance of 10 mm, with the axes of the two coils being congruent. The resonance frequency is that frequency at which the resistive part of the measured complex impedance is at maximum.

7.2.4.3 Test report

When applied the test report shall give the PICC resonance frequency and the measurement conditions.

7.2.5 PICC maximum loading effect

7.2.5.1 Purpose

This test is used to measure the PICC loading effect.

7.2.5.2 Procedure

Depending on the claimed PICC class, select:

— the relevant H_{min} as defined in ISO/IEC 14443-2:2016, Table 2;

— the relevant Reference PICC as defined in Table 3 and its voltage V_{load};

— the relevant Test PCD assembly as defined in Table 3.

If the PICC does not claim any particular class as specified in ISO/IEC 14443-1, then PICC Class 1 parameters, test apparatus and circuits shall be used for this test.

The PICC loading effect at H_{min} shall be measured using the Test PCD assembly. It shall not exceed the loading effect of the selected Reference PICC tuned to 13,56 MHz and calibrated to obtain V_{load} at CON3 at H_{min}. The procedure of this substitution method is as follows.

a) Tune the selected Reference PICC to 13,56 MHz as described in 5.4.3.

b) Calibrate the Test PCD assembly to produce the H_{min} operating condition on the calibration coil.

c) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'b' and adjust R2 to obtain a DC voltage of V_{load} measured at connector CON3. Alternatively, jumper J1 may be set to position 'c' and the applied voltage on CON2 is adjusted to obtain a DC voltage of V_{load} at connector CON3. In both cases, the operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.

   WARNING — R2 value should be between R2min and R2max as defined in Table 3. Check this range at least once before using the alternative method.

d) Remove the Reference PICC.

e) Place the PICC under test into the DUT position on the Test PCD assembly.

f) Measure the field strength monitored by the calibration coil. This field strength shall be greater than H_{min}.

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If PICC "Class 1" parameters were used and if the field strength measured in step f) was not greater than H_{min}, then the following alternative procedure may be used to measure the PICC loading effect:

— repeat steps b) to f) using Reference PICC 1 configured for a V_{load} of 6 V instead of the voltage defined in Table 3;

NOTE 1 The warning about R2 value is not applicable in this case.

— repeat the PICC transmission test defined in 7.2.1 with a field strength of H_{min} – 0,2 A/m(rms) instead of H_{min}, as defined in ISO/IEC 14443-2:2016, Table 2, using the $V_{LMA, PICC}$ limit defined for H_{min}, as defined in ISO/IEC 14443-2:2016, Table 8;

— repeat the PICC EMD level and low EMD time test defined in 7.2.2 with a field strength of H_{min} – 0,2 A/m(rms) instead of H_{min}, as defined in ISO/IEC 14443-2:2016, Table 2, using the $V_{E, PICC}$ limit defined for H_{min}, as defined in ISO/IEC 14443-2:2016, 10.2;

— repeat the PICC reception test defined in 7.2.3 with a field strength of H_{min} – 0,2 A/m(rms) instead of H_{min}, as defined in ISO/IEC 14443-2:2016, Table 2, using, for Type B PICC, the modulation index, m, defined for H_{min}, as defined in ISO/IEC 14443-2:2016, 9.1.2.1.

NOTE 2 This alternative procedure checks that a slightly higher PICC loading effect is compensated by a slightly lower PICC minimum operating field strength.

7.2.5.3 Test report

If the alternative procedure has not been used, the test result is only PASS if the field strength measured in step f) is greater than H_{min}, otherwise the test result is FAIL.

If the alternative procedure has been used, the test result is only PASS if the field strength measured in step f) is greater than H_{min} (using Reference PICC 1 configured for a DC voltage V_{load} of 6 V) and if the PICC transmission test defined in 7.2.1, the PICC EMD level and low EMD time test defined in 7.2.2 and the PICC reception test defined in 7.2.3 are PASS with a field strength of H_{min} – 0,2 A/m(rms) instead of H_{min}, otherwise the test result is FAIL.

The test report shall give the value of the measured field strength and the V_{load} value used.

7.3 Test methods for bit rates of 3*fc*/4, *fc*, 3*fc*/2 and 2*fc* from PCD to PICC

See Annex K.

7.4 PXD tests

PCD and PICC tests shall be applied as follows:

— when the PXD is in PCD Mode, tests defined in 7.1 and optionally 7.3 shall be applied;

— when the PXD is in PICC Mode, tests defined in 7.2 and optionally 7.3 shall be applied.

NOTE In automatic mode alternation, the PXD may be forced into the required mode.

8 Test of ISO/IEC 14443-3 and ISO/IEC 14443-4 parameters

8.1 PCD tests

See Annex H and Annex I.

8.2 PICC tests

See Annex G.

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8.3 PXD tests

8.3.1 PCD and PICC Modes

PCD and PICC tests shall be applied as follows:

— when the PXD is in PCD Mode, tests defined in 8.1 shall be applied;

— when the PXD is in PICC Mode, tests defined in 8.2 shall be applied.

NOTE In automatic mode alternation, the PXD may be forced into the required mode.

8.3.2 Automatic mode alternation

The tests defined in this subclause apply only to PXD supporting automatic mode alternation.

One cycle is defined as the duration between two consecutive beginnings of PCD Mode (RF field on).

8.3.2.1 PCD Mode and PICC Mode alternation cycle

8.3.2.1.1 Purpose

This test checks that

— each cycle does not last longer than t_{cyc},

— in each cycle, the PICC Mode lasts longer than PCD Mode, and

— the PICC Mode duration varies randomly and differs by at least t_{diff}.

8.3.2.1.2 Conditions

The PXD should not be in close proximity to another PXD, PCD or PICC.

8.3.2.1.3 Procedure

The RF field of the PXD shall be monitored and evaluated for at least 10 consecutive cycles.

a) Ensure that the PXD is in automatic Mode alternation.

b) Measure all RF field on and RF field off durations.

8.3.2.1.4 Test report

The test result is PASS if all the following conditions are met:

— no cycle lasts more than t_{cyc};

— for each t_{cyc} the PICC Mode duration (RF field off) is longer than the PCD Mode duration (RF field on);

— the PICC Mode durations vary;

— the minimum and maximum PICC Mode durations differ by at least t_{diff}.

Otherwise the test result is FAIL.

NOTE 1 The appreciation of the randomness of the PICC Mode duration may be done with common statistical methods.

NOTE 2 Due to statistical reasons the test result may be FAIL and the test may be repeated.

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8.3.2.2 PCD Mode

8.3.2.2.1 Polling

8.3.2.2.1.1 Purpose

This test checks that the PXD in automatic mode alternation polls for Type A and Type B PICCs as defined in ISO/IEC 14443-3:2016, 5.3 in each cycle of PCD Mode.

8.3.2.2.1.2 Conditions

The PXD should not be in close proximity to another PXD, PCD or PICC.

8.3.2.2.1.3 Procedure

All modulations during PCD Mode shall be monitored, and the timings between the Request commands shall be measured for at least 10 consecutive cycles.

a) Ensure that the PXD is in automatic alternation mode.

b) Monitor all Request commands during PCD Mode.

c) Measure timings before and between each command.

8.3.2.2.1.4 Test report

The test result is PASS if all the following conditions are met in each cycle:

— at least one REQA/WUPA command is sent by the PXD;

— at least one REQB/WUPB command is sent by the PXD;

— the duration of unmodulated field before at least one of the REQA/WUPA commands is more than 5 ms;

— the duration of unmodulated field before at least one of the REQB/WUPB commands is more than 5 ms.

Otherwise the test result is FAIL.

8.3.2.2.2 End of PCD Mode

8.3.2.2.2.1 Purpose

This test checks that the PXD in automatic mode alternation leaves the PCD Mode after processing of a PICC, and resumes its automatic mode alternation with the PICC Mode first.

8.3.2.2.2.2 Conditions

The PCD-test-apparatus shall be used.

8.3.2.2.2.3 Procedure

Perform the following steps:

a) Place the PCD-test-apparatus in the operating volume of the PXD.

b) Send responses to all anticollision commands sent by the PXD until the PCD-test-apparatus is in ACTIVE or PROTOCOL state.

c) Do not answer any further PXD commands.

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8.3.2.2.2.4 Test report

The test result is PASS if the PXD resumes its automatic mode alternation, possibly after application of the error handling or PICC presence check rules, with the PICC Mode first, otherwise the test result is FAIL.

8.3.2.3 PICC Mode

8.3.2.3.1 Reaction to polling

8.3.2.3.1.1 Purpose

This test checks that the PXD in automatic mode alternation responds to Type A or Type B Request commands as defined in ISO/IEC 14443-3:2016, 5.3 in each cycle of PICC Mode.

8.3.2.3.1.2 Conditions

The PICC-test-apparatus shall be used.

8.3.2.3.1.3 Procedure 1

Perform the following steps:

a) Switch the PICC-test-apparatus RF operating field off.

b) Place the PXD into the test position of the PICC-test-apparatus and ensure that the PXD is in automatic alternation mode.

c) Switch the PICC-test-apparatus RF operating field on while the PXD RF field is on.

d) Send a REQA command 5 ms after the start of PICC Mode (PXD RF field off).

e) Send a REQB command 5 ms after the end the REQA command.

f) Record the presence and the content of the PXD response.

8.3.2.3.1.4 Procedure 2

Perform the following steps:

a) Switch the PICC-test-apparatus RF operating field off.

b) Place the PXD into the test position of the PICC-test-apparatus and ensure that the PXD is in automatic alternation mode.

c) Switch the PICC-test-apparatus RF operating field on while the PXD RF field is on.

d) Send a REQB command 5 ms after the start of PICC Mode (PXD RF field off).

e) Send a REQA command 5 ms after the end the REQB command.

f) Record the presence and the content of the PXD response.

8.3.2.3.1.5 Test report

The test result is PASS if the PXD response is one of the following:

— ATQA in each of the two procedures (Type A PICC Mode);

— ATQB in each of the two procedures (Type B PICC Mode);

— ATQA in Procedure 1 and ATQB in Procedure 2 (Type A and Type B PICC Mode).

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Otherwise the test result is FAIL.

8.3.2.3.2 PICC Mode duration and exit conditions

8.3.2.3.2.1 Purpose

This test checks that, after reception of a valid REQA/WUPA command or REQB/WUPB command, the PXD in automatic mode alternation does not go in PCD Mode before a POWER-OFF state.

8.3.2.3.2.2 Conditions

The PICC-test-apparatus shall be used.

8.3.2.3.2.3 Procedure

Perform the following steps:

a) Switch the PICC-test-apparatus RF operating field on.

b) Ensure that the PXD is in automatic alternation mode and place the PXD into the test position of the PICC-test-apparatus.

c) Send a REQA command at least 5 ms after the start of PICC Mode (PXD RF field off).

d) Send a REQB command 5 ms after the end of the REQA command if there is no answer to the REQA command.

e) Keep the PICC-test-apparatus RF field on for more than 2 s.

f) Continue with anticollision commands to put the PXD in ACTIVE or PROTOCOL state and check the PXD responses.

g) Send a HALT or S(DESELECT) command to put the PXD in HALT state.

h) Keep the PICC-test-apparatus RF field on for more than 2 s.

i) Send a Request command of the Type which was answered in step c) or d) and check there is no PXD response.

j) Send a Wake-up command of the Type which was answered in step c) or d) and check there is a PXD response.

k) Switch the PICC-test-apparatus RF operating field off.

l) Check that the automatic alternation resumes in less than 1 s by monitoring the PXD RF field.

8.3.2.3.2.4 Test report

The test result is PASS if all steps of the procedure succeed, otherwise the test result is FAIL.

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Annex A
(normative)

Test PCD antennas

A.1 Test PCD antenna 1 layout including impedance matching network

Figure A.1, Figure A.2, Figure A.3, and Figure A.4 illustrate Test PCD antenna 1 layout. Drawings are not to scale.

The antenna coil track width is 1,8 mm (except for through-plated holes).

Starting from the impedance matching network, there are crossovers every 45°.

Printed circuit board (PCB): FR4 material, thickness 1,6 mm, double sided with 35 µm copper.

NOTE 1 The layout of the impedance matching network is informative.

NOTE 2 Such printed circuit boards and R_{ext} resistors are available from various commercial sources.

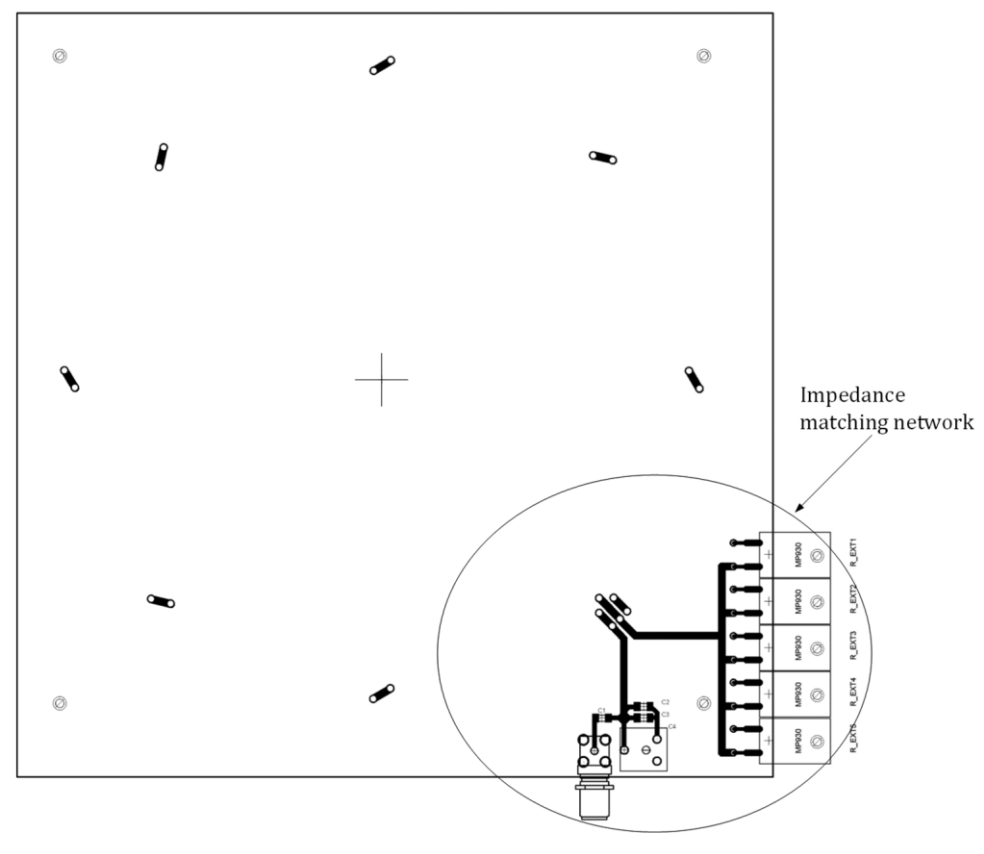

Figure A.1 — Test PCD antenna 1 layout including impedance matching network for a bit rate of *fc*/128 (view from front)

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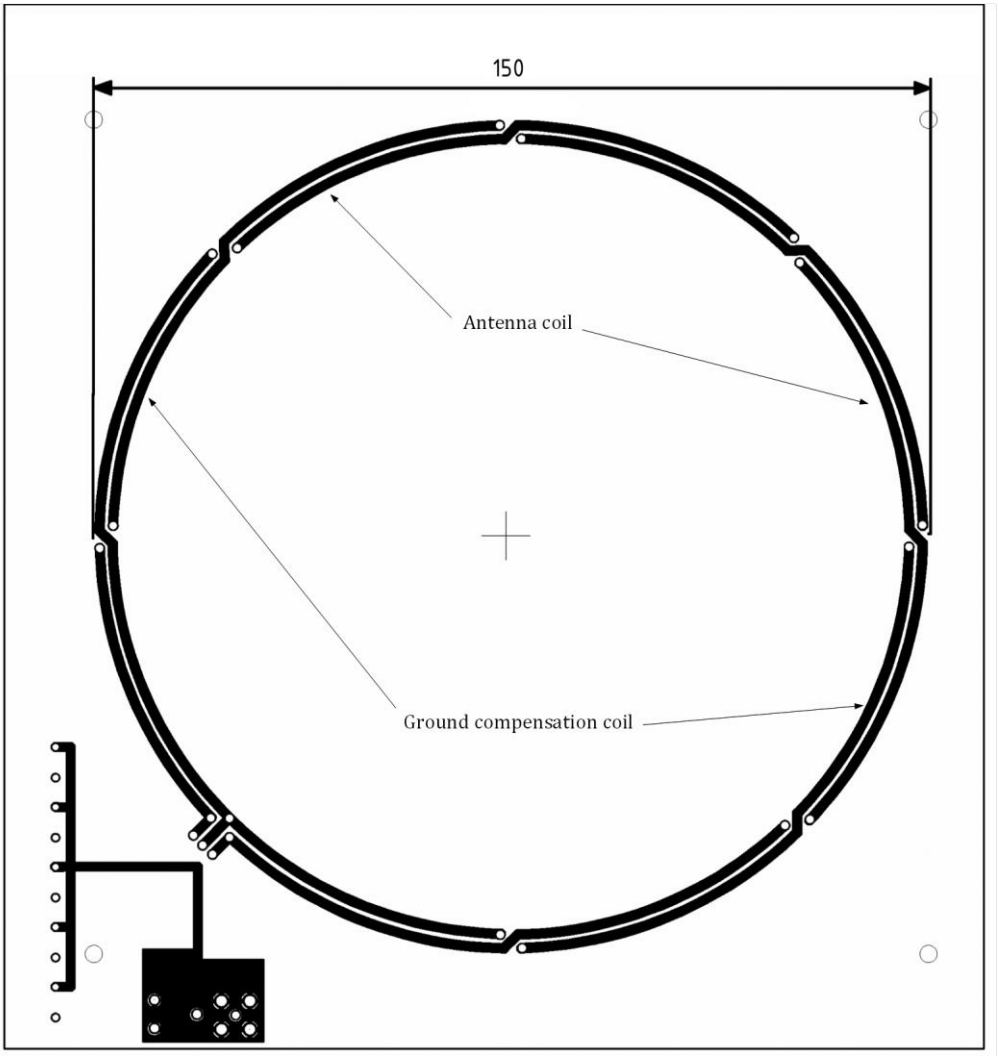

Figure A.2 — Test PCD antenna 1 layout including impedance matching network for a bit rate of *fc*/128 (view from back)

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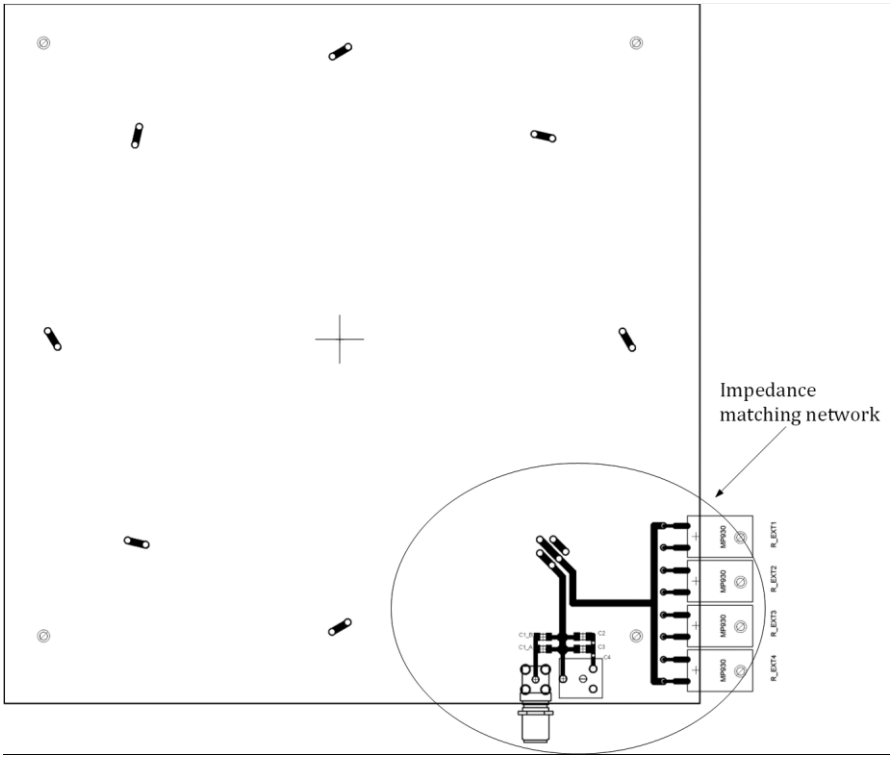

Figure A.3 — Test PCD antenna 1 layout including impedance matching network for bit rates higher than *fc*/128 (view from front)

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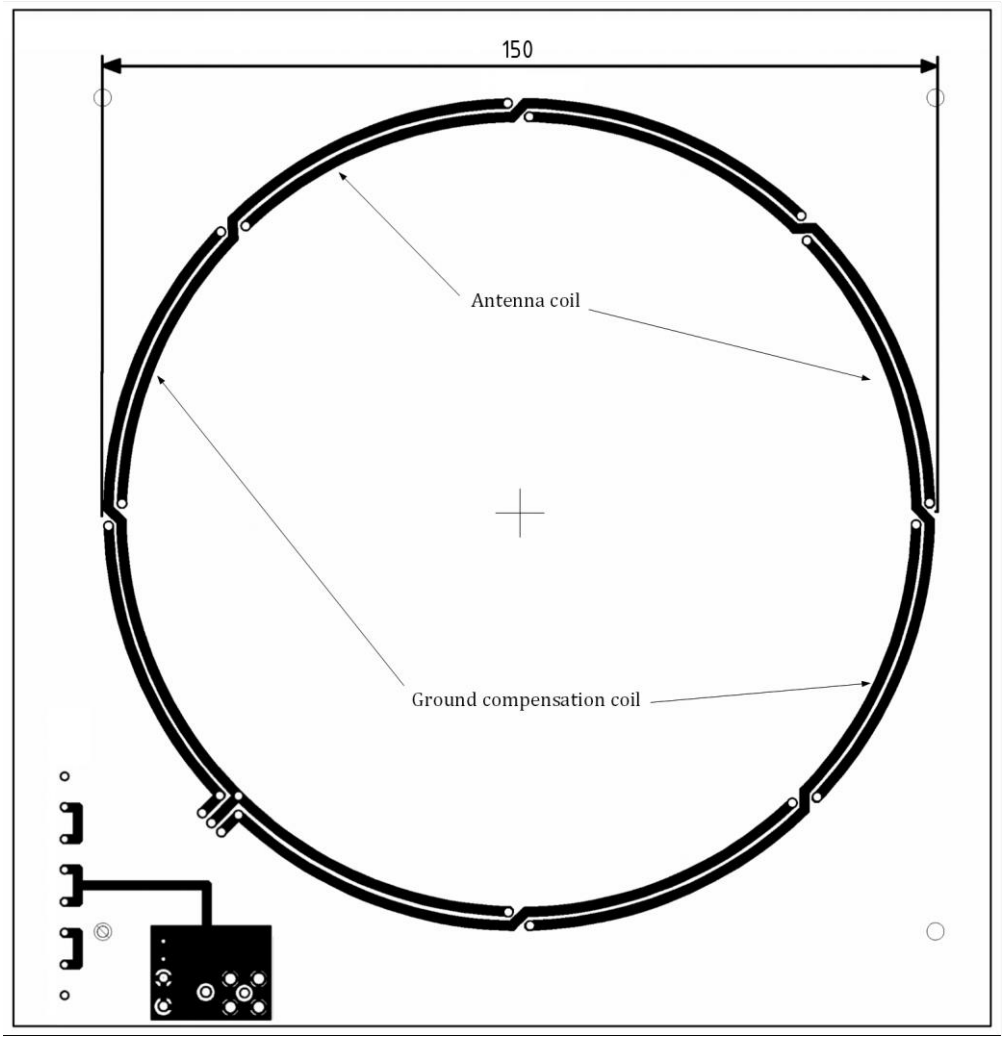

Figure A.4 — Test PCD antenna 1 layout including impedance matching network for bit rates higher than *fc*/128 (view from back)

A.2 Impedance matching network

The antenna impedance (R_{ant}, L_{ant}) is adapted to the signal generator output impedance (Z = 50 Ω) by a matching circuit (see A.2.1 and A.2.2). The capacitors C1, C1a, C1b, C2 and C3 have fixed values. The input impedance phase can be adjusted with the variable capacitor C4.

The Test PCD assembly as defined in 5.3 and in this Annex is intended to be used for time limited measurements, to avoid any overheating of the individual components. If the test is run continuously, heat dissipation shall be improved. Care shall be taken to keep maximum voltages and maximum heat dissipation within the specified limits of the individual components.

Two impedance matching networks are described: the impedance matching network for a bit rate of *fc*/128 and the impedance matching network for bit rates higher than *fc*/128; see Table A.1.

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Table A.1 — Impedance matching network use cases

Impedance matching network	Magnetic field capability	Bit rate capability
For a bit rate of *fc*/128	Up to 12 A/m (rms)	Only *fc*/128
For bit rates higher than *fc*/128	Up to 7,5 A/m (rms)	All bit rates

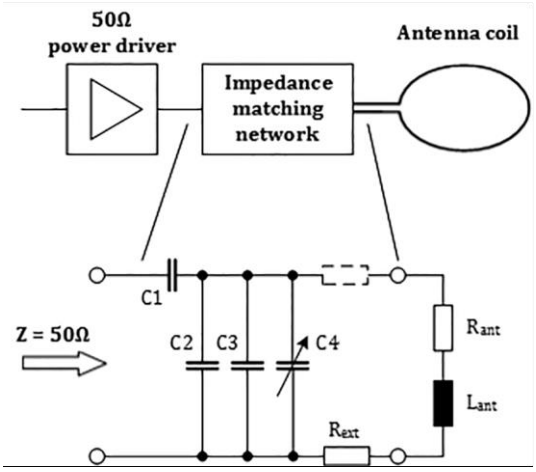
NOTE 1 The tolerance of the matched antenna impedance is ±5 Ω and ±10°.

NOTE 2 R_{ext} is placed on the ground side of the antenna coil.

NOTE 3 The power and voltage ranges include a safety margin.

The linear low distortion variable output 50 Ω power driver should be capable of emitting Type A and Type B modulations for transmission of REQA and REQB as defined in 7.2.3. The output power should be adjustable to deliver *H* fields in the range of 1,5 A/m (rms) – 12 A/m (rms). Care should be taken with the duration of fields above the upper operating range of 7,5 A/m (rms).

A.2.1 Impedance matching network for a bit rate of *fc*/128



Component Table:

	Value	Unit	Remarks
C1	47	pF	Voltage range 200 V
C2	180	pF	Voltage range 200 V
C3	22	pF	Voltage range 200 V
C4	2-27	pF	Voltage range 200 V
R_{ext}	0,94	Ω	Power range 10 W

Figure A.5 — Impedance matching network for a bit rate of *fc*/128

NOTE 1 R_{ext} may be built by connecting five resistors of 4,7 Ω 2 W in parallel.

NOTE 2 R_{ext} may still be placed at the position marked with a dashed outline, as shown in Figure A.5.

NOTE 3 R_{ext} may be 4 W if the maximum field is up to 7,5 A/m (rms).

NOTE 4 The parasitic capacitance of the antenna is not shown Figure A.5.

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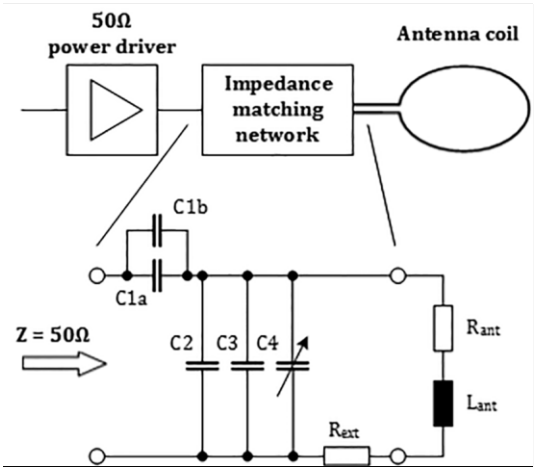
A.2.2 Impedance matching network for bit rates higher than *fc*/128



Component Table:

	Value	Unit	Remarks
C1a	82	pF	Voltage range 200 V
C1b	8,2	pF	Voltage range 200 V
C2	150	pF	Voltage range 200 V
C3	10	pF	Voltage range 200 V
C4	2-27	pF	Voltage range 200 V
R_{ext}	4,7	Ω	Power range 20 W

Figure A.6 — Impedance matching network for bit rates higher than *fc*/128

NOTE 1 R_{ext} may be built by a parallel circuit of each two resistors of 4,7 Ω 5 W in series.

R_{ext} should be placed on the ground side of the antenna as drawn in Figure A.6.

NOTE 2 The parasitic capacitance of the antenna is not shown in Figure A.6.

A.3 Test PCD antenna 2

A.3.1 Test PCD antenna 2 layout including impedance matching network

Figure A.7 and Figure A.8 illustrate the Test PCD antenna 2 layout. Drawings are not to scale.

The antenna coil track width is 1,8 mm (except for through-plated holes).

Starting from the impedance matching network there are crossovers every 45°.

Printed circuit board (PCB): FR4 material, thickness 1,6 mm, double sided with 35 µm copper.

NOTE 1 The layout and the position of the impedance matching network are informative. The outer PCB dimensions are informative.

NOTE 2 Such printed circuit boards and R_{ext} resistors are available from various commercial sources.

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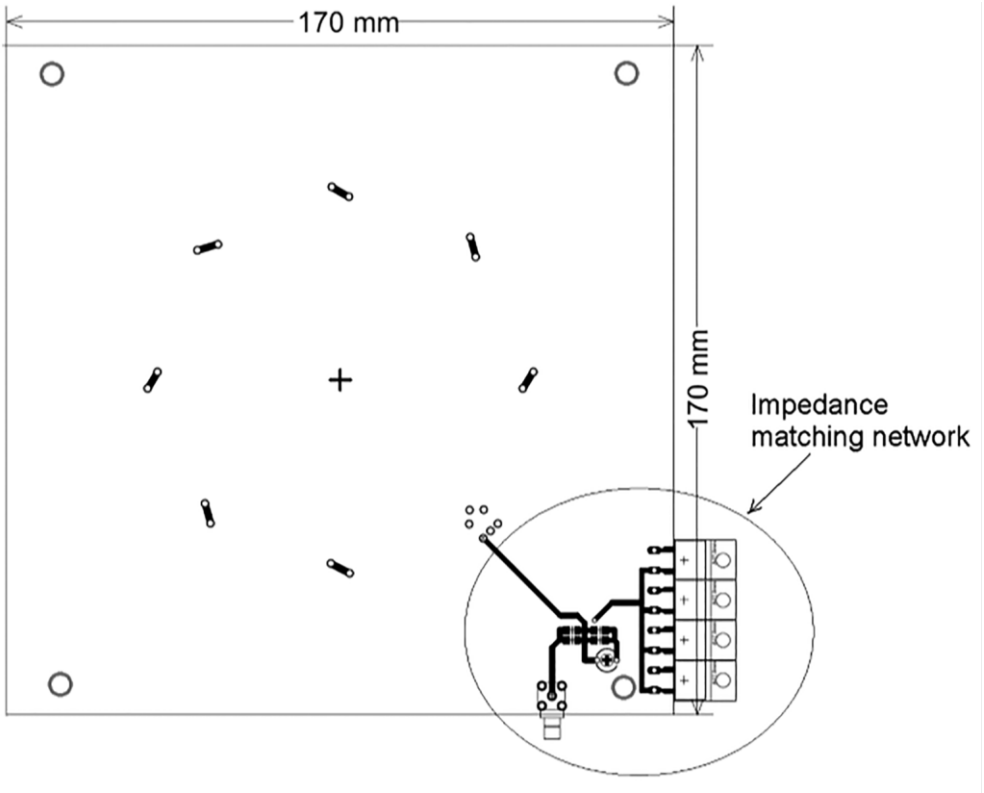

Figure A.7 — Test PCD antenna 2 layout including impedance matching network (view from front)

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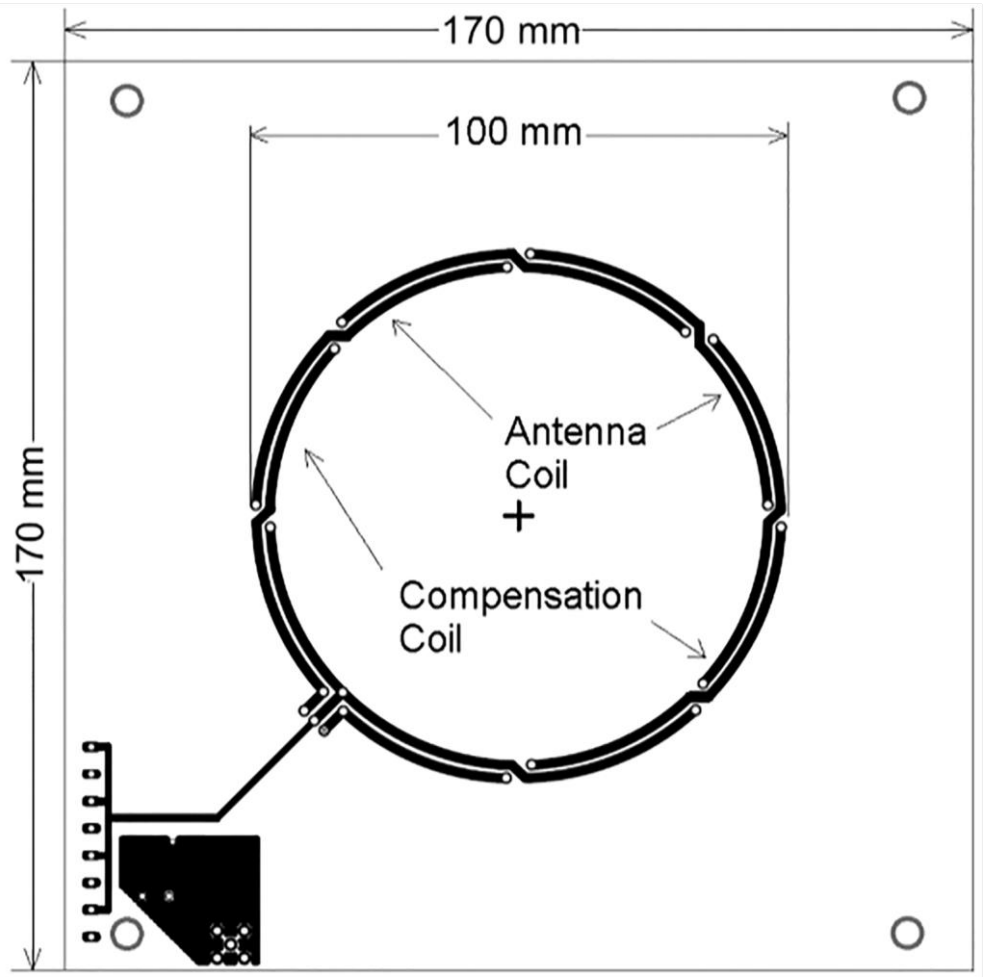

Figure A.8 — Test PCD antenna 2 layout including impedance matching network (view from back)

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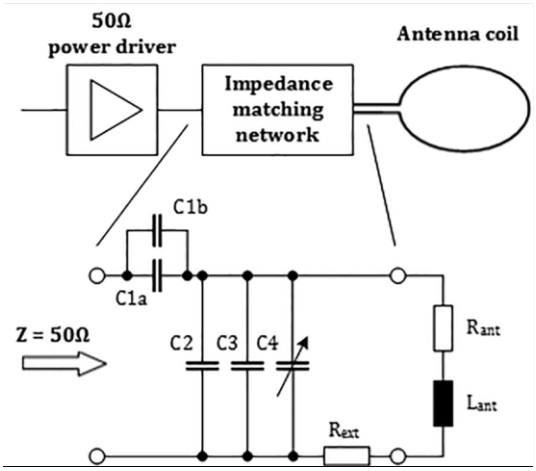
A.3.2 Impedance matching network 2



Component Table:

	Value	Unit	Remarks
C1a	100	pF	Voltage range 200 V
C1b	12	pF	Voltage range 200 V
C2	270	pF	Voltage range 200 V
C3	18	pF	Voltage range 200 V
C4	2-27	pF	Voltage range 200 V
R_{ext}	2,7	Ω	Power range 20 W

Figure A.9 — Impedance matching network 2

NOTE 1 R_{ext} may be built by either a parallel circuit composed of two equal branches having two resistors of 2,7 Ω 5 W in series each or a parallel circuit of 10 Ω, 10 Ω, 10 Ω and 15 Ω, 5 W.

R_{ext} should be placed on the ground side of the antenna as drawn in Figure A.9.

NOTE 2 The parasitic capacitance of the antenna is not shown in Figure A.9.

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