



BSI Standards Publication

Cards and security devices for personal identification — Test methods

Part 6: Contactless proximity objects

National foreword

This British Standard is the UK implementation of ISO/IEC 10373-6:2020+A1:2021. It supersedes BS ISO/IEC 10373-6:2020+A2:2020, which is withdrawn.

The start and finish of text introduced or altered by amendment is indicated in the text by tags. Tags indicating changes to ISO/IEC text carry the number of the ISO/IEC amendment. For example, text altered by ISO/IEC amendment 1 is indicated by **A1** **A1**.

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A list of organizations represented on this committee can be obtained on request to its committee manager.

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Cards and security devices for personal identification — Test methods —

Part 6: Contactless proximity objects

*Cartes et dispositifs de sécurité pour l'identification personnelle —
Méthodes d'essai —*

Partie 6: Objets sans contact de proximité



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Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of document should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

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For an explanation of the voluntary nature of standards, the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT) see www.iso.org/iso/foreword.html.

This document was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, SC 17, *Cards and security devices for personal identification*.

This fourth edition cancels and replaces the third edition (ISO/IEC 10373-6:2016), which has been technically revised. It also incorporates the Amendment ISO/IEC 10373-6:2016/Amd.3:2018.

The main changes compared to the previous edition are as follows:

- enhancement of test methods for PCD load modulation reception and PICC transmission including introduction of Active Reference PICC and PICC amplitude and phase drift analysis tool;
- introduction of PICC Type A Frame Delay Time (FDT) determination method;
- extension of frame with error correction test methods.

A list of all the parts in the ISO/IEC 10373 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

Cards and security devices for personal identification — Test methods —

Part 6: Contactless proximity objects

1 Scope

The ISO/IEC 10373 series defines test methods for characteristics of identification cards according to the definition given in ISO/IEC 7810. Each test method is cross-referenced to one or more base standards, which can be ISO/IEC 7810 or one or more of the supplementary standards that define the information storage technologies employed in identification card applications.

NOTE 1 Criteria for acceptability do not form part of the ISO/IEC 10373 series, but can be found in the International Standards mentioned above.

This document defines test methods which are specific to proximity cards and objects, proximity coupling devices and proximity extended devices, defined in ISO/IEC 14443-1, ISO/IEC 14443-2, ISO/IEC 14443-3 and ISO/IEC 14443-4.

NOTE 2 Test methods defined in this document are intended to be performed separately. A given proximity card or object, proximity coupling device or proximity extended device, is not required to pass through all the tests sequentially.

ISO/IEC 10373-1 defines test methods which are common to one or more integrated circuit card technologies and other parts in the ISO/IEC 10373 series deal with other technology-specific tests.

The conformance test plan defined in [Annex O](#) specifies the list of tests applicable for each part of the ISO/IEC 14443 series.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 7810, *Identification cards — Physical characteristics*

ISO/IEC 14443-1:2018, *Cards and security devices for personal identification — Contactless proximity objects — Part 1: Physical characteristics*

ISO/IEC 14443-2:2020, *Cards and security devices for personal identification — Contactless proximity objects — Part 2: Radio frequency power and signal interface*

ISO/IEC 14443-3:2018, *Cards and security devices for personal identification — Contactless proximity objects — Part 3: Initialization and anticollision*

ISO/IEC 14443-4:2018, *Cards and security devices for personal identification — Contactless proximity objects — Part 4: Transmission protocol*

3 Terms, definitions, symbols and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO/IEC 14443-1, ISO/IEC 14443-2, ISO/IEC 14443-3, ISO/IEC 14443-4 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- ISO Online browsing platform: available at <https://www.iso.org/obp>
- IEC Electropedia: available at <http://www.electropedia.org/>

3.1.1

base standard

standard to which the *test method* (3.1.8) is used to verify conformance

3.1.2

CascadeLevels

number of cascade levels of the PICC

3.1.3

Command Set

set describing the PICC commands during initialization and anticollision

Note 1 to entry: See ISO/IEC 14443-3:2018, 6.4 for PICC Type A and ISO/IEC 14443-3:2018, 7.5 for PICC Type B.

3.1.4

loading effect

change in PCD antenna current caused by the presence of PICC(s) in the field due to the mutual coupling modifying the PCD antenna resonance and quality factor

3.1.5

Mute

no response within a specified timeout

EXAMPLE Expiration of FWT.

3.1.6

scenario

defined typical protocol and application specific communication to be used with the *test methods* (3.1.8) defined in this document

3.1.7

Test Initial State

TIS

element from PICC states that is the PICC state before performing a specific PICC command from *Command Set* (3.1.3)

3.1.8

test method

method for testing characteristics of identification cards for the purpose of confirming their compliance with International Standards

3.1.9

Test Target State

TTS

element from PICC states that is the PICC state after performing a specific PICC command from *Command Set* (3.1.3)

3.2 Symbols and abbreviated terms

For the purposes of this document, the symbols and abbreviated terms given in ISO/IEC 14443-1, ISO/IEC 14443-2, ISO/IEC 14443-3, ISO/IEC 14443-4 and the following apply.

NOTE Elements in bold square brackets **[]** are optional definitions.

Answer to ATTRIB(cid)	Answer to ATTRIB, i.e. (MBLI = mbli, CID = cid, CRC_B), with mbli an arbitrary hex value (see ISO/IEC 14443-3:2018, 7.11)
ATTRIB(cid, fsdi)	Default ATTRIB command with PUPI from ATQB, CID = cid and Maximum Frame Size Code value = fsdi, i.e. ('1D' PUPI cid fsdi '01 00' CRC_B)
DUT	Device under test
$\boxed{A_1} H_0$	PCD field strength during power level management test procedures $\boxed{A_1}$
$I(c)_n$ (inf [CID = cid] [NAD = nad] [$\sim$ CRC])	ISO/IEC 14443-4 I-block with chaining bit $c \in \{1, 0\}$, block number $n \in \{1, 0\}$ and information field inf. By default no CID and no NAD will be transmitted. If CID = cid $\in \{0 \dots 15\}$ is specified, it will be transmitted as second parameter. If NAD = nad $\in \{0 \dots 'FF'\}$ is specified, it will be transmitted as third parameter (or second parameter if no CID is transmitted). If the literal ' $\sim$ CRC' is not specified, a valid CRC corresponding to the communication signal interface of the PICC will be transmitted by default (i.e. CRC_A or CRC_B)
IUT	Implementation Under Test (ISO/IEC 9646); within the scope of this document, IUT represents the PCD under the test
LT	Lower Tester (ISO/IEC 9646), the PICC-emulation part of the PCD-test-apparatus
N/A	Not applicable
PPS(cid, dri, dsi)	Default PPS request with CID = cid, DRI = dri and DSI = dsi, i.e. ('D' + cid '11' dsi $\times$ 4 + dri CRC_A)
R(ACK [CID = cid] [$\sim$ CRC]) _n	ISO/IEC 14443-4 R(ACK) block with block number n. The definition of the optional CID and $\sim$ CRC symbols is as described in the $I(c)_n$ block above
R(NAK [CID = cid] [$\sim$ CRC]) _n	ISO/IEC 14443-4 R(NAK) block with block number n. The definition of the optional CID and $\sim$ CRC symbols is as described in the $I(c)_n$ block above
RATS(cid, fsdi)	Default RATS command with CID = cid and FSDI value = fsdi i.e. ('E0' fsdi $\times$ 16 + cid CRC_A)
READY(I)	READY state in cascade level I, $I \in \{1, 2, 3\}$; e.g. READY(2) is a PICC cascade level 2
READY*(I)	READY* state in cascade level I, $I \in \{1, 2, 3\}$; e.g. READY*(2) is a PICC cascade level 2
REQB(N)	REQB command with N as defined in ISO/IEC 14443-3:2018, 7.7
S(WTX)(WTXM [CID = cid] [$\sim$ CRC])	ISO/IEC 14443-4 S(WTX) block with parameter WTXM. The definition of the optional CID and $\sim$ CRC symbols is as described in the $I(c)_n$ block above

S(DESELECT [CID = cid] [,~CRC])	ISO/IEC 14443-4 S(DESELECT) block. The definition of the optional CID and ~CRC symbols is as described in the I(c) _n block above
SAK(cascade)	the SELECT(I) answer with the cascade bit (bit 3) set to (1)b
SAK(complete)	the SELECT(I) answer with the cascade bit (bit 3) set to (0)b
SEL(c)	Select code of level c (i.e. SEL(1) = '93', SEL(2) = '95', SEL(3) = '97')
SELECT(I)	SELECT command of cascade level I, i.e. SELECT(1) = ('93 70' UIDTX ₁ BCC CRC_A) SELECT(2) = ('95 70' UIDTX ₂ BCC CRC_A) SELECT(3) = ('97 70' UIDTX ₃ BCC CRC_A)
SLOTMARKER(n)	Slot-MARKER command with slot number n, i.e. (16 × (n – 1) + 5 CRC_B)
TB-PDU	Transmission Block Protocol Data Unit, which consists of either I-block, R-block or S-block
TEST_COMMAND_SEQUENCE1	Sequence of commands used for several PICC tests. NOTE Its definition depends on applicative layer and represents a standard transaction of the application supported by the DUT. The applicant may also provide a specified set of commands.
TEST_COMMAND1(1)	Default test command consisting of one unchained I-block NOTE This command depends on the negotiated maximum frame size value of the PICC.
TEST_COMMAND1(n), n > 1	Default test command consisting of n chained I-blocks (PCD chaining) NOTE This command depends on the negotiated maximum frame size value of the PICC.
TEST_COMMAND1(n) _k	INF field of k'th I-block chain of TEST_COMMAND1(n) NOTE This command depends on the negotiated maximum frame size value of the PICC.
TEST_COMMAND2(n), n > 1	Default test command which expects a response consisting of n chained I-blocks NOTE This command depends on the negotiated maximum frame size value of the PCD.
TEST_COMMAND3	Default test command consisting of one I-block which needs more than FWT time for execution
TEST_COMMAND4	Default test command which expects a response of one I-block complying with the PICC transmission minimum frame length required for the PICC transmission test
TEST_RESPONSE1(n)	INF field of the response to TEST_COMMAND1(n) NOTE This response is assumed to be always unchained.

TEST_RESPONSE2(n)	Response to TEST_COMMAND2(n) NOTE This response depends on the negotiated maximum frame size value of the PCD.
TEST_RESPONSE2(n) _k	INF field of k'th I-block chain of TEST_RESPONSE2(n) NOTE This response depends on the negotiated maximum frame size value of the PCD.
TEST_RESPONSE3	Response I-block to TEST_COMMAND3 NOTE This response is always assumed to be unchained.
TEST_RESPONSE4	Response I-block to TEST_COMMAND4
TM-PDU	Test Management Protocol Data Unit (ISO/IEC 9646-1, PDU)
t_{START}	Start of PICC transmission
UIDTX ₁	Transmitted UID 32-bit data at cascade level I (see Table 1)
UT	Upper Tester (ISO/IEC 9646), the master part of the PCD-test-apparatus
UT_APDU	Upper Tester Application Protocol Data Unit: a packet of data to be sent by the PCD to the LT through the RF interface
V_{load}	DC voltage measured at connector CON3 of the Reference PICC
WUPB(N)	WUPB command with N as defined in ISO/IEC 14443-3:2018, 7.7
~X	Bit sequence consisting of the inverted bits of bit sequence X or any other bit sequence different from X
X[[a...b]]	Bit subsequence of bit sequence X consisting of the bits between position a and b included. If a > b then the sequence is empty
X[[n]]	Bit at position n of bit sequence X. First bit is at position 1
X[n]	Byte at position n of bit sequence X. First byte is at position 1 (i.e. $X[n] = X[((n - 1) \times 8 + 1 \dots n \times 8)]$)

Table 1 — Mapping from UID to UIDTX

Cascade level	Single UID PICC	Double UID PICC	Triple UID PICC
UIDTX ₁	UID0 UID1 UID2 UID3	'88' UID0 UID1 UID2	'88' UID0 UID1 UID2
UIDTX ₂	—	UID3 UID4 UID5 UID6	'88' UID3 UID4 UID5
UIDTX ₃	—	—	UID6 UID7 UID8 UID9

4 Default items applicable to the test methods

4.1 Test environment

Unless otherwise specified, testing shall take place in an environment of temperature $23\text{ °C} \pm 3\text{ °C}$ ($73\text{ °F} \pm 5\text{ °F}$) and of relative humidity 25 % to 75 %.

4.2 Pre-conditioning

No environmental pre-conditioning of PICCs or PCDs is required by the test methods in this document.

4.3 Setup tolerances

The following absolute tolerances shall be used when adjusting the Test PCD assembly modulation waveform:

- 1) for timings ($t_1, t_2, t_3, t_5, t_6, t_r, t_f$):
 - a) $\pm 1/f_c$ for a PCD to PICC bit rate of $f_c/128$
 - b) $\pm 0,5/f_c$ for a PCD to PICC bit rate of $f_c/64$
 - c) $\pm 0,3/f_c$ for PCD to PICC bit rates higher than $f_c/64$
- 2) for envelope overshoot, Type A, PCD to PICC bit rate of $f_c/128$: $\pm 1\%$ of H_{INITIAL}
- 3) for envelope overshoot, Type A, PCD to PICC bit rates higher than $f_c/128$: $\pm 0,01 \times (1-a)$
- 4) for envelope overshoot and undershoot, Type B: $\pm 0,01 \times (1-b)$
- 5) for the modulation index m : $\pm 0,5\%$
- 6) for the pulse shape factor a : $\pm 0,02$
- 7) for PCD field envelope during 60 % of t_2 : $\pm 0,5\%$ of H_{INITIAL}

Unless otherwise specified, a tolerance of $\pm 5\%$ shall be applied to the quantity values given to specify the characteristics of the test equipment (e.g. linear dimensions) and the test method procedures (e.g. test equipment adjustments).

4.4 Spurious inductance

Resistors and capacitors should have negligible inductance.

4.5 Measurement uncertainty

The measurement uncertainty for each quantity determined by these test methods shall be stated in the test report.

Basic information is given in ISO/IEC Guide 98-3.

4.6 DUT position

Unless otherwise specified, the PICC and Reference PICC antennas shall be centered on the sense coil a of the test PCD assembly.

4.7 Test conditions for PCD

Unless otherwise specified, the test conditions defined in [Table 2](#) shall be applied.

Table 2 — Test conditions for PCD

Conditions	Values
Type	Type A and Type B
Test positions	Position 0: See Table 3 Position Z_{max} : See Table 3

Table 2 (continued)

Conditions	Values
Reference PICCs	Reference PICC 1, Reference PICC 2 and Reference PICC 3 In accordance with the support of optional PICC classes as declared by the PCD manufacturer in Table 3: — Reference PICC 4 if PICC Class 4 is supported, — Reference PICC 5 if PICC Class 5 is supported, — Reference PICC 6 if PICC Class 6 is supported.

The information defined in Table 3 shall be provided by the PCD manufacturer.

Table 3 — PCD manufacturer information

Parameter	Description	Unit
Position 0	Position and orientation of the Reference PICCs on the PCD surface. This position may be PICC classes dependent.	
Position $Z_{\max}$	Position with maximum operating distance on the Z axis ^a . This position may be PICC classes dependent.	
Temperature range	Minimum and maximum temperature values.	°C
Optional PICC classes	List of supported optional PICC classes (4 and/or 5 and/or 6).	
 Support of PLI _{ATQ} handling	Ability to change power level (and therefore field strength) after receiving PLI _{ATQ} from a PICC	
Support of PLI _{CID} handling	Ability to change power level (and therefore field strength) after receiving PLI _{CID} from a PICC	
PCD to PICC supported bit rates	List of supported optional PCD to PICC bit rates.	
PICC to PCD supported bit rates	List of supported optional PICC to PCD bit rates.	
Maximum frame size supported	Maximum frame size in reception.	bytes
PCD to PICC frame with error correction supported	Frame with error correction from PCD to PICC.	
PICC to PCD frame with error correction supported	Frame with error correction from PICC to PCD.	
 Type A collision resolution supported	Collision resolution for Type A	
^a Z axis shall be perpendicular to the PCD surface through Position 0. If the PCD surface is not flat, Z axis shall correspond to the axis along which PICCs would habitually be held to the PCD and shall be coherent with PCD ergonomics; if not, the test laboratory may choose to redefine it (directionally).		

Unless otherwise specified, the values defined in Table 4 shall be used to adjust PCD-test-apparatus parameters.

Table 4 — Values of the PCD-test-apparatus parameters unless otherwise specified

Parameter	Value	Applies to
PCD to PICC and PICC to PCD bit rates	$f_c/128$	Type A and Type B
Load modulation amplitude	More than 20 mV at $H_{\min}$	Type A and Type B
Reference PICCs resonance frequency	16,5 MHz	Type A and Type B
J1 setting	position 'a'	Type A and Type B
J2 setting	position 'a'	Type A and Type B
Reference PICCs position	Position $Z_{\max}$	Type A and Type B
Start Of Frame (SOF) timing	10 etu "0" followed by 2 etu "1"	Type B
End Of Frame (EOF) timing	10 etu "0"	Type B
Extra Guard Time (EGT) timing	0 etu	Type B
TR0 for ATQB and DESELECT	$200/f_s$	Type B

Table 4 (continued)

Parameter	Value	Applies to
Frame waiting time	Any value as specified in ISO/IEC 14443-4:2018, 7.2	Type A and Type B
UID	Any of the size and contents as specified in ISO/IEC 14443-3:2018, 6.5.4	Type A
TR1	$140/f_s$	Type B
FSCI	8	Type A
Maximum Frame Size Code in ATQB	8	Type B

4.8 Test conditions for PICC

Unless otherwise specified, the test conditions defined in [Table 5](#) shall be applied:

Table 5 — Test conditions for PICC

Conditions	Values
Field strength ^a	For PICC Class 1: 1,5 A/m, 2,5 A/m, 4,5 A/m and 7,5 A/m For PICC Class 2 and Class 3: 1,5 A/m, 2,5 A/m, 4,5 A/m and 8,5 A/m For PICC Class 4: 2 A/m, 4 A/m, 7 A/m and 12 A/m For PICC Class 5: 2,5 A/m, 4,5 A/m, 8 A/m and 14 A/m For PICC Class 6: 4,5 A/m, 7 A/m, 11 A/m and 18 A/m
^a Any additional field strength values between H_{min} and H_{max} may be applied.	

The information defined in [Table 6](#) shall be provided by the PICC manufacturer.

Table 6 — PICC manufacturer information

Parameter	Description	Unit
Location, center and size of the antenna	Drawing with dimensions of the PICC outside shape and the position of the external rectangle/circle of the claimed PICC class.	
PICC class (optional) ^a	Claimed PICC class	
Resonance frequency range (optional)	Minimum and maximum resonance frequency	MHz
Communication signal interface	Supported communication signal interface(s): — Type A — Type B — Type A and Type B	
Temperature range	Minimum and maximum temperature values	°C
Supported PLI_{ATQ} values	List of supported optional PLI_{ATQ} values in Answer to Request	
Supported PLI_{CID} values	List of supported optional PLI_{CID} values in CID field	
PCD to PICC supported bit rates	List of supported optional PCD to PICC bit rates	
PICC to PCD supported bit rates	List of supported optional PICC to PCD bit rates	
Same bit rate for both directions	Indication if only same bit rate from PCD to PICC and from PICC to PCD is supported	
Random or fixed UID (Type A) or PUPI (Type B)	Indication whether the UID (Type A) or PUPI (Type B) is random or fixed	
Maximum frame size supported	Maximum frame size in reception	bytes
^a If not provided, test methods for Class 1 shall be used		

Table 6 (continued)

Parameter	Description	Unit
PCD to PICC frame with error correction supported	Frame with error correction from PCD to PICC	
PICC to PCD frame with error correction supported	Frame with error correction from PICC to PCD	
TEST_COMMAND_SEQUENCE1	See 0.2.1	
TEST_COMMAND1	See 0.2.1	
TEST_COMMAND2	See 0.2.1	
TEST_COMMAND3	See 0.2.1	
TEST_COMMAND4	See 0.2.1	
^a If not provided, test methods for Class 1 shall be used		

A1

Unless otherwise specified, the values defined in [Table 7](#) shall be used to adjust PICC-test-apparatus parameters.

Table 7 — Values of the PICC-test-apparatus parameters unless otherwise specified

Parameter	Value	Applies to
Parameters applicable for all PCD to PICC bit rates		
FSDI	8	Type A
Start Of Frame (SOF) timing	10 etu "0" followed by 2 etu "1"	Type B
End Of Frame (EOF) timing	10 etu "0"	Type B
Extra Guard Time (EGT) timing	0 etu	Type B
Maximum Frame Size Code in ATTRIB	8	Type B
Parameters applicable for a PCD to PICC bit rate of $f_c/128$		
PCD field envelope during 60 % of t_2	0,5 %	Type A
t_1	$40/f_c$	Type A
t_2	$7/f_c$	Type A
t_3	$12/f_c$	Type A
t_4	$6/f_c$	Type A
Overshoot	0	Type A and Type B
Modulation index m	12 %	Type B
Rise time t_r , fall time t_f	$12/f_c$	Type B
Parameters applicable for a PCD to PICC bit rate of $f_c/64$		
a	0,1	Type A
t_1	$18/f_c$	Type A
t_5	$15/f_c$	Type A
t_6	$9/f_c$	Type A
Overshoot	0	Type A and Type B
Modulation index m	12 %	Type B
Rise time t_r , fall time t_f	$10/f_c$	Type B
Parameters applicable for a PCD to PICC bit rate of $f_c/32$		
a	0,2	Type A
t_1	$9/f_c$	Type A
t_5	$7/f_c$	Type A
t_6	$8/f_c$	Type A
Overshoot	0	Type A and Type B

Table 7 (continued)

Parameter	Value	Applies to
Modulation index m	12 %	Type B
Rise time t_r , fall time t_f	$8/f_c$	Type B
Parameters applicable for a PCD to PICC bit rate of $f_c/16$		
a	0,4	Type A
t_1	$5/f_c$	Type A
t_5	$4/f_c$	Type A
t_6	$5/f_c$	Type A
Overshoot	0	Type A and Type B
Modulation index m	12 %	Type B
Rise time t_r , fall time t_f	$6/f_c$	Type B
Parameters applicable for a PCD to PICC bit rate of $f_c/8$		
Overshoot	0	Type A and Type B
Modulation index m	8 % for short modulation pulses	Type A and Type B
Rise time t_r , fall time t_f	$5/f_c$	Type A and Type B
Parameters applicable for a PCD to PICC bit rate of $f_c/4$		
Overshoot	0	Type A and Type B
Modulation index m	8 % for short modulation pulses	Type A and Type B
Rise time t_r , fall time t_f	$4/f_c$	Type A and Type B
Parameters applicable for a PCD to PICC bit rate of $f_c/2$		
Overshoot	0	Type A and Type B
Modulation index m	8 % for short modulation pulses	Type A and Type B
Rise time t_r , fall time t_f	$3/f_c$	Type A and Type B
Parameters applicable for a PCD to PICC bit rate of $3f_c/4$ and $3f_c/2$		
PR	56°	Type A and Type B
ISI _d	0	Type A and Type B
ISI _m	1	Type A and Type B
Phase noise	0,03	Type A and Type B
Parameters applicable for a PCD to PICC bit rate of f_c and $2f_c$		
PR	60°	Type A and Type B
ISI _d	0	Type A and Type B
ISI _m	1	Type A and Type B
Phase noise	0,0125	Type A and Type B

5 Apparatus and circuits for test of ISO/IEC 14443-1 and ISO/IEC 14443-2 parameters

5.1 Overview

This clause defines the test apparatus and test circuits for verifying the operation of a PICC or a PCD according to ISO/IEC 14443-1 and ISO/IEC 14443-2. The test apparatus includes the following:

- 1) measurement instruments (see 5.2);
- 2) calibration coil (see 5.3);
- 3) Test PCD assembly (see 5.4);

- 4) Reference PICC and Active Reference PICC (see 5.5);
- 5) PICC transmission test setup (see 5.6);
- 6) EMD test setup (see 5.7).

These are described in the following subclauses.

5.2 Minimum requirements for measurement instruments — Oscilloscope

The digital sampling oscilloscope shall be capable of sampling at a rate of at least 500 million samples per second with a resolution of at least 8 bits at optimum scaling and shall have an overall minimum bandwidth of 250 MHz. The oscilloscope should have the capability to output the sampled data as a text file to facilitate mathematical and other operations such as windowing on the sampled data using software programs (see Annex E and Annex F).

NOTE The overall bandwidth is the combination of oscilloscope and probing system bandwidth.

5.3 Calibration coils

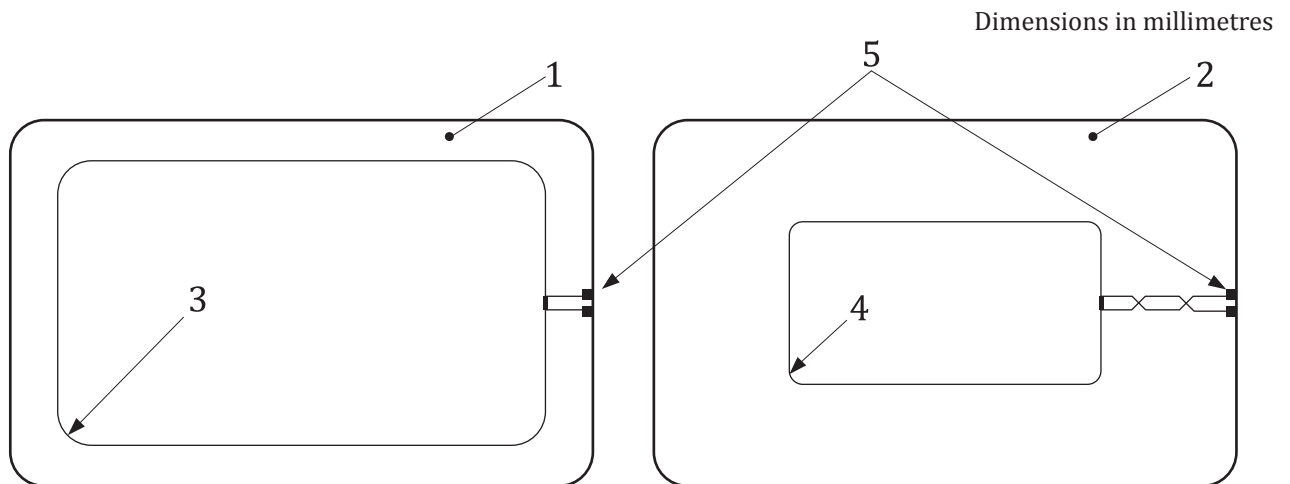
5.3.1 General

This subclause defines the size, thickness and characteristics of the calibration coils 1 and 2.

Calibration coil 1 shall be used only in Test PCD assembly 1 and calibration coil 2 shall be used only in Test PCD assembly 2.

5.3.2 Size of the calibration coil card

The calibration coil card shall consist of an area which has the height and width of an ID-1 type defined in ISO/IEC 7810 containing a single turn coil concentric with the card outline (see Figure 1).



Key

- 1 calibration coil 1 (ISO/IEC 7810 ID-1 outline)
- 2 calibration coil 2 (ISO/IEC 7810 ID-1 outline)
- 3 coil 72×42 , 1 turn
- 4 coil 46×24 , 1 turn
- 5 connections

NOTE Drawings are not to scale.

Figure 1 — Calibration coils 1 and 2

5.3.3 Thickness and material of the calibration coil card

The thickness of the calibration coil card shall be less than that of an ID-1 card. It shall be constructed of a suitable insulating material.

5.3.4 Coil characteristics

The coil on the calibration coil card shall have one turn. Relative dimensional tolerance shall be $\pm 2\%$.

The outer size of the calibration coil 1 shall be 72 mm $\times$ 42 mm with corner radius 5 mm.

NOTE 1 The area over which the field is integrated is approximately 3 000 mm².

NOTE 2 At 13,56 MHz the approximate inductance is 250 nH and the approximate resistance is 0,4 Ω .

The open circuit calibration factor for the calibration coil 1 is 0,318 V (rms) per A/m (rms) [equivalent to 900 mV (peak-to-peak) per A/m (rms)].

The outer size of the calibration coil 2 shall be 46 mm $\times$ 24 mm with corner radius 2 mm.

NOTE 3 The area over which the field is integrated is approximately 1 100 mm².

NOTE 4 At 13,56 MHz the approximate inductance is 140 nH and the approximate resistance is 0,3 Ω .

The open circuit calibration factor for the calibration coil 2 is 0,118 V (rms) per A/m (rms) [equivalent to 333 mV (peak-to-peak) per A/m (rms)].

The coil shall be made as a printed coil on printed circuit board (PCB) plated with 35 μ m copper. Track width shall be 500 μ m with a relative tolerance of $\pm 20\%$. The size of the connection pads shall be 1,5 mm $\times$ 1,5 mm.

A high impedance oscilloscope probe with an input admittance equivalent to a parallel capacitance $C_p < 14$ pF and a parallel resistance $R_p > 9$ k Ω at 13,56 MHz shall be used to measure the (open circuit) voltage induced in the coil.

The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.

5.4 Test PCD assembly

5.4.1 General

Two Test PCD assemblies are defined:

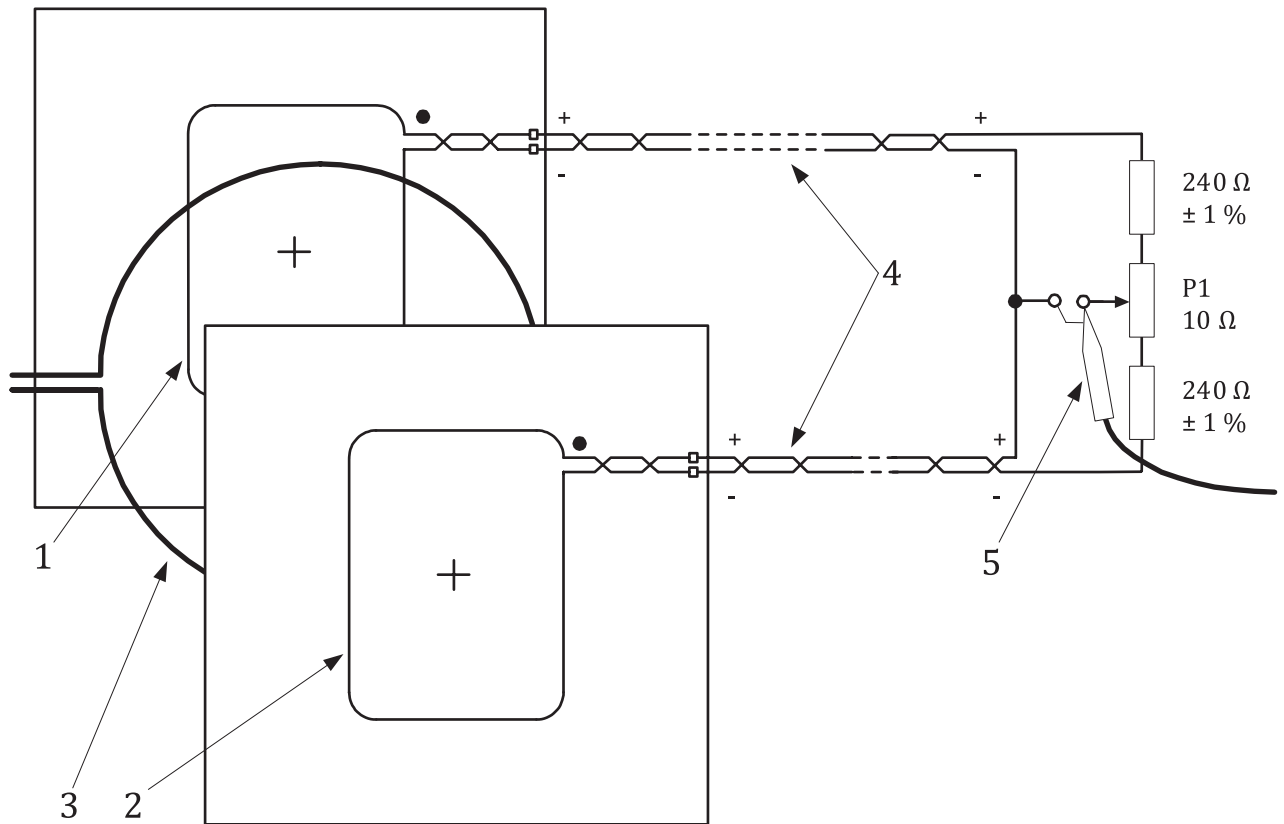
- 1) Test PCD assembly 1 for PICCs of "Class 1", "Class 2" and "Class 3" and for PICCs which do not claim compliance with a PICC class;
- 2) Test PCD assembly 2 for PICCs of "Class 4", "Class 5" and "Class 6".

Each Test PCD assembly shall consist of a circular Test PCD antenna and two parallel sense coils, sense coil a and sense coil b, as shown in principle by [Figure 2](#). The sense coils shall be connected such that the signal from one coil is in opposite phase to the other. The 10 Ω potentiometer P1 serves to fine adjust the balance point when the sense coils are not loaded by a PICC or any magnetically coupled circuit. The capacitive load of the probe including its parasitic capacitance shall be less than 14 pF.

The capacitance of the connections and of the oscilloscope probe should be kept to a minimum for reproducibility.

In order to avoid any unintended misalignment in case of an unsymmetrical set-up the tuning range of the potentiometer P1 is only 10 Ω . If the set-up cannot be compensated by the 10 Ω potentiometer P1, the overall symmetry of the set-up should be checked.

The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.



Key

- 1 sense coil a
- 2 sense coil b
- 3 test PCD antenna
- 4 identical length twisted pairs or coaxial cables of less than 100 mm
- 5 probe connected to oscilloscope

Figure 2 — Test set-up (principle)

5.4.2 Test PCD antenna

In Test PCD assembly 1 the Test PCD antenna 1 shall have a diameter of 150 mm.

In Test PCD assembly 2 the Test PCD antenna 2 shall have a diameter of 100 mm.

Each Test PCD antenna construction shall conform to the corresponding drawings in [Annex A](#).

The matching of each Test PCD antenna should be accomplished by using an impedance analyzer or a network analyzer or an LCR meter. If either an impedance analyzer or a network analyzer or an LCR meter is not available, then the matching may be accomplished with the procedure given in [Annex B](#).

5.4.3 Sense coils

In Test PCD assembly 1 the size of the sense coils 1 shall be 100 mm × 70 mm with corner radius 10 mm.

In Test PCD assembly 2 the size of the sense coils 2 shall be 60 mm × 47 mm with corner radius 10 mm.

Each sense coil construction shall conform to the corresponding drawings in [Annex C](#).

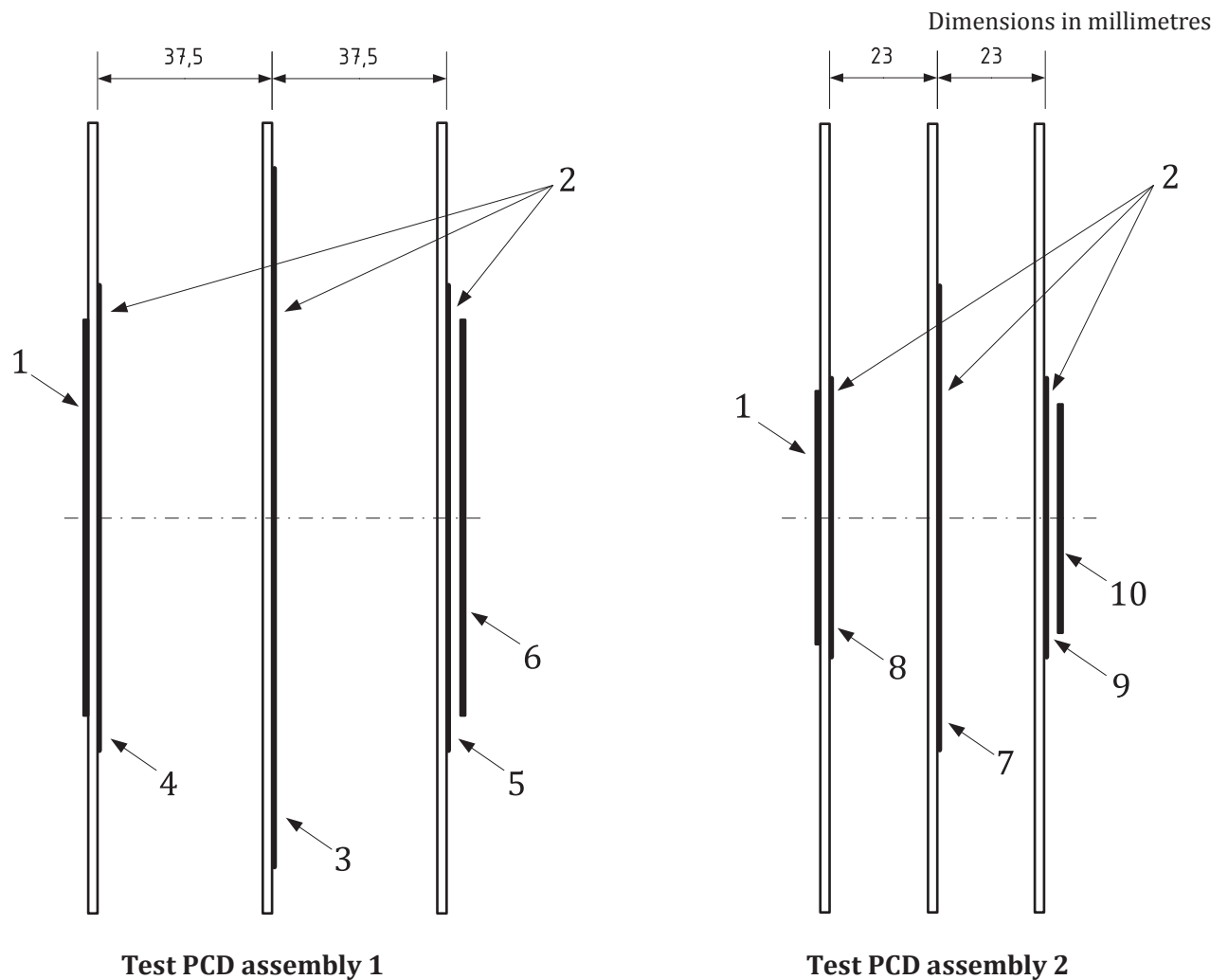
5.4.4 Assembly of Test PCD

The sense coils 1 and Test PCD antenna 1 shall be assembled parallel and with the sense and antenna coils coaxial and such that the distance between the active conductors is 37,5 mm as shown in [Figure 3](#), Test PCD assembly 1.

The sense coils 2 and Test PCD antenna 2 shall be assembled parallel and with the sense and antenna coils coaxial and such that the distance between the active conductors is 23 mm as shown in [Figure 3](#), Test PCD assembly 2.

The dimensional tolerance shall be better than $\pm 0,5$ mm. The distance between the coil in the DUT and the calibration coil shall be equal with respect to the coil of the Test PCD antenna.

NOTE These distances are chosen to offer a strong and homogenous magnetic field in the DUT position.



Key

- 1 DUT
- 2 active conductors
- 3 test PCD antenna 1
- 4 sense coil 1a
- 5 sense coil 1b
- 6 calibration coil 1
- 7 test PCD antenna 2
- 8 sense coil 2a
- 9 sense coil 2b
- 10 calibration coil 2

NOTE Drawings are not to scale.

Figure 3 — Test PCD assembly 1 and Test PCD assembly 2

5.5 Reference PICC and Active Reference PICC

5.5.1 General

Two reference equipments are defined to test PCDs:

- 1) the Reference PICC;
- 2) the Active Reference PICC.

5.5.2 Reference PICC

5.5.2.1 Introduction

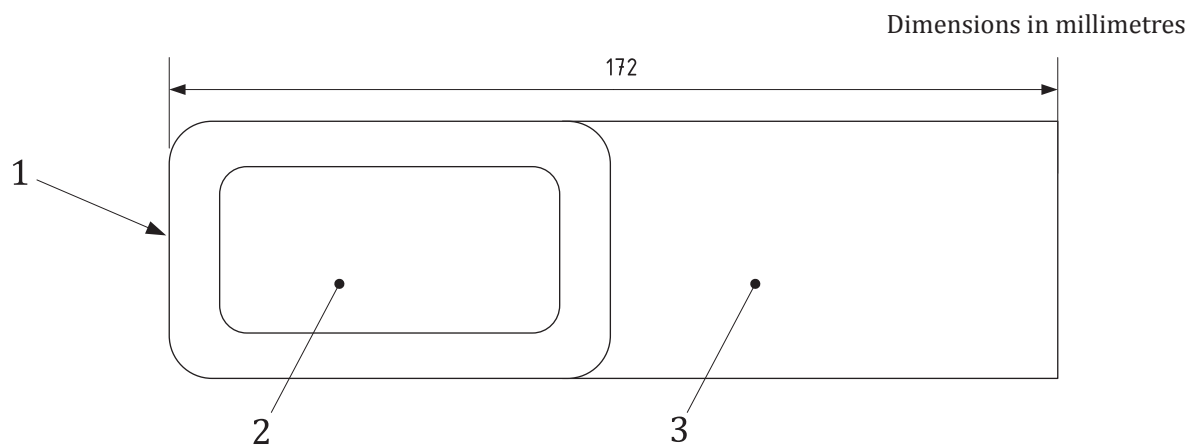
A Reference PICC is defined to test the ability of a PCD to

- 1) generate a field strength of at least $H_{\min}$ and not exceeding $H_{\max}$,
- 2) transmit a modulated signal to a PICC,
- 3) be immune against EMD signals from the PICC.

in its operating volume.

5.5.2.2 Dimensions of the Reference PICC

The Reference PICC shall consist of an area containing the coils which has the height and width defined in ISO/IEC 7810 for ID-1 type. An area external to this, containing the circuitry which emulates the required PICC functions, shall be appended in such a way as to allow insertion into the test set-ups and so as to cause no interference to the tests. The dimensions shall be as shown in [Figure 4](#).



Key

- 1 outline ISO/IEC 7810 ID-1
- 2 location of coils
- 3 location of circuitry

NOTE Drawing is not to scale.

Figure 4 — Reference PICC dimensions

5.5.2.3 Reference PICC construction

The Reference PICCs coils layouts shall be as defined in [D.1](#). If connectors are used between the coils and the circuitry, those connectors shall have minimal, if any, effect on the RF measurements.

The Reference PICC shall have a circuit diagram as defined in [Figure 5](#) and component values as defined in [Table 8](#).

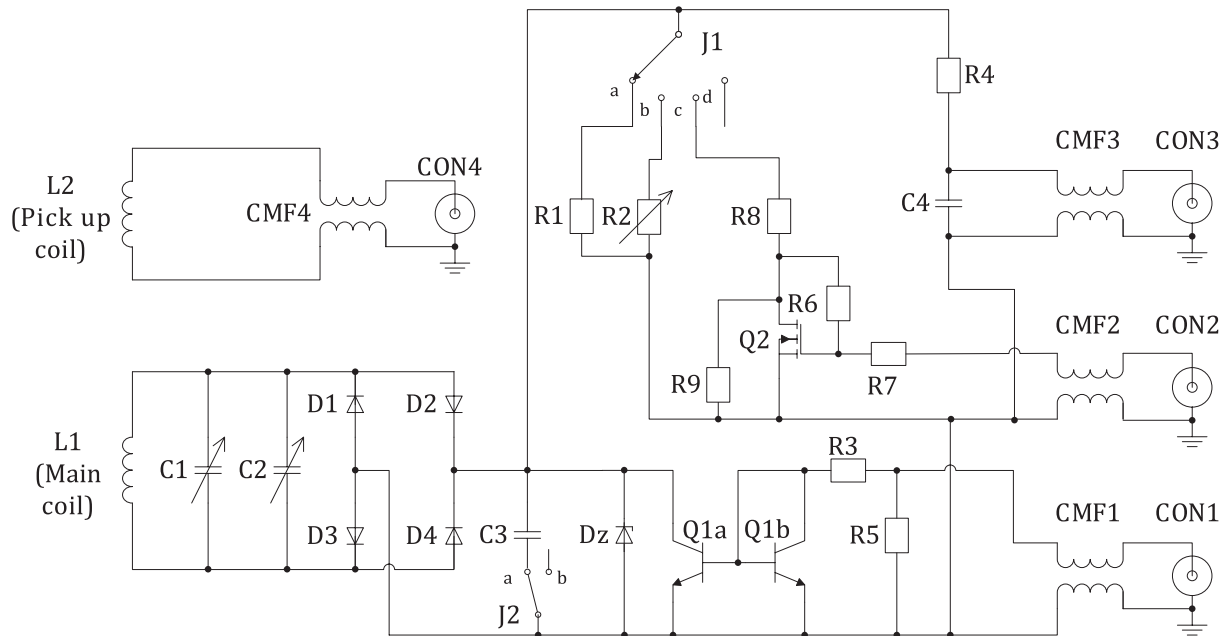


Figure 5 — Reference PICC circuit diagram

NOTE Position 'd' of jumper J1 is RFU.

Table 8 — Reference PICC components list

Component	Value	Component	Value
L1	As defined in D.1	C1	7 pF – 50 pF ^b
L2	As defined in D.1	C2	3 pF – 10 pF ^b
R1	1,8 kΩ	C3	27 pF
R2	0 kΩ – 2 kΩ ^a	C4	1 nF
R3	220 Ω	D1, D2, D3, D4	BAR43S or equivalent ^c
R4	51 kΩ	Dz	BZX84, 15 V or equivalent ^c
R5	51 Ω	Q1a, Q1b	BCV61A or equivalent
R6	500 kΩ	Q2	BSS83 or equivalent
R7	110 kΩ	CMF1, CMF2, CMF3, CMF4	ACM3225-102-2P or equivalent
R8	51 Ω	CON1, CON2, CON3, CON4	RF connector
R9	1,5 kΩ		

^a A multi-turn potentiometer (turns ≥10) should be used.

^b Q-factor shall be higher than 100 at 13,56 MHz.

^c Care should be taken on parameters C_j (Junction capacitance), C_p (Package capacitance), L_s (Series inductance) and R_s (Series resistance) of equivalent diodes. Note that these values may not be available in the datasheet.

At CON1 the load modulation signal shall be applied. The load modulation can be determined in Test PCD assembly. When not used, the load modulation signal generator shall be disconnected or set to 0 V.

With the voltage at CON2 the Reference PICC load can be adjusted until the required DC voltage shows at CON3.

The Reference PICC DC voltage shall be measured at CON3 using a high impedance voltmeter and the connection wires should be twisted or coaxial.

The PCD waveform parameters are picked up at CON4 using a high impedance oscilloscope probe. The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.

Position 'a' of J2 shall be used for testing bit rates of $f_c/128$, $f_c/64$, $f_c/32$ and $f_c/16$.

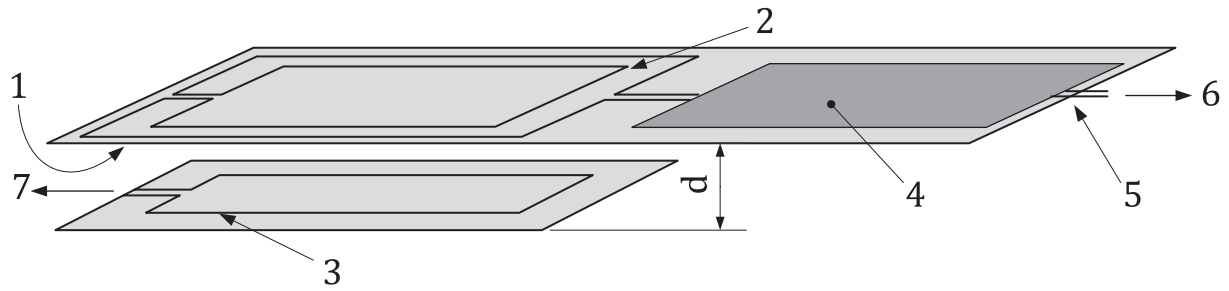
Position 'b' of J2 shall be used for testing bit rates of $f_c/8$, $f_c/4$ and $f_c/2$.

5.5.2.4 Reference PICC resonance frequency tuning

The Reference PICC resonance frequency shall be calibrated with the following procedure.

- a) Set jumper J1 to position 'a'.
- b) Connect the calibration coil directly to a signal generator and the Reference PICC CON3 to a high impedance voltmeter. Connect all the other connectors to the same equipment as used for the tests.
- c) Locate the Reference PICC at a distance $d = 10$ mm above the calibration coil with the axes of the two coils (calibration coil and Reference PICC main coil) being congruent (see [Figure 6](#)).
- d) Drive the calibration coil with a sine wave set to the desired resonance frequency.
- e) Adjust the Reference PICC capacitors C1 and C2 to get maximum DC voltage at CON3.
- f) Adjust the signal generator drive level to obtain a DC voltage at CON3 of V_{load} as defined in [Table 12](#).
- g) Repeat steps e) and f) until the maximum voltage after step e) is V_{load} .
- h) Calibrate the Test PCD assembly to produce the H_{min} operating condition on the calibration coil.
- i) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'b' and adjust R2 to obtain a DC voltage of V_{load} measured at CON3. The operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.
- j) Repeat steps b) to g) with the obtained value of R2.

Instead of a signal generator, a vector network analyzer may be used if sufficient power is provided to produce V_{load} at CON3 while reaching the maximum resistive part of the measured complex impedance of the calibration coil.

**Key**

- 1 main coil (bottom side)
- 2 pick up coil (top side)
- 3 calibration coil (top side)
- 4 reference PICC circuitry
- 5 CON3
- 6 to voltmeter
- 7 to signal generator
- d distance (see procedure above)

NOTE Drawing is not to scale.

Figure 6 — Reference PICC frequency tuning set-up (principle)

5.5.3 Active Reference PICC

5.5.3.1 General

An Active Reference PICC is defined to test the ability of a PCD to receive a load modulation signal from the PICC in its operating volume.

5.5.3.2 Dimensions of the Active Reference PICC

See [5.5.2.2](#).

5.5.3.3 Active Reference PICC construction

The Active Reference PICCs coils layouts shall be as defined in [D.2](#). If connectors are used between the coils and the circuitry, those connectors shall have minimal, if any, effect on the RF measurements.

The Active Reference PICC shall have a circuit diagram as defined in [Figure 7](#) and component values as defined in [Table 9](#). Input and output connectors are described in [Table 10](#).

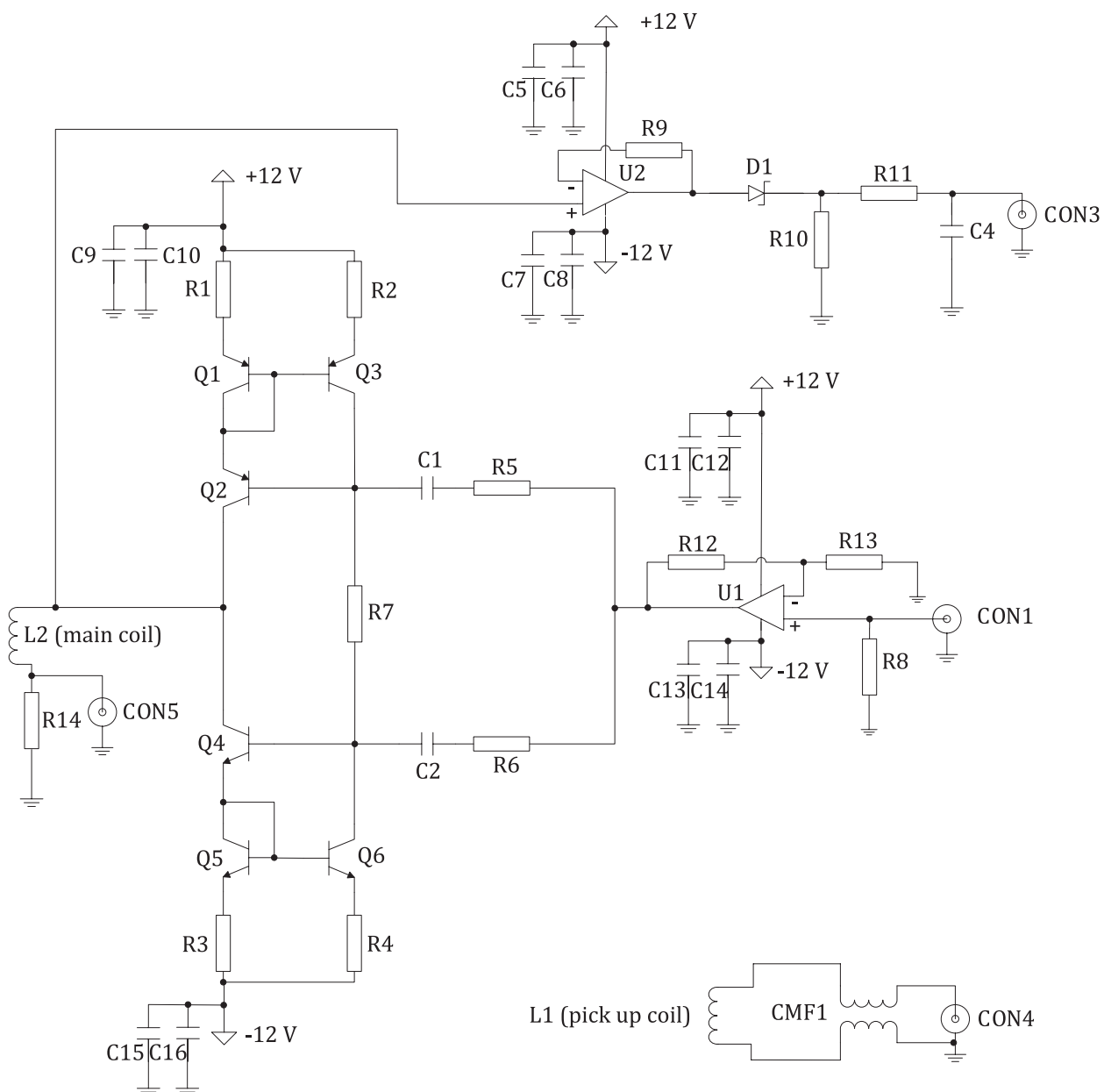


Figure 7 — Active Reference PICC circuit diagram

The resistor R14 should be placed as close as possible to the antenna coil.

Table 9 — Active Reference PICC components list

Component	Value	Power dissipation	Component	Value
R1, R3	10 Ω	235 mW	C1, C2, C4	1 nF
R2, R4, R5, R6	100 Ω	<50 mW	D1	BAT54 or equivalent
R7	1,3 k Ω	250 mW	Q1, Q2, Q3	BD136 or equivalent
R8	50 Ω	250 mW	Q4, Q5, Q6	BD135 or equivalent
R9	1,8 k Ω	<50 mW	U1, U2	THS3091 or equivalent
R10, R11	1,5 k Ω	<50 mW	C5, C7, C9, C11, C13, C15	4,7 μ F

Table 9 (continued)

Component	Value	Power dissipation	Component	Value
R12, R13	1,2 k Ω	<50 mW	C6, C8, C10, C12, C14, C16	100 nF
R14	0,5 Ω	<50 mW		

Table 10 — Active Reference PICC Input/Output connector description

Connector	Input/Output	Description
CON1	Input	Generation of the Active Reference PICC transmission and unmodulated state US (loading effect).
CON3	Output	Image of the field received when the Active Reference PICC does not transmit (DC voltage).
CON4	Output	PCD carrier extraction.
CON5	Output	Image of the field transmitted by the Active Reference PICC.

The Active Reference PICC received DC voltage shall be measured at CON3 using a high impedance voltmeter and the connection wires should be twisted or coaxial.

High impedance oscilloscope probes shall be used to pick up the signals at CON4 and CON5.

5.6 PICC transmission test setup

5.6.1 General description

The PICC transmission test setup contains:

- a signal generator with low phase noise, which is used to generate an RF carrier field and to synthesize PCD test commands sent to the PICC under test;
- the Test PCD assembly;
- a signal amplitude analyzing device made of a signal acquiring device (e.g. an oscilloscope) and the PCD phase stability analysis tool defined in [Annex M](#).

The signal amplitude analyzing device shall be able to carry out instantaneous phase versus time measurements with fixed frequency, high dynamic range, low measurement uncertainty and high time resolution. See [5.2](#) for minimum requirements on the amplitude analyzing device.

5.6.2 Phase stability precondition test

5.6.2.1 Purpose

In order to guarantee an RF field with high frequency stability, a phase stability test shall be performed and passed successfully by the PICC transmission test setup. The aim of this precondition test is to verify that the test apparatus used for PICC transmission measurements provides a signal frequency with high stability.

The phase stability test is passed if the maximum phase drift is smaller than $\pm 3^\circ$ when measured as described in [5.6.2.2](#).

NOTE The maximum phase drift value of $\pm 3^\circ$ for the phase stability test covers the measurement uncertainty and noise as well as component fabrication tolerances and temperature dependencies.

5.6.2.2 Test procedure

Perform the following steps to assess the instantaneous phase and compute its maximum phase drift at least at $H_{\min}$ and $H_{\max}$:

- a) Tune the Reference PICC 1 to 13,56 MHz as described in [5.5.2.4](#).
- b) Adjust the RF power delivered by the signal generator to the Test PCD antenna to the required field strength as measured by the calibration coil.
- c) Place the Reference PICC 1 into the DUT position on the Test PCD assembly, set jumper J1 to position 'b' and adjust R2 to obtain a voltage of V_{load} at CON3. Alternatively, jumper J1 may be set to position 'c' and the applied voltage on CON2 is adjusted to obtain a voltage of V_{load} at CON3. In both cases the operating field condition shall be verified by monitoring the voltage in the calibration coil and adjusting if necessary.
- d) Record the non-modulated RF carrier signal of the pick up coil for a time period of at least 25 ms.
- e) Compute the maximum phase drift from the instantaneous phase using the PCD phase stability analysis tool defined in [Annex M](#). Check if the maximum phase drift of the instantaneous phase is always smaller than $\pm 3^\circ$ with respect to the initial phase at the very beginning of the time period..

5.6.2.3 Test report

The test report shall contain the maximum phase drift of the PICC transmission test setup and shall state whether the requirements have been fulfilled.

5.7 EMD test setup

5.7.1 General description

The EMD test setup contains the following:

- 1) a signal generator with low phase noise, which is used to synthesize both an EMD test pattern and PCD test commands sent to the PICC under test;
- 2) the Test PCD assembly;
- 3) a signal amplitude analyzing device:
 - a) either a signal acquiring device (e.g. oscilloscope) and appropriate computation software;
 - b) or a spectrum analyzer (see additional constraints in [5.7.2](#)).

The signal amplitude analyzing device shall be able to carry out power versus time measurements with fixed frequency, fixed bandwidth, high dynamic range, low measurement uncertainty and high time resolution.

The PICC EMD tests may be performed using the RF output signal of a commercial PCD. The PCD EMD test may use a PICC emulator to generate the EMD test pattern.

5.7.2 Computation of power versus time

The beginning of the captured signal shall be windowed by a Bartlett window of exactly two subcarrier cycles. Fourier transformation of these windowed samples produces one power value. By shifting the Bartlett window by steps of $1/f_c$ from the beginning to the end of the captured signal, the desired power versus time result is finally computed.

NOTE The resulting 3 dB bandwidth of the above described window is 531 kHz and its noise equivalent bandwidth amounts to 843 kHz.

The computation of the power versus time shall be performed at $f_c + f_s$ and $f_c - f_s$, using a scaling such that a pure sinusoidal signal results in its peak magnitude. An example of computation is provided in [Annex J](#).

In case of using a spectrum analyzer, the analyzer shall have at least an equivalent analysis bandwidth. It shall pass the noise floor precondition test, as defined in [5.7.3](#), and there shall be some additional margin of $10/f_c$ on $t_{E, PICC}$ requirement and no spikes above the EMD limit.

5.7.3 Noise floor precondition test

5.7.3.1 Purpose

In order to ensure a high dynamic range and sufficient sensitivity, a noise floor measurement shall be performed and passed successfully by the EMD test setup. The aim of this precondition test is to verify that the test apparatus used for EMD level measurement satisfies a minimum noise requirement.

The noise floor test is passed if the noise standard deviation is at least three times smaller than the EMD limit $V_{E, PICC}$, when measured as described in [5.7.3.2](#).

The noise standard deviation is determined by calculating the root-mean-square value of the results of the Fourier transformation, as described in [5.7.2](#).

NOTE This noise floor can be obtained either with a 14-bit digitizer at a sampling rate of 100 million samples per second or with an 8-bit digital oscilloscope at sampling rate of 1 000 million samples per second.

5.7.3.2 Procedure

Perform the following steps to assess the noise floor at least at H_{min} and H_{max} .

- a) Tune the Reference PICC 1 to 13,56 MHz.
- b) Adjust the RF power delivered by the signal generator to the Test PCD antenna to the required field strength as measured by the calibration coil.
- c) Place the Reference PICC 1 into the DUT position on the Test PCD assembly, set jumper J1 to position 'b' and adjust R2 to obtain a voltage of V_{load} at CON3. Alternatively, jumper J1 may be set to position 'c' and the applied voltage on CON2 is adjusted to obtain a voltage of V_{load} at CON3. In both cases the operating field condition shall be verified by monitoring the voltage in the calibration coil and adjusted if necessary.
- d) Record the signal of the sense coils for a time period of at least 250 μs .
- e) Compute the noise standard deviations at $f_c + f_s$ and $f_c - f_s$ using suitable computer software, as e.g. the one given in [Annex J](#). Check if these noise standard deviations are three times smaller than $V_{E, PICC}$.

5.7.3.3 Test report

The test report shall state the noise standard deviations at $f_c + f_s$ and $f_c - f_s$ and shall state whether the requirements have been fulfilled.

6 Test of ISO/IEC 14443-1 parameters

6.1 PCD tests

6.1.1 Alternating magnetic field

6.1.1.1 Purpose

This test determines that the PCD generates a field not higher than the average value specified in ISO/IEC 14443-1 for each PICC class, in any possible PICC position.

6.1.1.2 Procedure

Apply the following procedure with each Reference PICC:

- Tune the Reference PICC to 19 MHz as described in 5.5.2.4 steps a) to g).
- Calibrate the Test PCD assembly (see Table 11) to produce the average field value specified in ISO/IEC 14443-1:2018, 4.4 on the calibration coil.
- Place the Reference PICC into the DUT position on the Test PCD assembly (see Table 11). Switch the jumper J1 to position 'b' and adjust R2 to obtain a DC voltage of 3 V measured at CON3. The operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.

WARNING — R2 value should be between $R2_{\min}$ and $R2_{\max}$ as defined in Table 11.

- Position the Reference PICC in any possible PICC position. The DC voltage at CON3 shall not exceed 3 V.

WARNING — If the PCD field is not continuously emitted, the DC voltage measurement shall be done when the PCD field is present.

- If exceeded, use the same conversion factor to measure the maximum and average DC voltage and convert in field strength to check the maximum and the average field values specified in ISO/IEC 14443-1:2018, 4.4 in a 30 s period.

Table 11 — R2 value for alternating magnetic field test

Reference PICC	$R2_{\min}$	$R2_{\max}$	Test PCD assembly
1	56 Ω	68 Ω	Test PCD assembly 1
2	97 Ω	119 Ω	Test PCD assembly 1
3	100 Ω	122 Ω	Test PCD assembly 1
4	84 Ω	102 Ω	Test PCD assembly 2
5	76 Ω	92 Ω	Test PCD assembly 2
6	88 Ω	108 Ω	Test PCD assembly 2

6.1.1.3 Test report

The test report shall give the DC voltage measured at CON3 for each Reference PICC. The test result is PASS only if the PCD meets the requirements given by the last two steps of the procedure in 6.1.1.2 for each Reference PICC, otherwise the test result is FAIL.

6.2 PICC tests

6.2.1 Alternating magnetic field

6.2.1.1 Purpose

The purpose of this test is to check the behavior of the PICC in relation to alternating magnetic field exposure at 13,56 MHz.

6.2.1.2 Apparatus

The Test PCD assembly shall be used to produce the alternating magnetic field.

6.2.1.3 Procedure

The procedure is as follows.

- a) In accordance with the PICC class, adjust the RF power delivered by the signal generator to the Test PCD antenna to a field strength of the average level specified in ISO/IEC 14443-1:2018, 4.4 as measured by the calibration coil.
- b) Place the PICC under test in the DUT position and readjust immediately the RF drive into the Test PCD antenna to the required field strength if necessary.
- c) After 5 min, remove the PICC from the DUT position for at least 5 s.
- d) In accordance with the PICC class, adjust the RF power delivered by the signal generator to the Test PCD antenna to a field strength of the maximum level specified in ISO/IEC 14443-1:2018, 4.4 as measured by the calibration coil.
- e) Place the PICC under test in the DUT position and readjust immediately the RF drive into the Test PCD antenna to the required field strength if necessary.
- f) Apply for 5 min an ASK 100 % modulation to this field with the following duty cycle:
 - 1) 5 s at 0 A/m (rms);
 - 2) 25 s at the maximum level specified in ISO/IEC 14443-1:2018, 4.4, in accordance with the PICC class.
- g) Wait for 30 s at 0 A/m (rms).
- h) Check that the PICC operates as intended. This check should be done at least by successfully executing PICC transmission test defined in [7.2.1](#).

6.2.1.4 Test report

The test report shall state whether or not the PICC operates as intended.

6.2.2 Void

The static electricity test, which was defined in former editions of this document, is no longer present.

6.3 PXD tests

PCD and PICC tests shall be applied as follows:

- 1) when the PXD is in PCD Mode, tests defined in [6.1](#) shall be applied;
- 2) when the PXD is in PICC Mode, tests defined in [6.2](#) shall be applied.

In automatic mode alternation, the PXD may be forced into the required mode.

7 Test of ISO/IEC 14443-2 parameters

7.1 PCD tests

All the PCD tests described below will be done in the operating volumes as defined by the PCD manufacturer for each supported PICC class.

All PCD tests of ISO/IEC 14443-2 parameters shall be performed using Reference PICCs 1, 2 and 3 and optionally other Reference PICCs corresponding to the optional PICC classes supported by the PCD, with the relevant parameters and Test PCD assembly as defined in [Table 12](#).

Table 12 — PICC classes parameters

PICC class	Reference PICC	$H_{\min}$ test			$H_{\max}$ test		Test PCD assembly
		V_{load}	$R2_{\min}$	$R2_{\max}$	$R2_{\min}$	$R2_{\max}$	
1	1	4,5 V	647 Ω	791 Ω	76 Ω	94 Ω	Test PCD assembly 1
2	2	4,5 V	1 030 Ω	1 260 Ω	112 Ω	138 Ω	Test PCD assembly 1
3	3	4,5 V	1 080 Ω	1 320 Ω	117 Ω	143 Ω	Test PCD assembly 1
4	4	4,5 V	990 Ω	1 210 Ω	99 Ω	121 Ω	Test PCD assembly 2
5	5	4,5 V	960 Ω	1 170 Ω	103 Ω	127 Ω	Test PCD assembly 2
6	6	4,5 V	700 Ω	900 Ω	117 Ω	143 Ω	Test PCD assembly 2

The PCD should be tested with a V_{load} of 6 V for Reference PICC 1 to ensure interoperability with PICCs compliant with the V_{load} requirement of ISO/IEC 10373-6:2016.

7.1.1 PCD field strength

7.1.1.1 Purpose

This test measures the field strength produced by a PCD in its operating volume. The maximum and minimum field strength values to be used with each Reference PICC are given in ISO/IEC 14443-2:2020, Table 1.

NOTE The test takes account of PICC loading of the PCD.

7.1.1.2 Procedure

7.1.1.2.1 Procedure for $H_{\max}$ test

- Tune the Reference PICC to 19 MHz as described in [5.5.2.4](#) steps a) to g).
- Calibrate the Test PCD assembly to produce the $H_{\max}$ operating condition on the calibration coil.
- Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'b' and adjust R2 to obtain a DC voltage of 3 V measured at CON3. Alternatively, jumper J1 may be set to position 'c' and the applied voltage on CON2 is adjusted to obtain a DC voltage of 3 V at CON3. In both cases, the operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.

WARNING — R2 value should be between $R2_{\min}$ and $R2_{\max}$ as defined in $H_{\max}$ test columns in [Table 12](#). Check this range at least once before using the alternative method.

- d) Position the Reference PICC within the defined operating volume of the PCD under test. The DC voltage at CON3 shall not exceed 3 V.

WARNING — If the PCD field is not continuously emitted, the DC voltage measurement shall be done when the PCD field is present.

7.1.1.2.2 Procedure for $H_{\min}$ test

- a) Tune the Reference PICC to 13,56 MHz as described in [5.5.2.4](#).
- b) Place the Reference PICC into the DUT position on the Test PCD assembly producing the $H_{\min}$ operating condition on the calibration coil. Check that the jumper J1 is set to position 'b' and that a DC voltage of V_{load} as defined in [Table 12](#) is measured at CON3. Alternatively, the jumper J1 may be set to position 'c' and the voltage on CON2 is adjusted to obtain a DC voltage of V_{load} as defined in [Table 12](#) at CON3. In both cases, the operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.

WARNING — R2 value should be between $R2_{\min}$ and $R2_{\max}$ as defined in $H_{\min}$ test columns in [Table 12](#). Check this range at least once before using the alternative method.

- c) Position the Reference PICC within the defined operating volume of the PCD under test. The DC voltage at CON3 shall exceed V_{load} as defined in [Table 12](#).

WARNING — If the PCD field is not continuously emitted, the DC voltage measurement shall be done when the PCD field is present.

- d) For Reference PICC 1 repeat:
- 1) step b) with a DC voltage V_{load} of 6 V measured at CON3 instead of V_{load} as defined in [Table 12](#), and
 - 2) step c), where the DC voltage at CON3 shall exceed 5,3 V [corresponding to $H_{\min} - 0,2 \text{ A/m (rms)}$], instead of V_{load} as defined in [Table 12](#).

7.1.1.3 Test report

The test report shall confirm the operating volume in which the DC voltage measured at CON3 for R2 or variable load resistor adjusted to $H_{\min}$ and $H_{\max}$ field strength fulfills the requirements defined in step d) of [7.1.1.2.1](#) and in step c) and step d) of [7.1.1.2.2](#).

7.1.2 Void

PCD field strength supporting operation with PICC Class 1, which was defined in former editions of this document, is no longer present.

7.1.3 Void

Power transfer PCD to PICC, which was defined in former editions of this document, is no longer present.

7.1.4 Modulation index m and waveform

7.1.4.1 Purpose

This test is used to determine the index of modulation of the PCD field as well as the rise and fall times and the overshoot values as defined in ISO/IEC 14443-2 for all supported PCD to PICC bit rates.

7.1.4.2 Procedure

- a) Position the calibration coil at an arbitrary position in the defined operating volume and display the induced coil voltage on a suitable oscilloscope. Determine the modulation index m and waveform characteristics using the analysis tool defined in [Annex E](#).
- b) Tune the Reference PICC to 16,5 MHz as described in [5.5.2.4](#) steps a) to g) and switch the jumper J1 to position 'c'.
- c) Switch the jumper J2 to position 'a' or to position 'b' according to the tested PCD to PICC bit rate and place the Reference PICC at a particular position in the PCD operating volume.
- d) Apply and adjust a DC voltage at CON2 to obtain a DC voltage at CON3 of V_{load} as defined in [Table 12](#). If a DC voltage of V_{load} cannot be reached at the selected position, the maximum achievable voltage should be used for the test.
- e) If the unmodulated voltage on CON4, measured with a suitable oscilloscope (requirements see [5.2](#)) is below 1 V (peak-to-peak), use an alternative pick up coil to determine the waveform characteristic. This alternative pick up coil should have a "figure of 8" shape with 15 mm radius positioned farthest away from the Reference PICC to minimize coupling and as close as possible to the PCD antenna to maximize induced voltage.
- f) Determine the modulation index m and waveform characteristic from the voltage at CON4 or at the alternative pick up coil using the analysis tool defined in [Annex E](#).
- g) Repeat steps c) to f) for various positions within the operating volume and all supported PCD to PICC bit rates.

NOTE 1 The selected position of the calibration coil within the operating volume is not expected to affect the results.

NOTE 2 The Reference PICC load does not represent the worst case loading effect of a PICC. Higher loading effects may be achieved with resonance frequencies closer to carrier frequency (e.g. 15 MHz or 13,56 MHz).

7.1.4.3 Test report

The test report shall give the measured modulation index m of the PCD field, the rise and fall times and overshoot values, within the defined operating volume in unloaded and loaded conditions.

7.1.5 Phase stability test

7.1.5.1 Purpose

The purpose of this test is to determine whether the PCD provides f_c with a phase drift within the limit defined in ISO/IEC 14443-2.

7.1.5.2 Test procedure

- a) Tune the Reference PICC 1 to 13,56 MHz as described in [5.5.2.4](#).
- b) Place the Reference PICC 1 at an arbitrary position in the PCD operating volume, set jumper J1 to position 'b' and adjust R2 to obtain a voltage of V_{load} (see [Table 12](#)) at CON3. Alternatively, jumper J1 may be set to position 'c' and the applied voltage on CON2 is adjusted to obtain a voltage of V_{load} at CON3.
- c) Record the signal of the pick up coil for a time period of at least 25 ms.
- d) Compute the maximum phase drift from the instantaneous phase using the PCD phase stability analysis tool defined in [Annex M](#). Check if the maximum phase drift of the instantaneous phase is smaller than the limit specified in ISO/IEC 14443-2:2020, 8.2.5.2.

7.1.5.3 Test report

The test report shall contain the maximum phase drift of the PCD.

The used test conditions shall be mentioned in the test report.

7.1.6 Load modulation reception for PICC to PCD bit rates of $f_c/128$, $f_c/64$, $f_c/32$ and $f_c/16$

7.1.6.1 Purpose

This test is used to verify that a PCD correctly detects the load modulation of a PICC which conforms to ISO/IEC 14443-2 for PICC to PCD bit rates of $f_c/128$, $f_c/64$, $f_c/32$ and $f_c/16$, if supported.

In order to limit the testing time, only the highest PICC to PCD bit rate corresponding to every supported subcarrier f_s shall be tested.

NOTE In future revisions of ISO/IEC 10373-6, it is intended to extend this test to cover also PICC to PCD bit rates of $f_c/8$, $f_c/4$ and $f_c/2$.

7.1.6.2 General description

For the load modulation reception test the Active Reference PICC uses the principle of active load modulation to modify the field generated by the PCD.

The active load modulation signal of the Active Reference PICC shall be strictly synchronous to the PCD generated field. The pick up coil voltage on CON4, an alternative pick up coil (see 7.1.4.2, step e)), the main coil current on CON5 or any other mean may be used to synchronize the Active Reference PICC active load modulation signal generating device to the PCD RF field. It is recommended to perform synchronization during time periods when neither the PCD nor the Active Reference PICC modulates the RF field. During the Active Reference PICC response, the Active Reference PICC phase reference shall not vary more than 3° from the $\emptyset_{LM, INIT}$ value when it was synchronized; if synchronization is done much before the Active Reference PICC response, care shall be taken to limit the possible phase drift until the start of the Active Reference PICC response.

The active load modulation signal shall be generated such that the load modulation signal envelope observed at the load modulation test circuit of Figure 2 has a sinusoidal shape without phase jumps.

7.1.6.3 Precondition test

Perform the following steps to verify the synchronous functionality of the Active Reference PICC:

- Place the Active Reference PICC in the DUT position of the Test PCD assembly.
- Calibrate the Test PCD assembly to produce any field strength operating condition in the range of $[H_{min}, H_{max}]$ on the calibration coil.
- Adjust the load of the Active Reference PICC to the equivalent load defined for the Reference PICC (with V_{load} DC voltage at Reference PICC CON3 as defined in Table 12 as setup at H_{min}) having the same antenna class by applying a constant carrier signal to connector CON1, adjusting first its phase in order to achieve destructive interference and then its amplitude. The operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary. Note the Active Reference PICC CON3 DC voltage corresponding to the field condition.
- Send a command with the Test PCD assembly.
- The Active Reference PICC shall respond strictly synchronously i.e., with a theoretical $\emptyset_{LM, INTER}$ of 0° and a constant $\emptyset_{LM, INIT}$ between multiple responses. The Active Reference PICC shall respond with a 256 byte frame at a PICC to PCD bit rate of $f_c/128$.

- f) Display the whole Active Reference PICC response of both, calibration coil and load modulation test circuit, including at least 200 carrier periods before the first and 20 carrier periods after the last modulation of the Active Reference PICC on the signal acquiring device and store the sampled data of calibration coil and load modulation test circuit in separate files for analysis by the PICC amplitude and phase drift analysis tool defined in [Annex N](#).
- g) Repeat steps d) to f) 24 times.

The precondition test is PASS when the Active Reference PICC response $\varnothing_{LM, INTER}$ is less than $\pm 3^\circ$ and its $\varnothing_{LM, INIT}$ maximum variation is less than $\pm 3^\circ$ over 24 responses.

7.1.6.4 Test conditions

7.1.6.4.1 General

This test shall be done at ambient, minimum and maximum temperatures. If minimum and maximum temperatures are not provided in PCD test conditions, load modulation reception test shall be performed only at ambient temperature.

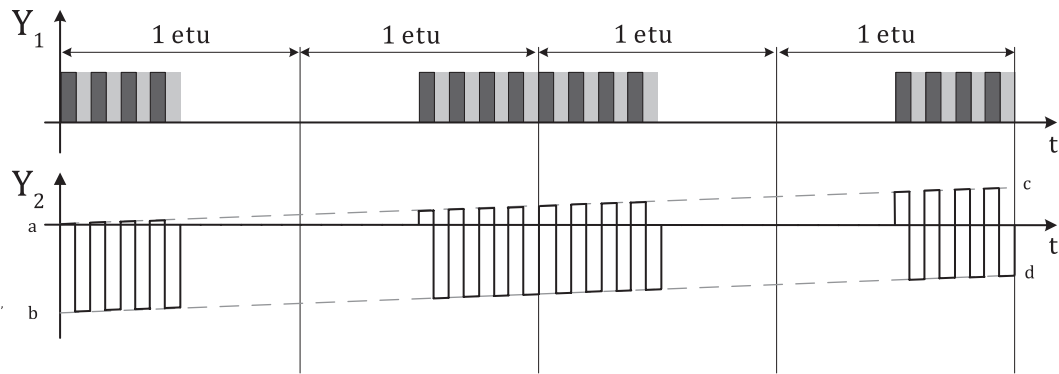
Test conditions are communication signal interface and PICC to PCD bit rate dependent defined and are described in the following two subclauses. [Figure 8](#) to [Figure 17](#) illustrate the test conditions.

- 1) The top plot shows the Active Reference PICC carrier signal:
 - a) Active Reference PICC carrier transmission, equivalent to state MS1, is shown as a black colored bar,
 - b) inverse Active Reference PICC carrier transmission, equivalent to state MS2, is shown as grey colored bar, and
 - c) no Active Reference PICC carrier transmission, equivalent to state US, is shown in white color.
- 2) The bottom plot shows the phase signal also including the interstate phase drift (grey dashed line) over time.

7.1.6.4.2 Test conditions for Type A for a PICC to PCD bit rate of $f_c/128$

Four phase drift conditions are defined within limits defined in ISO/IEC 14443-2.

- 1) Phase drift condition A1: Constant interstate phase drift of $\varnothing_{LM, INTER, PCD}$ over the complete Active Reference PICC response, active load modulation transmission during state MS1 and active load modulation transmission with the inverse phase of MS1 during state MS2. For an example see [Figure 8](#).

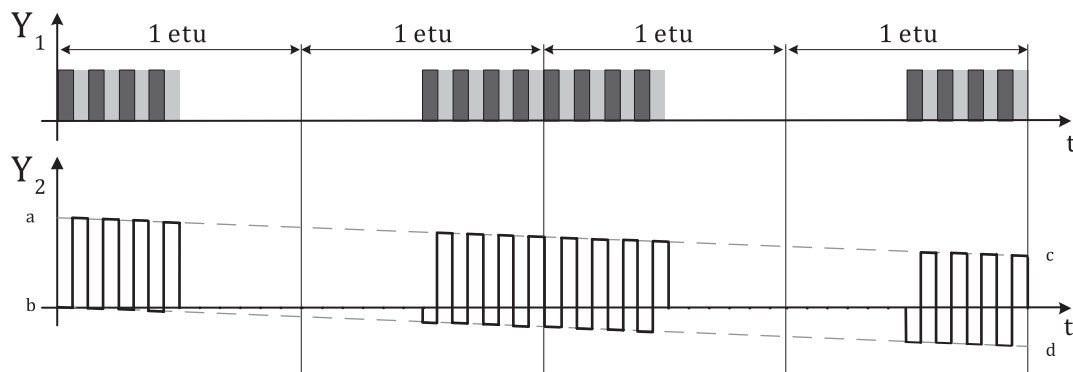
**Key**

Y_1 amplitude
 Y_2 phase (degree)

a $\emptyset_{LM, INIT}$
 b $\emptyset_{LM, INIT} - 180^\circ$
 c $\emptyset_{LM, INIT} + \emptyset_{LM, INTER, PCD}$
 d $\emptyset_{LM, INIT} - 180^\circ + \emptyset_{LM, INTER, PCD}$

Figure 8 — Example of phase drift condition A1 for Type A at a PICC to PCD bit rate of $f_c/128$

- 2) Phase drift condition A2: Constant interstate phase drift of $-\emptyset_{LM, INTER, PCD}$ over the complete Active Reference PICC response, active load modulation transmission during state MS1 and active load modulation transmission with the inverse phase of MS1 during state MS2. For an example see [Figure 9](#).

**Key**

Y_1 amplitude
 Y_2 phase (degree)

a $\emptyset_{LM, INIT} + 180^\circ$
 b $\emptyset_{LM, INIT}$
 c $\emptyset_{LM, INIT} + 180^\circ - \emptyset_{LM, INTER, PCD}$
 d $\emptyset_{LM, INIT} - \emptyset_{LM, INTER, PCD}$

Figure 9 — Example of phase drift condition A2 for Type A at PICC to PCD bit rate of $f_c/128$

- 3) Phase drift condition A3: Constant interstate phase drift of $\emptyset_{LM, INTER, PCD}$ during sequence D and E defined in ISO/IEC 14443-2:2020, 8.2.6.1. For an example see [Figure 10](#).
- a) Active load modulation transmission during MS1 and active load modulation transmission with the inverse phase of MS1 during state MS2.
- b) If sequence D directly follows sequence E, the constant interstate phase drift shall be $\emptyset_{LM, INTER, PCD}$ over both sequences.

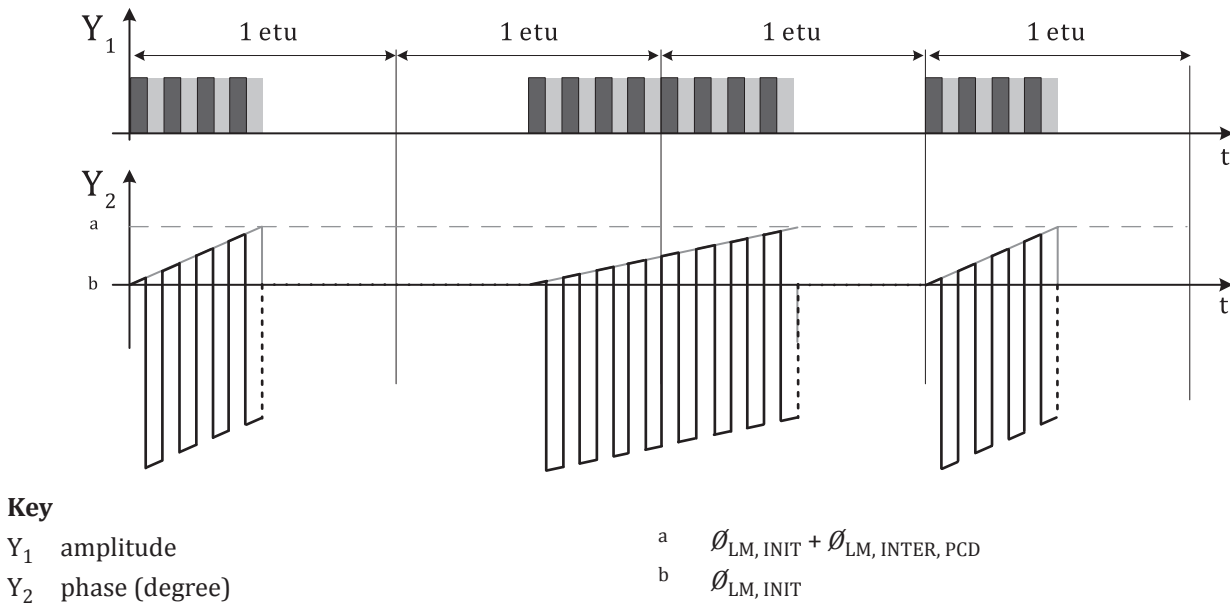


Figure 10 — Example of phase drift condition A3 for Type A at PICC to PCD bit rate of $f_c/128$

- 4) Phase drift condition A4: Constant interstate phase drift of $-\varnothing_{LM, INTER, PCD}$ during sequence D and E defined in ISO/IEC 14443-2:2020, 8.2.6.1. For an example see [Figure 11](#).
- a) Active load modulation transmission during MS1 and active load modulation transmission with the inverse phase of MS1 during state MS2.
- b) If sequence D directly follows sequence E, the constant interstate phase drift shall be $-\varnothing_{LM, INTER, PCD}$ over both sequences.

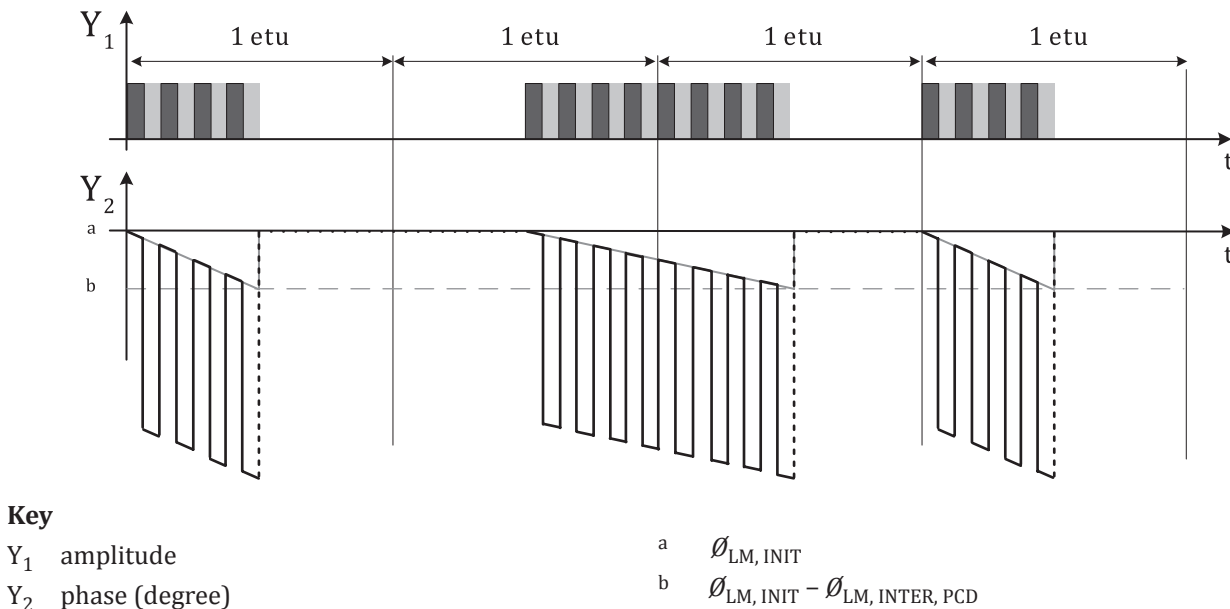


Figure 11 — Example of phase drift condition A4 for Type A at PICC to PCD bit rate of $f_c/128$

All of these phase drift conditions shall be tested at:

- $V_{LMA, min, PCD}$ and $V_{LMA, max, PCD}$
- 24 different $\varnothing_{LM, INIT}$ in steps of 15° .

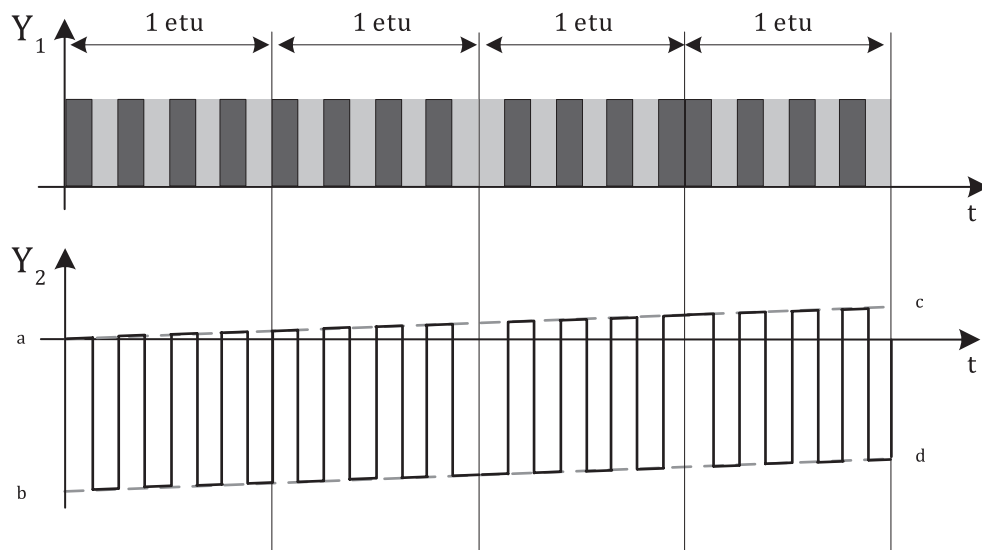
This results in 192 tests per Active Reference PICC.

NOTE Further $\emptyset_{LM, INIT}$ phases may be tested.

7.1.6.4.3 Test conditions for Type B for a PICC to PCD bit rate of $f_c/128$ and for Type A and Type B for optional PICC to PCD bit rates of $f_c/64$, $f_c/32$ and $f_c/16$

Two phase drift conditions are defined within limits defined in ISO/IEC 14443-2.

- 1) Phase drift condition B1: Constant interstate phase drift of $\emptyset_{LM, INTER, PCD}$ over the complete Active Reference PICC response, active load modulation transmission during state MS1 and active load modulation transmission with the inverse phase of MS1 during state MS2. For an example see [Figure 12](#).



Key

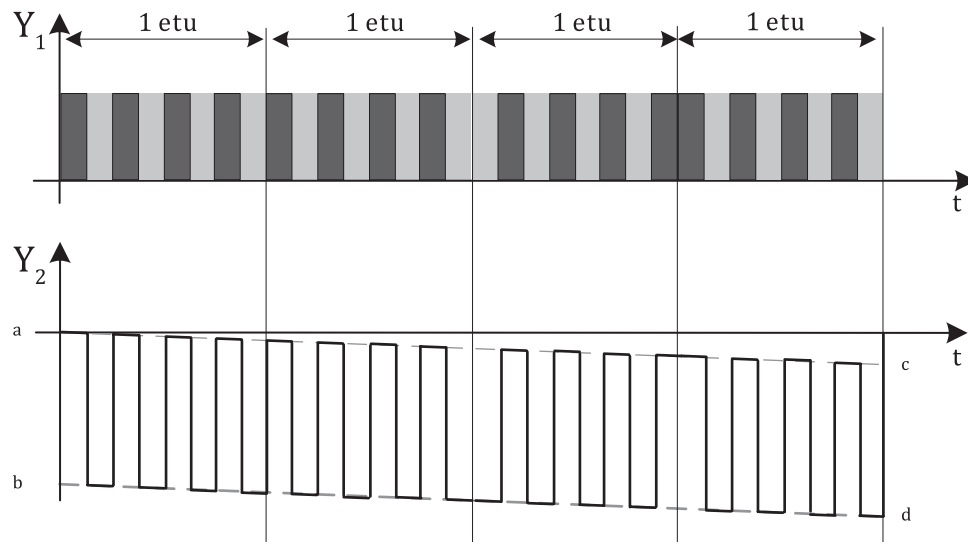
Y_1 amplitude

Y_2 phase (degree)

- a $\emptyset_{LM, INIT}$
- b $\emptyset_{LM, INIT} - 180^\circ$
- c $\emptyset_{LM, INIT} + \emptyset_{LM, INTER, PCD}$
- d $\emptyset_{LM, INIT} - 180^\circ + \emptyset_{LM, INTER, PCD}$

Figure 12 — Example of phase drift condition B1 at PICC to PCD a bit rate of $f_c/64$

- 2) Phase drift condition B2: Constant interstate phase drift of $-\emptyset_{LM, INTER, PCD}$ over the complete Active Reference PICC response, active load modulation transmission during state MS1 and active load modulation transmission with the inverse phase of MS1 during state MS2. For an example see [Figure 13](#).



Key

Y_1 amplitude

Y_2 phase (degree)

a $\emptyset_{LM, INIT}$

b $\emptyset_{LM, INIT} - 180^\circ$

c $\emptyset_{LM, INIT} - \emptyset_{LM, INTER, PCD}$

d $\emptyset_{LM, INIT} - 180^\circ - \emptyset_{LM, INTER, PCD}$

Figure 13 — Example of phase drift condition B2 at PICC to PCD a bit rate of $f_c/64$

All of these phase drift conditions shall be tested at:

- $V_{LMA, min, PCD}$ and $V_{LMA, max, PCD}$
- 24 different $\emptyset_{LM, INIT}$ in steps of 15° .

This results in 96 tests per each combination of PICC to PCD bit rate, communication signal interface and Active Reference PICC.

NOTE Further $\emptyset_{LM, INIT}$ phases may be tested.

7.1.6.5 Test procedure 1

The PCD shall operate under the conditions defined in 7.1.6.4 after the selection of that PICC to PCD bit rate. The PCD shall correctly react to a received PICC response at the selected PICC to PCD bit rate.

- a) Place the Active Reference PICC in the DUT position of the Test PCD assembly.
- b) Calibrate the Test PCD assembly to produce H_{min} in accordance with the Active Reference PICC class.
- c) Adjust the load of the Active Reference PICC to the equivalent load defined for the Reference PICC (with V_{load} DC voltage at Reference PICC CON3 as defined in Table 12 as setup at H_{min}) having the same antenna class by applying a constant carrier signal to connector CON1, adjusting first its phase in order to achieve destructive interference and then its amplitude. The operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary. Note the Active Reference PICC CON3 DC voltage corresponding to the field condition.
- d) Adjust the Active Reference PICC input signal at CON1 to get $V_{LMA, min, PCD}$ associated with the noted field strength and PICC class as specified in ISO/IEC 14443-2.

NOTE The V_{LMA} is measured as described in 7.2.1.

- e) Select an applicable phase drift condition defined in 7.1.6.4.

- f) Produce a response at a PICC to PCD bit rate of $f_c/128$ and record the initial phase $\emptyset_{LM, INIT}$ using the PICC amplitude and phase drift analysis tool of [Annex N](#).
- g) Place the Active Reference PICC in a position in the PCD operating volume with the same field strength condition as setup in step c) by measuring CON3 DC voltage. If this field strength condition cannot be achieved, measure the maximum field strength which can be achieved with a Reference PICC (with V_{load} DC voltage at Reference PICC CON3 as defined in [Table 11](#)) having the same antenna class then redo the procedure steps a), b) and d) using this maximum achievable field strength in steps b) and d).
- h) The PCD shall correctly detect the Active Reference PICC response.
- i) Repeat step h) at least for all mandatory $\emptyset_{LM, INIT}$ values defined in [7.1.6.4](#).
- j) Repeat steps h) and i) for all applicable phase drift conditions defined in [7.1.6.4](#).
- k) Repeat steps a) and d) to j) for the highest PICC to PCD bit rate corresponding to every supported subcarrier f_s .
- l) Repeat steps a) and d) to k) at least for all mandatory PCD V_{LMA} values defined in [7.1.6.4](#).
- m) Repeat steps a), b) and d) to l) at least for all field strength conditions defined in [Table 5](#).

Any tested position where the load modulation reception test is FAIL, shall be considered out of the operating volume.

7.1.6.6 Test procedure 2

- a) Place the Active Reference PICC in the DUT position of the Test PCD assembly.
- b) Calibrate the Test PCD assembly to produce H_{min} in accordance with the Active Reference PICC class.
- c) Minimize the load of the Active Reference PICC by applying no constant carrier signal to connector CON1. The operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary. Note the Active Reference PICC CON3 DC voltage corresponding to the field condition.
- d) Adjust the Active Reference PICC input signal at CON1 to produce $f_c - f_s$ and $f_c + f_s$ sidebands amplitudes of $V_{LMA, min, PCD}$ associated with H_{min} and PICC class as specified in ISO/IEC 14443-2.
- e) Select phase drift condition A1 or B1 defined in [7.1.6.4](#), depending on the PICC communication signal interface and the PICC to PCD bit rate.
- f) Produce a response and record the initial phase $\emptyset_{LM, INIT}$ using the PICC amplitude and phase drift analysis tool of [Annex N](#).
- g) Place the Active Reference PICC in a position in the PCD operating volume with the same field strength condition as setup in step c) by measuring CON3 DC voltage.
- h) The PCD shall correctly detect the Active Reference PICC response.
- i) Repeat step h) at least for all mandatory $\emptyset_{LM, INIT}$ values defined in [7.1.6.4](#).
- j) With $f_c + f_s$ sideband amplitude of PCD V_{LMA} as adjusted in step d), repeat steps h) and i) for $f_c - f_s$ sideband amplitude increased by 2,0 dB, 4,0 dB, 6,0 dB, 8,0 dB and 10,0 dB.
- k) With $f_c - f_s$ sideband amplitude of PCD V_{LMA} as adjusted in step d), repeat steps h) and i) for $f_c + f_s$ sideband amplitude increased by 2,0 dB, 4,0 dB, 6,0 dB, 8,0 dB and 10,0 dB.
- l) Repeat steps h) to k) for the highest supported PICC to PCD bit rate corresponding to every subcarrier f_s .

Any tested position where the load modulation reception test is FAIL, shall be considered out of the operating volume.

7.1.6.7 Test report

The test report shall confirm the intended operation at the mandatory PICC to PCD bit rate of $f_c/128$ for Test procedure 1 and Test procedure 2. For PCDs supporting one or more of the optional PICC to PCD bit rates the test report shall confirm the intended operation at the supported PICC to PCD bit rates tested for Test procedure 1 and Test procedure 2.

The used test conditions shall be mentioned in the test report.

7.1.7 Load modulation reception for PICC to PCD bit rates of $f_c/8$, $f_c/4$ and $f_c/2$

7.1.7.1 Purpose

This test is used to verify that a PCD correctly detects the load modulation of a PICC which conforms to ISO/IEC 14443-2 for PICC to PCD bit rates of $f_c/8$, $f_c/4$ and $f_c/2$, if supported.

NOTE In future revisions of ISO/IEC 10373-6 a test similar to [7.1.6](#) can be defined also for these PICC to PCD bit rates.

7.1.7.2 Procedure

- a) Tune the Reference PICC to 13,56 MHz as described in [5.5.2.4](#) and switch the jumper J1 to position 'c' and the jumper J2 to position 'b'.
- b) Place the Reference PICC at a particular position in the PCD operating volume.
- c) Apply and adjust a DC voltage at CON2 to obtain a DC voltage at connector CON3 of V_{load} as defined in [Table 3](#).
- d) Increase the modulation signal amplitude at CON1 to produce responses until the PCD detects at least 10 of them consecutively.
- e) Place the Reference PICC in the DUT position on the Test PCD assembly.
- f) Adjust the Test PCD assembly to produce a field strength H which gives the same voltage at CON3 and note the corresponding field strength by reading the calibration coil voltage.
- g) Measure the Reference PICC load modulation amplitude V_{LMA} as described in [7.2.1](#) and compare it with $V_{LMA, min, PCD}$ associated with the noted field strength. This measured V_{LMA} defines the PCD sensitivity criterion in order to compare with $V_{LMA, min, PCD}$ to perform these test measurements.
- h) Repeat steps b) to g) for various positions within the operating volume for PICC to PCD bit rates of $f_c/8$, $f_c/4$ and $f_c/2$, if supported.
- i) Repeat steps a) to h) with Reference PICC tuned to resonance frequency 15 MHz.

Any position in which the PCD sensitivity is above $V_{LMA, min, PCD}$ shall be considered out of the operating volume.

The test coverage may be expanded by using additional resonance frequencies below 13,56 MHz such as 12 MHz and 10 MHz.

The PCD sensitivity should be below $V_{LMA, min, PCD}$ to ensure good reception of the load modulation.

NOTE This test does not check that the PCD reception is independent of the phase of the load modulation. Consequently, it cannot guarantee the correct reception of any PICC compliant with ISO/IEC 14443-2.

7.1.7.3 Test report

The test report shall give the PCD load modulation sensitivity for the tested positions.

7.1.8 PCD EMD immunity test

7.1.8.1 Purpose

The purpose of this test is to determine whether the PCD is insensitive to any load modulation amplitude below $V_{E, PCD}$ for all supported PICC to PCD bit rates.

7.1.8.2 Procedure

- Tune the Reference PICC to 13,56 MHz as described in 5.5.2.4 and switch the jumper J1 to position 'c'.
- Switch the jumper J2 to position 'a' or to position 'b' according to the tested PICC to PCD bit rate and place the Reference PICC at a designated position in the PCD operating volume.
- Apply and adjust a DC voltage at CON2 to obtain a DC voltage at CON3 of V_{load} as defined in Table 12.
- Send the test pattern as shown in Figure 14. The test pattern is a valid standard frame including one single byte (01011101)b. The initial load modulation amplitude V_{EMD} of the test pattern shall be sufficiently low so that the PCD detects the PICC answer sent in step e).
- Immediately after this test pattern, applying no gap, send the appropriate PICC answer to the PCD command with a PICC V_{LMA} , measured as defined in 7.2.1, of a value higher, e.g. twice, than the minimum value for the applied field strength H .
- Increase V_{EMD} by adjusting the voltage at CON1 until the PCD does no longer detect the answer correctly. This may be determined by monitoring the next PCD command following the PICC answer; see Figure 14.
- Place the Reference PICC into the DUT position on the Test PCD assembly.
- Adjust the Test PCD assembly to produce a field strength H which gives the same voltage at CON3 and note the corresponding field strength by reading the calibration coil voltage.
- Derive the current value of V_{EMD} on the Reference PICC by applying the power versus time measurement as described in 5.7.2.
- Compare this measured V_{EMD} value with $V_{E, PCD}$.
- Repeat steps b) to j) for other designated positions within the operating volume.
- Repeat steps b) to k) for all supported PICC to PCD bit rates.

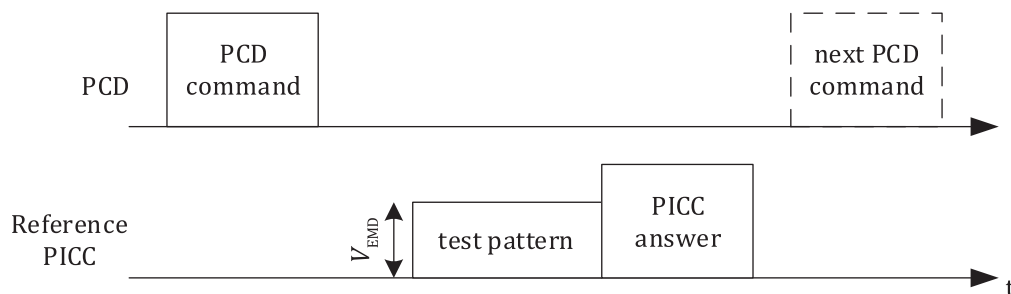


Figure 14 — PCD immunity test (common for Type A and Type B)

7.1.8.3 Test report

The test report shall state whether the PCD was insensitive to any load modulation amplitude below $V_{E, PCD}$ for all supported PICC to PCD bit rates.

7.1.9 Procedures for PCD supporting optional PLI_{ATQ} or PLI_{CID} handling

7.1.9.1 Scope

These tests apply only to PCDs which support PLI_{ATQ} or PLI_{CID} handling.

If the PCD supports optional PLI_{ATQ} or PLI_{CID} handling, the additional procedures specified in 7.1.9.2, 7.1.9.3, 7.1.9.4 and H.5 shall be used to verify that, for every power level used by the PCD:

- a) the PCD complies with the field strength requirements specified in ISO/IEC 14443-2:2020/Amd 1, ISO/IEC 14443-3:2018/Amd 1 and ISO/IEC 14443-4:2018/Amd 1;
- b) the PCD complies with modulation index and waveform requirements specified in ISO/IEC 14443-2;
- c) the PCD complies with load modulation reception requirements specified in ISO/IEC 14443-2;
- d) the PCD complies with EMD immunity requirements specified in ISO/IEC 14443-2.

7.1.9.2 Modulation index and waveform

The steps c) to g) of the procedure specified in 7.1.4.2 shall be repeated for every power level between minimum and maximum power level obtained by PLI_{ATQ} or PLI_{CID} .

For each power level, the test report shall be as specified in 7.1.4.3.

7.1.9.3 Load modulation reception

The procedures specified in 7.1.6.5 and 7.1.6.6 shall be repeated for every power level between minimum and maximum power level obtained by PLI_{ATQ} or PLI_{CID} .

For each power level, the test report shall be as specified in 7.1.6.7.

7.1.9.4 PCD EMD immunity test

The steps b) to l) of the procedure specified in 7.1.8.2 shall be repeated for every power level between minimum and maximum power level obtained by PLI_{ATQ} or PLI_{CID} .

For each power level, the test report shall be as specified in 7.1.8.3. 

7.2 PICC tests

7.2.1 PICC transmission

7.2.1.1 Purpose

-  The purpose of this test is to verify that the load modulation amplitude V_{LMA} of the PICC and the phase parameters $\phi_{LM, INTER}$ and $\phi_{LM, INTRA}$ of the PICC conform to ISO/IEC 14443-2 for all mandatory and supported optional PICC to PCD bit rates within the operating field range $[H_{min}$ respectively H_{LP} if the PICC supports PLI_{ATQ} or PLI_{CID} , $H_{max}]$. 

7.2.1.2 Conditions

This test shall be done at ambient, minimum and maximum temperatures. If minimum and maximum temperatures are not provided in PICC test conditions, the PICC transmission test shall be performed only at ambient temperature.

7.2.1.3 Procedure

Step 1:

The load modulation test circuit of [Figure 2](#) and the Test PCD assembly of [Figure 3](#) defined for the PICC class (see ISO/IEC 14443-2:2020, 8.2.2.2) are used. If the PICC does not claim to meet the requirements of one particular PICC class as specified in ISO/IEC 14443-1, then use the Test PCD assembly 1.

Adjust the RF power delivered by the signal generator to the Test PCD antenna to the required field strength as measured by the calibration coil. Connect the output of the load modulation test circuit of [Figure 2](#) to a signal acquiring device. The 10 Ω potentiometer P1 shall be trimmed to minimize the residual carrier. This signal shall be at least 40 dB lower than the signal obtained by shorting one sense coil. Additionally connect the output of the calibration coil (see [Figure 1](#) and [Figure 3](#)) to the same signal acquiring device as the load modulation test circuit.

Step 2:

The PICC under test shall be placed in the DUT position (see [Figure 3](#)). If the PICC meets the requirements of one particular class as specified in ISO/IEC 14443-1, then its antenna shall be located within the zone defined for its PICC class centered in sense coil a. If the PICC does not claim to meet the requirements of one particular class as specified in ISO/IEC 14443-1, then its antenna shall be located within the external rectangle defined for “Class 1” centered in sense coil a. The RF drive into the Test PCD antenna shall be re-adjusted to the required field strength.

For each PICC to PCD bit rate supported by the PICC, the Test PCD shall put the PICC in the PROTOCOL state. An I-block shall be sent by the Test PCD to obtain a response from the PICC of at least the length defined in [Table 13](#) for that PICC to PCD bit rate (TEST_COMMAND4 and TEST_RESPONSE4 fit this purpose). If this frame length is not supported by the PICC, its maximum supported frame length shall be used.

Table 13 — PICC transmission minimum frame length definition

PICC to PCD bit rate	Minimum frame length [bytes]
$f_c/128$	128
$f_c/64$	256
$f_c/32$	512
$f_c/16$	1024
$f_c/8$	2048
$f_c/4$	4096
$f_c/2$	4096

NOTE These minimum frame lengths stem from the memory size of the signal acquiring device and can be increased in the future.

Display the whole PICC response of both, calibration coil and load modulation test circuit, including at least 200 carrier periods before the first and 20 carrier periods after the last modulation of the PICC on the signal acquiring device and store the sampled data of calibration coil and load modulation test circuit in separate files for analysis by computer programs as defined in [Annex F](#) and [Annex N](#).

Load modulation amplitude computation:

Fourier transform with a Bartlett window exactly six subcarrier cycles of the sampled modulation waveform using suitable computer software (as the one given in [Annex F](#)). Use a discrete Fourier transformation with a scaling such that a pure sinusoidal signal results in its peak magnitude. In order to minimize transient effects, avoid analyzing a subcarrier cycle immediately following a non-modulating period or a phase shift of the subcarrier. The discrete Fourier transformation shall be done at the sidebands frequencies generated by the PICC under test, i.e. $f_c + f_s$ and $f_c - f_s$.

Amplitude and phase drift computation:

Use the PICC amplitude and phase drift analysis tool defined in [Annex N](#).

This test procedure shall be repeated 5 times. The test apparatus shall generate the carrier frequency f_c as defined in ISO/IEC 14443-2:2020, 6.2:

- 1) once at the lower limit of the allowed range,
- 2) 3 times in the middle of the allowed range and
- 3) once at the upper limit of the allowed range.

Before each repetition the test apparatus shall perform a field reset of at least 5 ms.

7.2.1.4 Test report

The test report shall state:

- 1) Compliancy of the PICC load modulation amplitude V_{LMA} with the requirements defined in ISO/IEC 14443-2:
 - a) For PICC to PCD bit rates of $f_c/128$, $f_c/64$, $f_c/32$ and $f_c/16$, if supported, the resulting peak amplitudes of the upper and lower sidebands at $f_c + f_s$ and $f_c - f_s$ shall be above $V_{LMA, min, PICC}$ as defined in ISO/IEC 14443-2:2020, 8.2.2.2.
 - b) For PICC to PCD bit rates of $f_c/8$, $f_c/4$ and $f_c/2$, if supported, the average value resulting from the peak amplitudes of the upper and lower sidebands at $f_c + f_s$ and $f_c - f_s$ shall be above $V_{LMA, min, PICC}$ as defined in ISO/IEC 14443-2:2020, 8.2.2.2.
 - c) For all PICC to PCD bit rates, the average value resulting from the peak amplitudes of the upper and lower sidebands at $f_c + f_s$ and $f_c - f_s$ shall be below $V_{LMA, max, PICC}$ as defined in ISO/IEC 14443-2:2020, 8.2.2.2.
- 2) Compliancy of the amplitude parameter $V_{|MS1-US|}$ of the PICC with the requirements defined ISO/IEC 14443-2:2020, 8.2.2.2 and phase parameters $\emptyset_{LM, INTRA}$ and $\emptyset_{LM, INTER}$ of the PICC with the requirements defined ISO/IEC 14443-2:2020, 8.2.2.3 for all mandatory and supported optional PICC to PCD bit rates.
- 3) Based on the state information retrieved in [N.9.1](#), compliancy of the following parameters of the PICC:
 - a) For Type A PICC responses using a bit rate of $f_c/128$, the duration of an etu, the number of subcarrier periods per etu, whether 50 % of an etu are modulated with the subcarrier, and the start of communication shall comply with ISO/IEC 14443-2.
 - b) For Type A PICC responses using a bit rate higher than $f_c/128$, if supported, the duration of an etu, the bit level encoding, and the start of communication shall comply with ISO/IEC 14443-2.
 - c) For Type B PICC responses, the bit level encoding, TR1, SOF, character encoding, EGT and EOF shall comply with ISO/IEC 14443-3:2018.

Furthermore, the test report shall

- 1) give the measured peak amplitudes of the upper and lower sidebands at $f_c + f_s$ and $f_c - f_s$ and the applied fields and modulations,
- 2) give the measured phase characteristics, and
- 3) confirm the intended operation at the mandatory PICC to PCD bit rate of $f_c/128$ and all supported optional PICC to PCD bit rates.

The used test conditions shall be mentioned in the test report.

7.2.2 PICC EMD level and low EMD time test

7.2.2.1 Purpose

- A1** The purpose of this test is to determine that the PICC does not generate an electromagnetic disturbance amplitude V_{EMD} higher than $V_{E, PICC}$ during $t_{E, PICC}$ with the exceptions defined in ISO/IEC 14443-2 within the operating field range [H_{min} respectively H_{LP} if the PICC supports PLI_{ATQ} or PLI_{CID} , H_{max}] as specified in ISO/IEC 14443-2 for all supported PICC to PCD bit rates.

NOTE 1 The low EMD time $t_{E, PICC}$ is a function of FDT/TR0 as defined in ISO/IEC 14443-3:2018, 8.2.

NOTE 2 The EMD limit $V_{E, PICC}$ is a function of the field strength.

A1

7.2.2.2 Noise requirements

In order to ensure a high dynamic range and sufficient sensitivity to EMD, the noise floor precondition test defined in [5.7.3](#) shall be performed before this test.

7.2.2.3 Test commands

The PICC EMD test shall be performed for ISO/IEC 14443-3 commands. Depending on the PICC application, additional higher layer commands shall be included in the test plan.

7.2.2.4 Procedure

This test shall be done at least applying H_{min} and H_{max} . Using the Test PCD assembly, perform the following steps.

- a) Adjust the RF power delivered by the signal generator to the Test PCD antenna to the required field strength as measured by the calibration coil.
- b) Place the PICC under test into the DUT position. The RF drive into the Test PCD antenna shall be readjusted to the required field strength if necessary.
- c) Reset the PICC by switching the RF field off and on; then if necessary send a transition of sequence commands to put the PICC into the Test Initial State, (see [G.3.3.2.2](#) for PICC Type A and [G.4.4.2.2](#) for PICC Type B).
- d) Send the command to be tested.
- e) Record the sense coil's signal for a time period of at least 200 μs before the start of PICC subcarrier generation. Additionally, record at least 50 μs after the first detected subcarrier in order to determine precisely the position of the PICC answer.

- f) Determine the value of $t_{E, \text{PICC}}$ from the acquired signal: if the PCD modulation is present on the trace then measure the time between the last rising edge of PCD modulation and the start of PICC subcarrier generation and calculate $t_{E, \text{PICC}}$ with the formula given in ISO/IEC 14443-3:2018, 8.2; if the PCD modulation is not present on the trace then $t_{E, \text{PICC}}$ equals its maximum value defined in ISO/IEC 14443-3:2018, 8.2.
- g) Compute the signal power at the frequencies $f_c + f_s$ and $f_c - f_s$ as a function of time as defined in 5.7.2.
- h) Compute the maximum signal out of the two results obtained in g).
- i) Determine the time t_{START} corresponding to half of the amplitude of the maximum signal obtained in h) during the rising edge of PICC transmission. Check if the amplitude of the maximum signal obtained in h) during the time period $[t_{\text{START}} - t_{E, \text{PICC}}; t_{\text{START}} - 1/f_s]$ complies with the requirements defined in ISO/IEC 14443-2.
- j) Repeat steps d) to i) for the next test command.
- k) Repeat steps d) to j) for all supported PICC to PCD bit rates.

7.2.2.5 Test report

The test report shall state whether the PICC EMD level during $t_{E, \text{PICC}}$ complies with the requirements defined in ISO/IEC 14443-2 for all supported PICC to PCD bit rates.

Furthermore the test report shall give the measured maximum electromagnetic disturbance levels of the upper and lower sidebands at $f_c + f_s$ and $f_c - f_s$ during $t_{E, \text{PICC}}$. A graph showing EMD levels during $t_{E, \text{PICC}}$ should be incorporated in the report in case the test fails.

7.2.3 PICC reception

7.2.3.1 Purpose

- A1 The purpose of this test is to verify the ability of the PICC to receive the PCD commands within the operating field range [$H_{\min}$ respectively H_{LP} if the PICC supports PLI_{ATQ} or PLI_{CID} , $H_{\max}$] as specified in ISO/IEC 14443-2 for all supported PCD to PICC bit rates. A1

7.2.3.2 General conditions

The test conditions shall be checked using the analysis tool defined in Annex E with the PICC under test in the DUT position. If at least one parameter is not within the tolerances defined in 4.3, the test conditions shall be readjusted.

The test PCD assembly may use a pre-equalization method and/or an impedance matching network different from those specified in A.2 to achieve some of the test conditions defined in Table 14, Table 15, Table 16 and Table 17.

For a frame size higher than 256 bytes, a frame with error correction as defined in ISO/IEC 14443-4 should be used.