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Telecommunications and information exchange between systems — Unmanned aircraft area network (UAAN)

Part 2: Physical and data link protocols for shared communication

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Telecommunications and information exchange between systems — Unmanned aircraft area network (UAAN) —

Part 2: Physical and data link protocols for shared communication

Télécommunications et échange d'information entre systèmes — Réseau de zone de drones (Unmanned aircraft area network - UAAN) —

Partie 2: Protocoles de liaison de données et physiques pour la communication partagée

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Foreword

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This document was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 6, *Telecommunications and information exchange between systems*.

A list of all parts in the ISO/IEC 4005 series can be found on the ISO and IEC websites.

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Introduction

Unmanned aircrafts (UAs) operating at low altitude will provide a variety of commercial services in the near future. UAs that provide these services are distributed in the airspace. In level II, many people operate their own UAs without the assignment of communication channels from a central control centre.

This document describes shared communication, which is a wireless distributed communication. Shared communication allows all units related with UAs to communicate with UAs when necessary. Shared communication can support communication between UAs, UAs and controllers, UAs and ground equipment, UAs and landing devices, and UAs and obstacle devices. A wireless distributed communication described by this document is intended to be used in licensed frequency bands.

The ISO/IEC 4005 series consists of the following four parts:

— ISO/IEC 4005-1: To support various services for UAs, it describes a wireless distributed communication model and the requirements that this model shall satisfy.

— ISO/IEC 4005-2 (this document): It describes communication in which all units involved in UA operations can broadcast or exchange information by sharing communication resources with each other.

— ISO/IEC 4005-3: It describes the control communication for the controller to control the UA.

— ISO/IEC 4005-4: It describes video communication for UAs to send video to a controller.

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Telecommunications and information exchange between systems — Unmanned aircraft area network (UAAN) —

Part 2: Physical and data link protocols for shared communication

1 Scope

This document describes communication protocols for the physical and data link layer of shared communication, which is a wireless distributed communication network for units related with UAs in level II.

Physical layer includes frame structure, encoding procedure, physical layer procedure and coexistence operations. Data link layer includes channel and slot, resource management, broadcast and exchange of data, synchronization, security, and interface with upper layer and other communication layers.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 4005-1, *Telecommunications and information exchange between systems — Unmanned aircraft area network (UAAN) — Part 1: Communication model and requirements*

ISO/IEC 4005-3:2023, *Telecommunications and information exchange between systems — Unmanned aircraft area network (UAAN) — Part 3: Physical and data link protocols for control communication*

ISO/IEC 4005-4:2023, *Telecommunications and information exchange between systems — Unmanned aircraft area network (UAAN) — Part 4: Physical and data link protocols for video communication*

ISO 21384-4, *Unmanned aircraft systems — Part 4: Vocabulary*

3 Terms and definitions

For the purposes of this document, the terms and definitions defined in ISO/IEC 4005-1, ISO 21384-4 and the following apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at https://www.electropedia.org/

3.1
broadcast slot
slot used to broadcast the information of a unit

3.2
data slot block
block in which multiple slots are grouped together for efficient resource allocation

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3.3
linearization slot
slot used to maintain the linearity of the power amplifier

3.4
response clearing
transmission of a tone signal in subslot 0 of the subslot set corresponding to the same slot of this frame, in order to respond to a talk packet received in a slot of the previous frame

3.5
slot block
block in which four slots are grouped together to perform efficient competition

3.6
super frame slot
slot with a frame period greater than one second

3.7
talk slot
slot used to exchange information with a specific counterpart

3.8
tone slot block
block in which multiple slots are grouped together to perform efficient competition

4 Abbreviated terms

CC	Control Communication
CRC	Cyclic Redundancy Check
CSCH	Control Subchannel
DL	Data Link
DLL	Data Link Layer
DQPSK	Differential Quadrature Phase Shift Keying
GF	Galois Field
LFSR	Linear Feedback Shift Register
PCCC	Parallel Concatenated Convolutional Code
PB	Parsing Block
PF	Parsing Field
PN	Pseudo Noise
SA	Source Address
SC	Shared Communication
SRRC	Square Root Raised Cosine
TX	Transmission
UTC	Coordinated Universal Time

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VC Video Communication

VSCH Video Subchannel

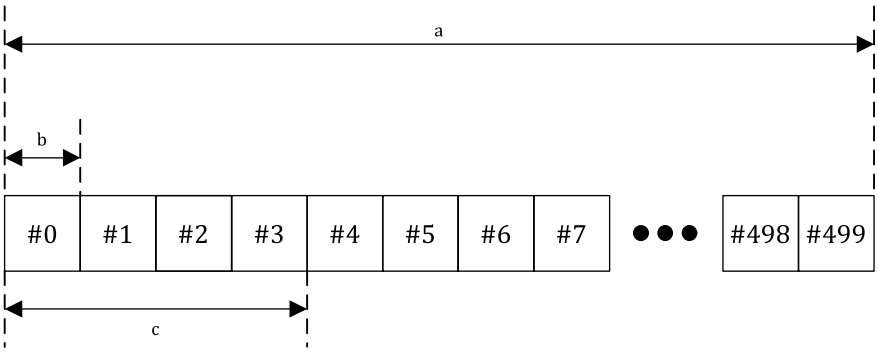
5 Physical layer

5.1 Physical layer frame structure

5.1.1 Data channel

5.1.1.1 Frame structure

The frame length of the data channel is 1 second and consists of 500 slots. The one slot time T_s is 2 ms. A data slot block has four slots. Therefore, there are 125 slot blocks in one frame, and the slot block is 8 ms in length as shown in Figure 1. The frame number changes from 0 to 59 in 1 min interval.



a 1 frame, T_f=1 second=500 T_s.

b 1 slot, T_s=2 ms.

c 1 slot block, T_{sb}=8 ms=4 T_s.

Figure 1 — Data channel frame structure

5.1.1.2 Slot block transmit time mask

The transmission time mask of a slot block is shown Figure 2.

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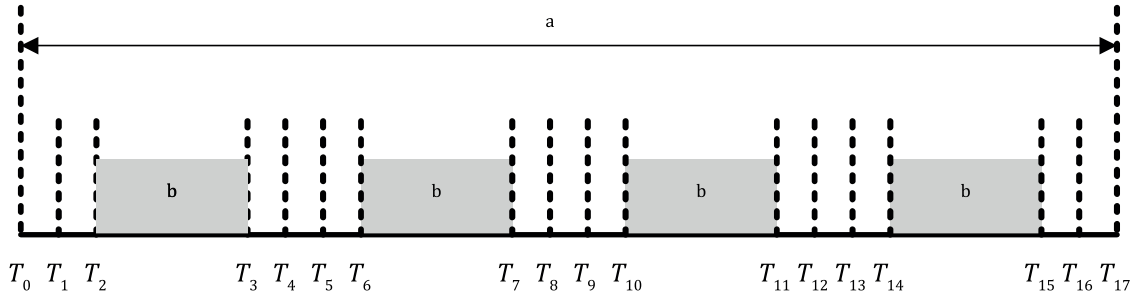

Key

T_0	0 µs
T_1, T_2, …, T_{17}	symbol time offsets from T_0
a	8 ms.
b	Modulated signal.

Figure 2 — Transmission time mask of a slot block

T_1, T_2, T_3, T_4, T_5, T_6, T_7, T_8, T_9, T_{10}, T_{11}, T_{12}, T_{13}, T_{14}, T_{15}, T_{16}, T_{17} are symbol offsets from T_0, and symbol time is 1/672000 second. Each value is as follows.

T_1 is 152, T_2 is 154, T_3 is 1449, T_4 is 1451, T_5 is 1456.5, T_6 is 1459.5, T_7 is 2754.5, T_8 is 2756.5, T_9 is 2763, T_{10} is 2765, T_{11} is 4060, T_{12} is 4062, T_{13} is 4068.0, T_{14} is 4070.5, T_{15} is 5365.5, T_{16} is 5366.5, T_{17} is 5376.

T_0 is 0 µs as the start time of the slot block. T_1, T_5, T_9 and T_{13} are offsets when the power amplifier is gated on, and unmodulated fine signals begin to be transmitted. T_2, T_6, T_{10}, and T_{14} are offsets at which modulation signal transmission starts. T_3, T_7, T_{11}, and T_{15} are offsets at which the transmission of the modulated signal ends. T_4, T_8, T_{12}, and T_{16} are offsets at which the power amplifier is gated off, and transmission of unmodulated fine signals is stopped. The transmit powers of T_1 to T_2, T_3 to T_4, T_5 to T_6, T_7 to T_8, T_9 to T_{10}, T_{11} to T_{12}, T_{13} toT_{14} and T_{15} to T_{16} shall be at least 50 dB less than the modulation signal transmit power.

5.1.2 Tone channel

5.1.2.1 Frame structure

5.1.2.1.1 General

There are two types of tone channels. One is a competition tone channel and the other is an information tone channel. The competition tone channel is used for resource allocation, occupation, and management operations. Information tone channels are used to convey simple information. In this document, the frame structure for the information tone channel is described, but whether and how to use the information tone channel is determined by the upper layer.

5.1.2.1.2 Information tone channel frame structure

The frame length of information tone channel is 1 sec and the number of slots per frame is 500. One slot is divided into 33 subslots, and the length T_{ss} of a subslot is 60 µs as shown in Figure 3. The information given to each subslot is determined by the upper layer. SS_x means the x-th subslot (see Annex G).

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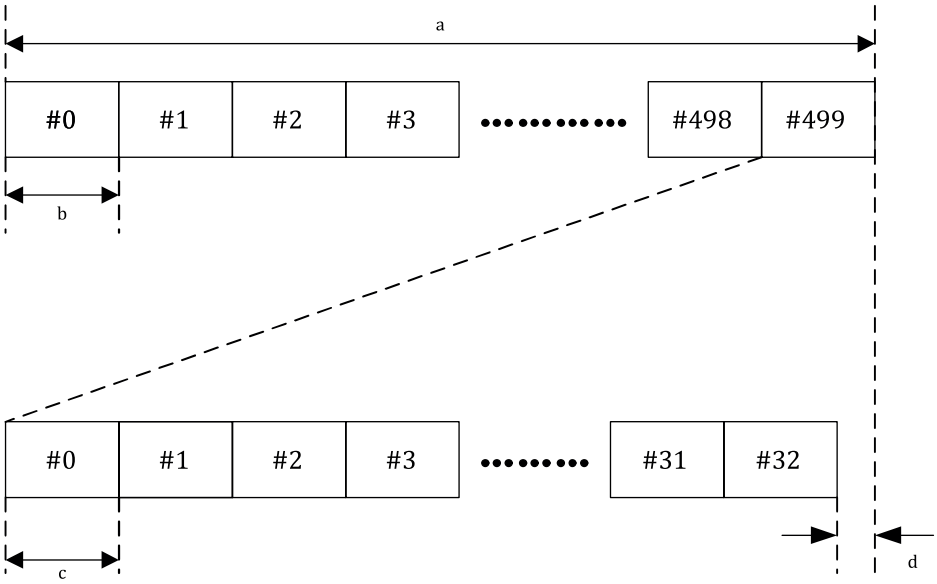

a 1 frame, T_f = 1 second = 500 T_s.

b 1 slot, T_s = 2 ms.

c T_{ss} = 60 µs.

d 20 µs.

Figure 3 — Frame structure of information tone channel

5.1.2.1.3 Competition tone channel frame structure

The frame length of competition tone channel is 1 sec and the number of slots per frame is 500. Four tone slots constitute one slock block. Thus, there are 125 slot blocks in one second frame. There are a total of 132 subslots in one slot block. The length T_{ss} of the subslot is 60 µs. The 132 subslots are divided into four parts, as shown in Figure 4, according to each slot numbers.

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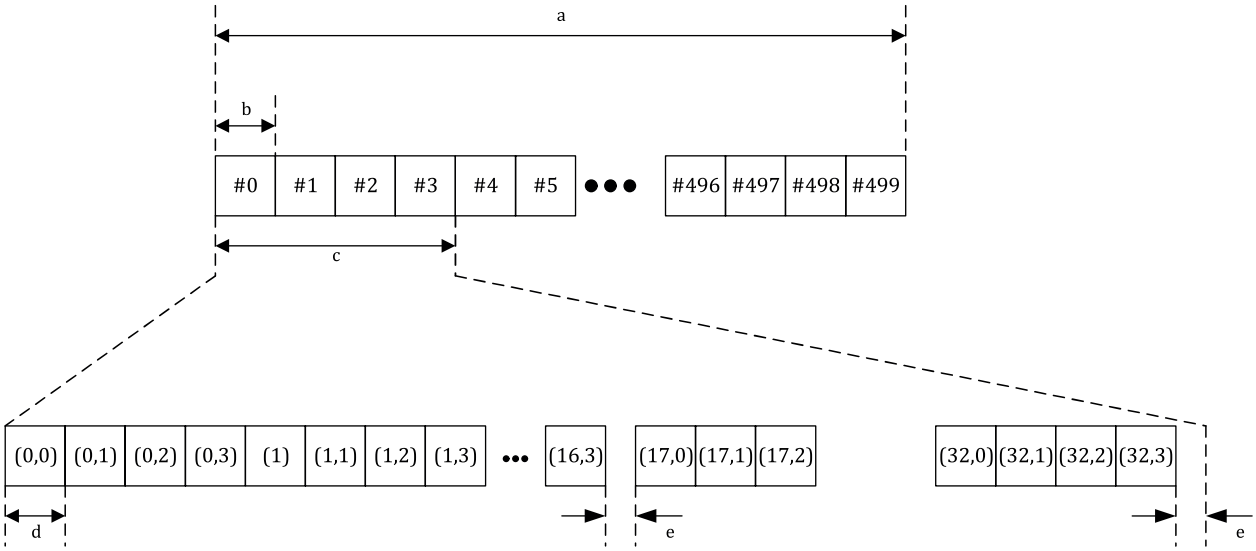

a 1 frame, T_f = 1 second = 500 T_s.

b 1 slot, T_s = 2 ms.

c 1 slot block, T_{sb} = 8 ms.

d T_{ss} = 60 µs.

e 40 µs.

Figure 4 — Frame structure of competition tone channel

The n-th slot block is composed of the following subslots.

— (0, 4n), (0, (4n + 1)), (0, (4n + 2)), (0, (4n + 3)), (1, 4n), (1, (4n + 1)), (1, (4n + 2)), (1, (4n + 3)),… , (32, 4n), (32, (4n + 1)), (32, (4n + 2)), (32, (4n + 3))

where (x, y) is the x-th subslot of the y-th subslot set. The 132 subslots constitute 4 subslot sets.

5.1.2.2 Subslot transmit time mask

Subslot transmission time mask is shown in Figure 5.

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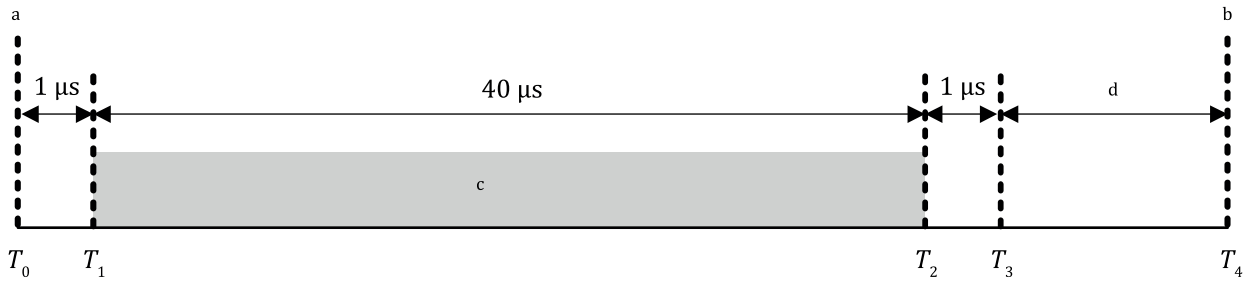

Key

T_1, T_2, T_3, and T_4 are time offsets from T_0

T_1 is 1 µs

T_2 is 41 µs

T_3 is 42 µs

T_4 is 60 µs

T_0 is the start time of the subslot, the power amplifier is gated on and the unmodulated fine signal starts to be transmitted

T_1 is the time at which transmission of the modulated signal begins

T_2 is the time at which transmission of the modulated signal is terminated

T_3 is the time when the power amplifier is gated off and the transmission of unmodulated fine signals is stopped

a Subslot start.

b Subslot end.

c Tone signal.

d Guard time.

Figure 5 — Subslot transmission time mask

The transmission power between T_0 and T_1 and between T_2 and T_3 shall be 50 dB less or less than the maximum transmission power of the modulated signal.

5.1.2.3 Subslot signal waveform

The modulation scheme of subslot signal is on-off keying. The subslot transmission signal is transmitted in the 40 µs interval from T_1 to T_2 in Figure 5. The waveform of the subslot transmission signal uses a raised cosine function. The subslot signal is generated by the following formula.

$$g(t;\alpha)=\frac{\cos(\pi\alpha(t-2T))}{1-(2\alpha(t-2T)/T)^2}\sin c\left(\frac{(t-2T)}{T}\right),\qquad 0\le t\le 4T \tag{1}$$

where

α is 0,75 as a roll-off factor;

T is 10 µs as a raised cosine period.

See Annex D.

5.2 Encoding procedure

The encoding follows the following procedure as shown in Figure 6. CRC encoding, turbo coding, rate matching, interleaving, modulation mapping, burst mapping, and pulse mapping are performed in this order.

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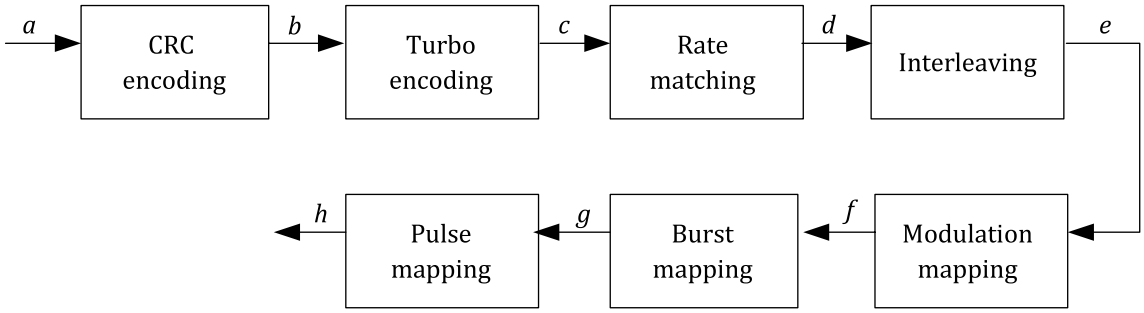

Figure 6 — Encoding procedure

The number of symbols according to each encoding stage is shown in Table 1.

Table 1 — Number of symbols at each encoding stage

Stage	Number of symbols
a	792 (binary)
b	816 (binary)
c	2460 (binary)
d	2432 (binary)
e	2432 (binary)
f	1216 (Complex)
g	1288 (Complex)
h	1295×*OS* (Complex)

5.2.1 CRC encoding

The input bits are defined as $a_0, a_1, a_2, a_3, \ldots, a_{A\text{-}1}$ and parity bits as $p_0, p_1, p_2, p_3, \ldots, p_{23}$ where, A represents the number of input sequences. Parity bits are generated through CRC generation polynomial as follows.

$$g_{\mathrm{CRC}}(D) = D^{24} + D^{22} + D^6 + D^5 + D + 1 \tag{2}$$

The encoding performed through the cyclic generator polynomials has a systematic form as follows. The resulting polynomial has zero remainder when it is divided by $g_{\mathrm{CRC}}(D)$ on GF(2).

$$a_0 D^{\mathrm{A}+23} + a_1 D^{\mathrm{A}+22} + \ldots + a_{A\text{-}1} D^{24} + p_0 D^{23} + p_1 D^{22} + \ldots + p_{22} D^1 + p_{23} \tag{3}$$

After CRC insertion, bits are represented by $b_0, b_1, b_2, b_3, \ldots, b_{B\text{-}1}$ (where $B = A + 24$), and the relationship between a_k and b_k is as follows.

$$b_k = \begin{matrix} a_k, & for\, k = 0,1,2,\cdots,A-1 \\ P_{k-A}, & for\, k = A, A+1, A+2, \cdots, A+23 \end{matrix} \tag{4}$$

5.2.2 Turbo encoding

The turbo encoder consists of Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one turbo coded internal interleaver. The coding rate of the turbo encoder is 1/3. The structure of the turbo encoder is shown in Figure 7. The PCCC transfer function is as follows:

$$G(D) = [1, g_1(D)/g_0(D)] \tag{5}$$

where $g_0(D) = 1+D^2+D^3$, $g_1(D) = 1+D+D^3$.

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When the input bits of the turbo encoder are encoded, the initial values of the shift registers of the 8-state constituent encoder shall all be zero.

For k = 0, 1, 2, …, K-1, the output value of the turbo encoder is expressed as follows:

$$c_{3k} = x_k$$

$$c_{3k+1} = z_k$$

$$c_{3k+2} = z'_k \tag{6}$$

Output bits of the first and second 8-state constituent encoders for turbo encoder input bits b_0, b_1, b_2, b_3, …, b_{B-1} are z_0, z_1, z_2, z_3, …, z_{B-1} and z'_0, z'_1, z'_2, z'_3, …, z'_{B-1}, and the output bits through the turbo code internal interleaver that is described in Annex A are represented by b'_0, b'_1, b'_2, b'_3, …, b'_{B-1} and these output bits are used as inputs for the second 8-state constituent encoder. The turbo code internal interleaver shall use Table A.1 in Annex A.

Trellis termination is performed by taking tail bits from shift register feedback after all information bits have been encoded. The generated tail bits are added after encoding of the information bits.

The first three tail bits are used for the first constituent encoder termination and not the second constituent encoder. The remaining three tail bits are used for the termination of the second constituent encoder and not the first constituent encoder.

The bits transmitted for trellis termination are determined as follows:

$$c_{3B} = x_B,\ c_{3B+3} = z_{B+1},\ c_{3B+6} = x'_B,\ c_{3B+9} = z'_{B+1}$$

$$c_{3B+1} = z_B,\ c_{3B+4} = x_{B+2},\ c_{3B+7} = z'_B,\ c_{3B+10} = x'_{B+2}$$

$$c_{3B+2} = x_{B+1},\ c_{3B+5} = z_{B+2},\ c_{3B+8} = x'_{B+1},\ c_{3B+11} = z'_{B+2} \tag{7}$$

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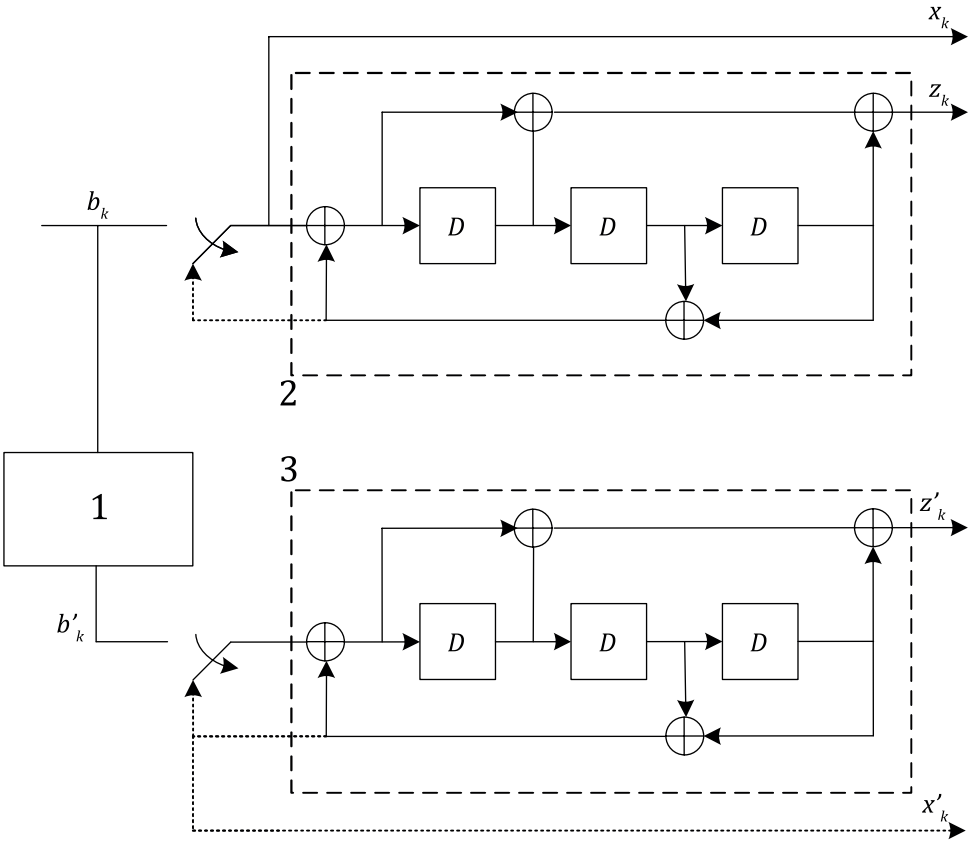

Key

1	turbo code internal interleaver
2	first constituent encoder
3	second constituent encoder
D	register
b_k	a k-th bit of turbo encoder input
b'_k	a k-th bit of turbo code internal interleaver output
x_k	a k-th systematic bit of turbo encoder output
z_k	a k-th bit of first constituent encoder output
x'_k	a k-th bit of second constituent encoder output for trellis termination
z'_k	a k-th bit of second constituent encoder output

Figure 7 — Turbo encoder structure

Input bit sequence of turbo code internal interleaver, b_0, b_1, b_2, b_3, ..., b_{B-1} and output bit sequence generated from turbo code internal interleaver, b'_0, b'_1, b'_2, b'_3, ..., b'_{B-1} have the following relationship.

$$b'_i = b_j \tag{8}$$

where the mapping between the output bit index i and the input bit index j shall follow Table A.1 in Annex A. Where j and i are as follows, and row and column numbers start at zero.

j = (number shown in table) − 1

$$i = (\text{row number in table})\times 16+(\text{column number in table}) \tag{9}$$

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5.2.3 Rate matching

Rate matching outputs d_0, d_1, d_2, d_3, ..., d_{D-1} by puncturing the input bits c_0, c_1, c_2, c_3, ..., c_{C-1}. The puncturing bit numbers are as follows.

— 43, 131, 217, 305, 391, 479, 565, 653, 739, 827, 913, 1001, 1087, 1175, 1261, 1349, 1435, 1523, 1609, 1697, 1783, 1871, 1957, 2045, 2131, 2219, 2305, 2393

5.2.4 Interleaving

The interleaver uses block interleaving with 38 rows and 64 columns.

$$e_m = d_n$$

$$m = (n \times 64)\%2432 + \lfloor n/38 \rfloor \tag{10}$$

where $\lfloor x \rfloor$ means the largest integer among integers less than or equal to x and $0 \le n \le 2431$.

5.2.5 Modulation mapping

Modulation mapping generates a complex symbol f_n from the input bit e_m, $0 \le n \le 2431$, $0 \le m \le 1215$. Two input bits are mapped to one complex number as shown in Table 2.

Table 2 — modulation mapping

$e_{2n}e_{2n+1}$	00	01	10	11
f_n	$exp(j/4\pi)$	$exp(j{\cdot}7/4\pi)$	$exp(j{\cdot}3/4\pi)$	$exp(j{\cdot}5/4\pi)$

5.2.6 Burst mapping

Output complex symbols $g_0, g_1, ..., g_{1287}$ are generated from the input complex symbols $f_0, f_1, ..., f_{1215}$.

$$g_n = \prod_{k=0}^{n} c(k) \tag{11}$$

where, $c(n)$ is shown in Table 3.

Table 3 — $c(n)$

n	$c(n)$	Number of symbols
0, 1	$TSS(n)$	2
2, ..., 37	$PTS1(n\text{-}2)$	36
38, ..., 443	$f_{n\text{-}38}$	406
444, ..., 459	$PTS2(n\text{-}444)$	16
460, ..., 865	$f_{n\text{-}54}$	406
866, ...,881	$PTS2(n\text{-}866)$	16
882, ...,1285	$f_{n\text{-}70}$	404
1286, 1287	$TSS(n\text{-}1286)$	2

where $TSS(n)$, $PTS1(n)$, and $PTS2(n)$ are shown in Table 4, Table 5 and Table 6 respectively.

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Table 4 — *TSS*(*n*)

TSS(0)	*TSS*(1)
$exp(j{\cdot}3/4\pi)$	$exp(j{\cdot}7/4\pi)$

Table 5 — *PTS1*(*n*)

n	*PTS*1(*n*)	*n*	*PTS*1(*n*)	*n*	*PTS*1(*n*)
0	$exp(j{\cdot}5/4\pi)$	12	$exp(j{\cdot}5/4\pi)$	24	$exp(j{\cdot}7/4\pi)$
1	$exp(j{\cdot}7/4\pi)$	13	$exp(j/4\pi)$	25	$exp(j{\cdot}5/4\pi)$
2	$exp(j{\cdot}7/4\pi)$	14	$exp(j/4\pi)$	26	$exp(j{\cdot}7/4\pi)$
3	$exp(j{\cdot}5/4\pi)$	15	$exp(j{\cdot}5/4\pi)$	27	$exp(j/4\pi)$
4	$exp(j/4\pi)$	16	$exp(j{\cdot}7/4\pi)$	28	$exp(j{\cdot}5/4\pi)$
5	$exp(j/4\pi)$	17	$exp(j/4\pi)$	29	$exp(j{\cdot}3/4\pi)$
6	$exp(j{\cdot}3/4\pi)$	18	$exp(j{\cdot}5/4\pi)$	30	$exp(j{\cdot}3/4\pi)$
7	$exp(j{\cdot}5/4\pi)$	19	$exp(j{\cdot}3/4\pi)$	31	$exp(j/4\pi)$
8	$exp(j{\cdot}3/4\pi)$	20	$exp(j{\cdot}7/4\pi)$	32	$exp(j/4\pi)$
9	$exp(j/4\pi)$	21	$exp(j/4\pi)$	33	$exp(j{\cdot}5/4\pi)$
10	$exp(j{\cdot}5/4\pi)$	22	$exp(j/4\pi)$	34	$exp(j{\cdot}3/4\pi)$
11	$exp(j{\cdot}5/4\pi)$	23	$exp(j{\cdot}3/4\pi)$	35	$exp(j{\cdot}7/4\pi)$

Table 6 — *PTS*2(*n*)

n	*PTS*2(*n*)	*n*	*PTS*2(*n*)	*n*	*PTS*2(*n*)
0	$exp(j/4\pi)$	6	$exp(j{\cdot}5/4\pi)$	12	$exp(j{\cdot}3/4\pi)$
1	$exp(j{\cdot}3/4\pi)$	7	$exp(j{\cdot}3/4\pi)$	13	$exp(j{\cdot}3/4\pi)$
2	$exp(j/4\pi)$	8	$exp(j{\cdot}5/4\pi)$	14	$exp(j/4\pi)$
3	$exp(j{\cdot}7/4\pi)$	9	$exp(j{\cdot}7/4\pi)$	15	$exp(j{\cdot}7/4\pi)$
4	$exp(j{\cdot}7/4\pi)$	10	$exp(j{\cdot}5/4\pi)$		
5	$exp(j{\cdot}3/4\pi)$	11	$exp(j{\cdot}7/4\pi)$		

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5.2.7 Pulse mapping

The complex symbol g_m is converted into a complex signal h_n where the oversampling ratio of the filter is OS times and depends on implementation. For $0 \le n < 1295 \times OS$, the complex signal is defined as follows.

$$h_n = w\left(\frac{nT_s}{OS}\right)\sum_{m=0}^{1287} p\left(\left(\frac{n}{OS} - m - 4\right)T_s\right)g_m \tag{12}$$

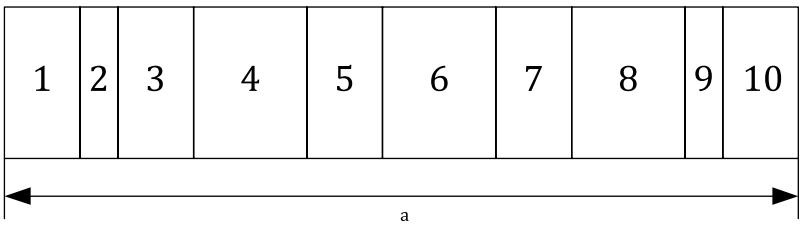
where symbol duration T_s is the 1/672000 second and pulse shape $p(t)$ is defined as SRRC function of roll-off factor 0,35 as follows.

$$p(t) = \frac{1}{1 + \frac{(1-\alpha)\pi}{4\alpha}} \cdot \frac{\cos\left(\frac{(1+\alpha)\pi t}{T_s}\right) + \frac{\sin((1-\alpha)\pi t / T_s)}{4\alpha t / T_s}}{1 - (4\alpha t / T_s)^2} \tag{13}$$

Here window function $w(t)$ to process tapering at signal start and end is introduced for good frequency characteristics reducing spurious emission. The $w(t)$ is defined as follows.

$$w(t) = \begin{cases} (1/2)(1 - \cos(\pi t / 2T_s)), & 0 \le t < 2T_s \\ 1, & 2T_s \le t < 1293T_s \\ (1/2)(1 - \cos\left(\frac{\pi}{2T_s}(t - 1295T_s)\right)), & 1293T_s \le t < 1295T_s \\ 0, & otherwise \end{cases} \tag{14}$$

The modulated signal is shown in Figure 8. D represents the modulation mapping output. Timing of modulated signal transmission is as described in 5.1.1.2 i.e. the modulated signals are transmitted in the time intervals of T_2 to T_3, T_6 to T_7, T_{10} to T_{11}, and T_{14} to T_{15} in Figure 2.



Key

1 filter delay, 4 symbols
2 *TLS* , 2 symbols
3 PTS_1, 36 symbols
4 data symbol, 406 symbols
5 PTS_2, 16 symbols
6 data symbol, 406 symbols
7 PTS_2, 16 symbols
8 data symbol, 404 symbols
9 *TLS* , 2 symbols
10 filter delay, 3 symbols
[a] Modulated signal, 1295 symbol.

Figure 8 — Modulated signal structure

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5.3 Physical layer procedure

5.3.1 Slot synchronization

The synchronization mode of the unit includes 'A sync', 'B sync' and 'C sync'.

— A sync is synchronization obtained from UTC.

— B sync is secondary synchronization acquired from the synchronization signal of the A sync unit.

— C sync is sync status within 20 seconds after sudden loss of sync in A or B sync mode.

A sync unit shall know the date, hour, minute, second, slot number.

The time error of A sync shall be within ±0,4 µs. The time error of B sync shall be within ±4 µs. The time error of C sync shall be within ±5 µs.

The frequency error of A sync shall be within ±0,1ppm. The frequency error of the B sync shall be within ±0,2ppm. The frequency error of the C sync shall be within ±0,3ppm.

5.3.2 Transmit power control

The upper layer can designate the transmit powers for specific slot blocks. All units have the same transmission power for the same slot block. Normal slot transmit power is PTXnormalSCH. The transmission power of the tone subslot is a value obtained by adding PTX_SCHTCH_differ to the transmission power of the related data slot block.

5.3.3 Measurements

5.3.3.1 General

The physical layer shall have the ability to measure the following parameters. It shall be possible to measure the tone subslot received signal power, the data slot received signal power, and the propagation delay time of the received data signal. The received power decision point shall be the receiving antenna connector.

5.3.3.2 Slot map

The slot map consists of 500 bit strings. The *n*-th bit indicates whether *n*-th data slot is usable or not. '1' means the slot is available, and '0' means the slot is not available. The physical layer shall dynamically update the slot map for every slot block interval.

The availability of the corresponding data slot is determined by receiving a signal of the slot clearing subslot in the tone subslot set mapped with the corresponding data slot. If the power of the slot clearing subslot signal is greater than PRXtoneCompeteThre, it is determined that the data slot mapped thereto is occupied.

5.4 Coexistence operation

If the hardware of shared communication described in this document and the hardware of control communication described in ISO/IEC 4005-3, and the hardware of video communication described in ISO/IEC 4005-4 are completely physically isolated and do not affect each other at all, it shall be allowed that they do not perform coexistence operations, which is implementation dependent. In general, the three communications affect each other, and in this case, the following coexistence operations shall be performed.

The TX operation of a shared slot includes the TX operation of the corresponding shared slot and the mapped tone subslot set. The TX operation of a control communication includes TX of the mapped tone

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subslot set and CSCH TX. The TX operation of video communication includes TX of the mapped tone subslot set and VSCH TX.

When a UA periodically broadcasts its information to a shared slot of a shared channel, a shared slot and a tone subslot set mapped to the shared slot generally require 1 slot and 4 slots, respectively, for TX operation. If the TX operation of the shared slot used for mandatory periodic broadcasting and the TX operation of the control channel overlap, the TX operation of the shared slot shall be performed.

The talk slot TX operation of a shared channel shall not overlap with the periodic broadcast slot TX operation of the conversation partner, and also the conversation partner's CSCH TX and the VSCH TX.

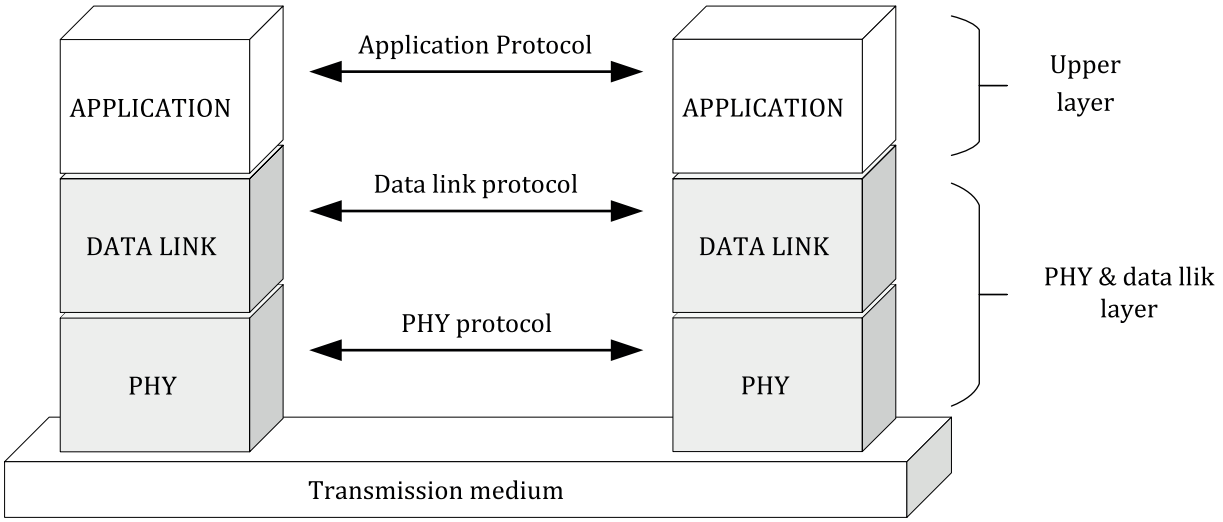
6 Data link layer

6.1 General

The data link layer describes the behaviour of units for broadcast links and unicast links. This document describes the allocation, occupation and return of data slots which are wireless communication resources.

Since this document uses a synchronous distributed communication, units allocate slot resources by themselves, occupy the allocated slot resources by themselves, and return slot resources by themselves. When occupying the allocated slot resource, collision check is continuously performed for the slot resource.

This data link describes only the basic functions of generating, maintaining, and terminating links. If necessary, additional functions for the link are implemented in the upper layer. The upper layer is mainly an application layer that provides services, as shown in Figure 9.



Key

PHY physical layer

Figure 9 — Protocol stack structure

Slots and channels are used in this document. There are data channel and tone channels, and one data channel and one tone channel work by mapping to each other.

The upper layer can flexibly design the frames and slots of the data channel, i.e. the length of the frame can be longer than 1 sec for certain slots or slots for a specific unit can be designated or transmission power of specific slots can be designated.

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