

Harmonized system of quality
assessment for electronic components

Film and hybrid integrated circuits —

Generic specification —
Section 1: Requirements for internal
visual inspection

Committees responsible for this British Standard

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- Federation of the Electronics Industry
- GAMBICA (BEAMA Ltd.)
- Ministry of Defence
- National Supervising Inspectorate
- Society of British Aerospace Companies Limited

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National foreword

This British Standard has been prepared under the direction of the Electronic Components Standards Policy Committee. It is identical with IEC 748-20-1:1994 (QC 760001) *Semiconductor devices — Integrated circuits — Part 20: Generic specification for film integrated circuits and hybrid film integrated circuits — Section 1: Requirements for internal visual examination*, published by the International Electrotechnical Commission (IEC), and is a harmonized specification in the IECQ system of quality assessment for electronic components.

IEC 748-20-1 was prepared by IEC Subcommittee 47A, Integrated circuits, of IEC Technical Committee No. 47, Semiconductor devices, and the United Kingdom participation in the drafting was provided by Subcommittee ECL/24/4, Film and hybrid integrated circuits, of Technical Committee ECL/24, Semiconductors.

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Summary of pages

This document comprises a front cover, an inside front cover, pages i to iv, pages 1 to 18 and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

1 Scope and object

1.1 Purpose

The purpose of these examinations is to check the internal materials, construction and workmanship of film and hybrid integrated circuits (F and HFICs).

These examinations will normally be used prior to tapping or encapsulation to detect and eliminate the F and HFICs with internal defects that could lead to device failure in normal application. Other acceptance criteria may be agreed upon with the purchaser or supplier.

1.2 Sequence of inspections

The order in which inspections are presented is not a required order of examination and may be varied at the discretion of the manufacturer. Any aspect which may be obscured by a subsequent assembly process shall be examined before that process.

1.3 Inspection apparatus

The apparatus for this test shall include optical equipment capable of the specified magnification(s) and any visual standard (gauges, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate fixtures shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.

1.4 Inspection environment

Under consideration.

1.5 Magnification

"High magnification" ($100\times$ to $200\times$) inspection is normally performed with a microscope perpendicular to the relevant surface with the device under illumination.

"Low magnification" ($10\times$ to $100\times$) inspection is normally performed with a monocular, a binocular or a stereomicroscope at an appropriate angle and illumination.

1.6 Definitions

For the purposes of this section of IEC 748-20, the following definitions apply.

1.6.1

active circuit area

all areas of functional circuit elements, operating metallization or any connected combinations thereof

1.6.2

multi-layer metallization (for conductors)

two or more layers of metal or any other material used for interconnections that are not isolated from each other

1.6.3

edge metallization

metallization that electrically connects different layers of metallization on or within a substrate at its edge

1.6.4

foreign material

any material not used in the manufacture of the microcircuit or any in-built material that is displaced from its original or intended position within the microcircuit package. Foreign material that appears opaque under those conditions of lighting and magnification used in routine visual inspection is considered as conductive

1.6.5

protective layer (passivation)

layer of insulating material that protects part or all of the substrate area, including metallization, but excluding connecting pads, for example glassivation, solder resist, etc.

1.6.6

isolating layer

layer used to isolate separate conductive or resistive levels

1.6.7

kerf

slit or cut made by a material-removing process (for example laser or abrasive trimming)

1.6.8

multilevel metallization (for conductors)

two or more levels of metal or any other material used for interconnections that are isolated from each other by a grown or deposited insulating material and interconnected for example by vias or edge metallization

1.6.9

bond pad area

that area of exposed metallization which is not covered by passivation

1.6.10

compound bond

bonding of one bond on top of another bond

1.6.11

through-hole metallization

metallization that electrically connects different levels of metallization on or within a substrate via a hole or holes

1.6.12

scratch

any tearing defect on the surface of a layer

1.6.13**cosmetic scratch**

shallow scratch which may extend completely across a layer and which does not expose or damage underlying layers, or laterally displace metallization beyond the edge of the conductor for example by mechanical deformation

1.6.14**void**

any defect in a layer not caused by a scratch where underlying material is visible

1.7 Interpretations

Reference herein to “that exhibits” is considered satisfied when the visual image or visual appearance of the device under examination indicates a specific condition is present.

This does not require confirmation by any other method of testing.

1.8 Alternative test methods

Visual examination requirements given below are not necessarily the only methods which can be used.

However, the manufacturer should satisfy the National Authorized Institution (NAI) that any alternative method will give equivalent assurance, otherwise the specified method is to be used.

2 Substrate and processes — Low magnification**2.1 Substrate**

No device shall be acceptable that shows the following:

- holes through the substrate, except through lead holes, used or unused component mounting holes, or alignment holes;
- any crack that exceeds 0,125 mm in length and point toward an operating portion of the circuit (see Figure 1);
- any chip out that reduces any active (metallized) circuit area (see Figure 2);
- any crack that comes closer than 0,025 mm to an operating portion of the circuit (see Figure 3);
- any substrate having attached portions of another substrate that exceed the substrate dimensions allowed by the assembly drawing (see Figure 4);
- any substrate having a section broken out around any substrate mounting hole greater than 25 % of the mounting hole circumference when designed for substrate to post attachment (see Figure 5);
- any crack that originates at an edge (see Figure 6).

2.2 Processes**2.2.1 Conductors**

No device shall be acceptable that shows the following:

- 1) metallization scratches (a scratch is any tearing effect, including probe marks, in the surface of the metallization);
 - scratch in the metallization excluding bonding pads that exposes the substrate or underlying dielectric anywhere along its length and leaves less than 50 % of the metal width undisturbed (see Figure 7);
 - scratch in multilayered metallization that exposes the underlying metal anywhere along its length and leaves less than 50 % of the top layer metal width undisturbed (see Figure 8);
 - scratch in the bonding pad or fillet area that exposes the underlying dielectric or substrate and reduces the metallization path width connecting the bond to the inter connecting metallization to less than 50 % of the narrowest entering interconnect metallization stripe width. If two or more strips enter a bonding pad, each shall be considered separately (see Figure 9);
- 2) metallization voids
 - void(s) in metallization except for wire or beam lead bonding pads that leaves less than 50 % of the metal width undisturbed (see Figure 7);
 - void(s) in the wire or beam lead bonding pad area that leaves an area less than twice the maximum allowable bond size undisturbed;
 - void(s) in the wire or beam lead bonding pad, including fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 % of the narrowest entering interconnect metallization strip width (see Figure 9).

NOTE If two or more strips enter a bonding pad, each should be considered separately.

- 3) metallization corrosion
 - any metallization corrosion (see Figure 10);
- 4) metallization adherence
 - any metallization lifting, peeling or blistering (see Figure 11);
- 5) metallization probing (criteria contained in 1) and 2) shall apply as limitations on probing damage);