

**Harmonized system of quality assessment
for electronic components**

**Semiconductor devices.
Integrated circuits.**

**Sectional specification for film
integrated circuits and hybrid
film integrated circuits:
capability approval**

Committees responsible for this British Standard

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- EEA (The Association of Electronics, Telecommunications and Business Equipment Industries)
- Electronic Components Industry Federation
- GAMBICA (BEAMA Ltd.)
- Ministry of Defence
- National Supervising Inspectorate
- Society of British Aerospace Companies Ltd.

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National foreword

This British Standard has been prepared under the direction of the Electronic Components Standards Policy Committee. It is identical with IEC Publication 748-22 : 1992 (QC 760200) *Semiconductor devices — Integrated circuits Part 22 : Sectional specification for film integrated circuits and hybrid film integrated circuits on the basis of the capability approval procedures*, published by the International Electrotechnical Commission (IEC) and is a harmonized specification within the IECQ system of quality assessment for electronic components.

Cross-references

The British Standard which implements the IECQ basic rules given in Publication QC 001002 is BS 9000 *General requirements for a system for electronic components of assessed quality Part 3 : 1991 Specification for national implementation of the IECQ system*.

International standard	Corresponding British Standard
IEC 63 : 1963	BS 2488 : 1966 <i>Schedule of preferred numbers for the resistance of resistors and the capacitance of capacitors for telecommunication equipment</i> (Technically equivalent)
IEC 68-1	BS 2011 <i>Environmental testing</i> Part 1.1 : 1989 <i>General and guidance</i> (Identical)
IEC 68-2	Part 2.1 : <i>Tests</i> (Most Parts are identical)
IEC 440 : 1973	BS 5694 : 1979 <i>Method for measurement of non-linearity in resistors</i>
IEC 747-1	BS 6493 <i>Semiconductor devices</i> Part 1 : 1984 <i>Discrete devices</i> Section 1.1 <i>General</i> (Identical)
IEC 748-20 : 1988 (QC 760000)	BS QC 760000 ¹⁾ : 1990 <i>Harmonized system of quality assessment for electronic components. Film and hybrid integrated circuits. Generic specification</i> (Identical)
IEC 748-21 : 1991	BS QC 760100 : 1991 <i>Harmonized system of quality assessment for electronic components. Semiconductor devices. Integrated circuits. Sectional specification for film and hybrid integrated circuits: qualification approval</i> (Identical)
IEC 748-22-1 : 1991	BS QC 760201 : 1992 <i>Harmonized system of quality assessment for electronic components. Semiconductor devices. Integrated circuits. Blank detail specification for film and hybrid integrated circuits: capability approval</i> (Identical)

The international text makes reference to 'IL': Inspection Levels and 'AQL': Acceptance Quality Levels. These quantities are specified in IEC 410 : 1973 which is technically equivalent to BS 6001 *Sampling procedure for inspection by attribute Part 1 : 1991 Specification for sampling plans indexed by acceptable quality level (AQL) for lot-by-lot inspection*.

Compliance with a British Standard does not of itself confer immunity from legal obligations.

¹⁾ This standard was erroneously published as BS QC 763000. An amendment to correct this has now been published.

SEMICONDUCTOR DEVICES

Integrated circuits

Part 22: Sectional specification for film integrated circuits and hybrid film integrated circuits on the basis of the capability approval procedures

1 Scope and object

1.1 Scope

This sectional specification applies to film integrated circuits and hybrid film integrated circuits manufactured as catalogue circuits or as custom-built circuits whose quality is assessed on the basis of the capability approval procedures.

1.2 Object

The object of this specification is to present preferred values for ratings and characteristics, to select from the generic specification the appropriate test and measuring methods, and to give general performance requirements to be used in detail specifications for film integrated circuits and hybrid film integrated circuits derived from this specification.

The concept of preferred values is directly applicable to catalogue circuits but does not necessarily apply to custom built circuits.

Test severities and requirements prescribed in detail specifications referring to this sectional specification shall be of equal or higher performance level, since lower performance levels are not permitted.

One or more blank detail specifications, referenced by an IEC number are associated with this specification. When completed as specified in subclause 2.3 of this specification, the blank detail specification forms a detail specification. Such detail specifications shall be used for the granting of capability approval to film integrated circuits and hybrid film integrated circuits according to the boundaries of capability identified by the manufacturer in his capability manual and maintenance of capability approval in accordance with the IEC system.

2 General, preferred characteristics, ratings and severities for environmental, including mechanical tests

2.1 Related documents

IEC 748-20/QC 760 000 (1988): *Semiconductor devices – Integrated circuits – Part 20: Generic specification for film integrated circuits and hybrid film integrated circuits.*

IEC 748-22-1/QC 760 201 (1991): *Semiconductor devices – Integrated circuits – Blank detail specification for film integrated circuits and hybrid film integrated circuits on the basis of the capability approval procedures (section 1).*

2.2 Preferred ratings and characteristics

Preferred values of voltages and currents are given in IEC Publication 747-1; for resistors and capacitors preferred values are given in IEC Publication 63; for custom-built circuits, any values and tolerances may be chosen.

The circuits covered by this specification are classified into climatic categories according to the general rules given in IEC Publication 68-1.

The severities for the cold and dry heat tests are the lower and upper category temperatures respectively. Because of the construction of some circuits, these temperatures will occur between two of the preferred temperatures given in IEC Publication 68-2. In this event, the nearest preferred temperature within the actual range of the circuit shall be chosen for this severity.

2.3 Information to be given in a detail specification

Detail specifications shall be derived from the relevant blank detail specification.

Detail specifications shall not specify severities inferior to those of the generic or sectional specification. When more severe requirements are included, they shall be listed in the detail specification and indicated in the test schedules, for example by an asterisk.

NOTE - The information given on dimensions, characteristics and ratings may, for convenience, be presented in tabular form.

The following information shall be given in each detail specification and the values quoted shall preferably be selected from those given in the appropriate subclause of this sectional specification.

Each detail specification shall state all the tests and measurements required for lot-by-lot and periodic inspections. This shall, as a minimum, include the relevant tests given in this specification with methods and severities.

Environmental tests (including mechanical), measurements, severities and end-point limits for periodic tests shall be included in the detail specification(s) for the Capability Qualifying Circuits (CQCs). They shall be in accordance with the applicable parts of the generic specification and this specification.

2.3.1 Outline drawing and dimensions

There shall be an illustration of the circuit as an aid to easy recognition and for comparison of the circuit with others. Dimensions and their associated tolerances, which affect interchangeability and mounting, shall be given in the detail specification. All dimensions shall be stated in millimetres.

Normally, numerical values shall be given for the length, width and height of the body, and the termination spacing or, for cylindrical types, the body diameter and the length and diameter of the terminations.

When necessary, for example when a detail specification covers more than one package, the dimensions and their associated tolerances shall be placed in a table below the drawing.

When the configuration is other than that described above, the detail specification shall state such dimensional information as will adequately describe the circuit.

2.3.2 *Mounting*

The detail specification shall prescribe the method of mounting to be applied for normal use and for the application of the vibration, bump and shock tests. The design of the circuit may be such that special mounting fixtures are required in its use. In this case, the detail specification shall prescribe the mounting fixtures and they shall be used in the application of the vibration, bump and shock tests.

2.3.3 *Severities for environmental, including mechanical tests*

The detail specification shall prescribe the appropriate method of testing and the appropriate severities selected from section 4 of the generic specification.

2.3.4 *Marking*

The detail specification shall prescribe the content of the marking on the circuit and on the primary package. Deviations from subclause 2.6 of the generic specification shall be specifically stated.

2.3.5 *Ordering information*

The detail specification shall prescribe that the following information is required when ordering circuits:

- 1) circuit type (e.g. hybrid thick film integrated circuit);
- 2) number of the detail specification with style reference and assessment level (if appropriate);
- 3) function of the circuit (if appropriate);
- 4) basic functional characteristics with tolerance (if appropriate).

2.3.6 *Additional information (not for inspection purposes)*

The detail specification may include information which is not normally required to be verified by the inspection procedure, such as circuit diagrams, curves, drawings and notes needed for clarification.

3 **Capability approval procedures**

See subclause 3.6 of the generic specification with the following details:

3.1 *Selection of capability qualifying circuits (CQCs)*

3.1.1 The CQCs for approval testing shall be taken from the following sources:

- 1) special circuits designed to qualify the design rules, processes and products and/or
- 2) circuits intended for shipment to customers.

Any or all of these CQCs in combination with process test vehicles shall be adequate to assess the complete design rules, material and manufacturing processes, including any subcontracted process.

Terminations of film elements and added components used for assessment shall be individually accessible for electrical measurement without influence from other circuit elements.

3.1.2 The CQCs shall be used to carry out the tests prescribed for capability approval and for periodic testing, and hence to demonstrate to the NSI that for limiting design layouts:

1) performance limits claimed for individual film element types are achieved;

2) environmental limits claimed for structures intended for shipment are met

and

3) the electrical function performances claimed in the capability manual and the detail specifications are met.

3.1.3 Circuits which have received qualification approval according to IEC Publication 748-21 may be counted as CQCs (provided the requirements of 3.1.1 have been met) for the purpose of capability approval, subject to NSI agreement on relevant structural similarity claims.

3.1.4 A manufacturer who has received capability approval is permitted to obtain a separate qualification approval for any individual circuit he makes, provided all appropriate testing in IEC Publication 748-21 has been completed successfully.

3.1.5 A manufacturer using customer circuits among those selected as CQCs may vary the types tested according to his production plan. In this case the CQCs need not necessarily assess all the claimed limits of his capability all of the time, but they shall be representative of those released during the current maintenance of approval period.

His CQC selection shall be made available to the NSI.

3.1.6 When production material divides into separate processes after a common process, e.g. encapsulation, the common process can be assessed by a single sample.

3.1.7 Where a manufacturer carries out screening tests on all circuits, as a normal production process, he may use screened CQCs for approval.

Where initial screening is not normally carried out or is an option, approval will be carried out on unscreened products.

3.2 *Structural similarity*

- 1) The CQCs shall be selected by the manufacturer's chief inspector and agreed by the NSI before commencing the approval programme.
- 2) Rules for structural similarity applicable to the grouping of completed circuits for electrical, dimensional and environmental (including mechanical) tests are given in appendix A of this specification.
- 3) These rules shall be used to establish the basis of selection for approval. They shall also be used to determine whether new circuits are within the existing approved capability or require its extension to enable their release.
- 4) Where CQCs are structurally similar for a test sequence, they may be grouped together to form the required numbers in the test tables. Each test sequence has its own structural similarity rules and criteria (see appendix A).

3.3 *Capability approval*

3.3.1 The procedures for capability approval are given in 3.6 of the generic specification.

The test tables for capability approval by CQCs and quality conformance inspection (lot-by-lot and periodic tests) collectively prescribe the minimum test programme on completed circuits.

The manufacturer may select which assessment level K, L or M he wishes to include, but a manufacturer with approved capability may only release products as follows:

Assessment level

K
L
M

Release assessment levels

K, L or M
L or M
M

NOTE - The suffix "N" is used if necessary to denote nonqualified components. See generic specification, subclause 3.6.2.3.

A manufacturer may upgrade the assessment level of his approval by following the procedures given in the generic specification and he may downgrade without further periodic testing until current test interval dates expire. In either case the NSI shall be notified.

Any additional test required for specific applications shall be given in the detail specification and be subject to agreement between the customer and manufacturer.

The post-test electrical limits for the relevant environmental tests shall be given in the detail specification.

3.3.2 *Release for delivery before completion of group B tests*

Due to the need for extended periods of lot collection from small quantity production batches, a manufacturer may, with the agreement of the customer, release products in advance of group B tests provided that the previous lot of identical circuits passed satisfactorily.

In this case, he shall indicate clearly on the relevant release documents that the circuits are released under subclause 3.3.2 of this specification and complete the tests within one month of despatch.

In the event of subsequent failure to meet environmental tests, all products which have been released in advance may be subject to recall or quarantine, dependent on the reason for failure.

3.3.3 *Capability approval (fixed sample size procedures)*

3.3.3.1 *Sampling*

The sample size and criteria of acceptability depend on the assessment level which is claimed and are detailed in table 2.

When additional groups are introduced into the test schedule, the number of circuits required for group "0" shall be increased by the same number as that required for the additional groups.

3.3.3.2 *Tests*

The tests in table 1 are intended to validate the design rules, materials, processes, piece parts and package range by testing all the CQCs and process test vehicles.

For each test group, different CQCs may be grouped together according to the structural similarity rules given in appendix A, to reach the required number of samples for that group.

The complete series of tests specified in table 1 is required for the approval of capability covered by the capability manual. The tests in each group shall be carried out in the given order.

The required portions of the sample shall be subjected to the tests of group "0" and then the total sample divided for the other groups.

Circuits found defective during the tests of group "0" shall not be used for the other groups.

"One defective" is counted when a CQC has not satisfied the whole or part of the tests of a group.

The approval is granted when the number of defectives does not exceed the specified number of permissible defectives for each group or sub-group and the total number of permissible defectives.

Table 1 - Test schedule for qualification approval

Sample sizes and acceptance criteria are detailed for each assessment level in table 2.

Subclause numbers refer to section 4 of the generic specification.

Subclause numbers, tests and test sequences	D or ND	Test conditions	Performance requirements
<i>Group 0</i> <i>Sub-group 01</i> 4.3.1 Precap visual examination	ND		
<i>Sub-group 02a</i> 4.3.2 External visual and marking examination	ND		
<i>Sub-group 02b</i> 4.3.3 Dimensions			
<i>Sub-group 03 (Note 7)</i> 4.5.16 Induced flammability (for information only)	D		
<i>Sub-group 04 (Note 1)</i> 4.5.9 Sealing	ND		
<i>Sub-group 05</i> 4.4.11 Major static and dynamic electrical characteristics at room temperature	ND		
<i>Sub-group 06</i> 4.4.11 Major static and dynamic electrical characteristics at extreme operating temperatures	ND		
<i>Group 1 Sequence (Notes 1 and 2)</i> Initial measurements 4.5.6 Vibration, swept frequency and 4.5.7 Acceleration, steady state or 4.5.5 Shock and 4.5.7 Acceleration, steady state Final measurements	D/ND	4.4.11: Sub-group 05 4.5.9: Sealing 4.4.11: Sub-group 05	

For notes, see next page.

Table 1 (continued)

Subclause numbers, tests and test sequences	D or ND	Test conditions	Performance requirements
<i>Group 2</i> Sequence Initial measurements 4.5.11 Resistance to soldering heat 4.5.15.2 Resistance to solvents (Note 7) 4.5.8 Change of temperature 4.5.3 Damp heat, steady state (Note 4) Final measurements	D	4.4.11: Sub-group 05 4.5.9: Sealing (Note 1) 4.4.11: Sub-group 05 4.3.2: External visual and marking examination	
<i>Group 3</i> Sequence (Note 5) 4.5.10 Solderability 4.5.12.1 Tensile Bending (wire or strip) Final measurement or (Note 3) 4.5.10 Solderability 4.5.12.1 Tensile 4.5.12.3 Bending (row) 4.5.12.2 Thrust Final measurements	D	4.5.9: Sealing (Note 1) 4.5.9: Sealing (Note 1)	
<i>Group 4</i> Sequence Initial measurements 4.5.2 Cold 4.5.1 Storage at high temperature Final measurements	ND	4.4.11: Sub-group 05 Temperature: °C Temperature: °C 4.4.11: Sub-group 05	
<i>Group 5</i> Initial measurements 4.5.14 Endurance: 1 000 h ----- Endurance: 2 000 h (Note 6) ----- ----- Final measurements	D	4.4.11: Sub-group 05 4.4.11: Sub-group 05	

NOTES

- 1 Cavity circuits only.
- 2 Mounting conditions as recommended by the detail specification.
- 3 The detail specification shall state which option is to be used.
- 4 The detail specification may delete the damp heat test for unencapsulated circuits.
- 5 Use of completely processed electrical rejects is permitted.
- 6 In assessment level K: provisional approval after 1 000 h;
definitive approval after 2 000 h.
- 7 Applicable to encapsulation having organic material used for sealing purposes.
- 8 Not required for CQCs.

3.3.4 *Maintenance of capability approval*

3.3.4.1 *Screening and lot-by-lot acceptance tests*

The screening and testing on a lot-by-lot basis, for all circuits intended for release to customers are prescribed in the blank detail specification, table 2.

For group A and B tests, the sample shall be collected from one week's production, or such other period as declared by the manufacturer up to a maximum of one month.

3.3.4.2 *Periodic tests*

The periodic tests for CQCs are prescribed in table 3 and the blank detail specification.

Where customer circuits are used as CQCs, samples for periodic testing shall be drawn from lots which have passed the tests of screening when appropriate and lot-by-lot inspection.

Provisional capability approval may be granted after 1 000 h.

3.3.4.3 *Tests*

The complete series of tests specified in the blank detail specification is required for the maintenance of capability approval.

The tests in each group shall be carried out in the order given.

"One defective" is counted when a circuit has not satisfied the whole or a part of the tests of a group.

The approval is maintained when the number of defectives does not exceed the specified number of permissible defectives for each group and the total number of permissible defectives.

3.3.5 *Special requirements*

Small production lots (under consideration).

3.3.6 *Quality conformance inspection*

3.3.6.1 *Test schedule*

The schedule for the lot-by-lot and periodic tests for quality conformance inspection is given in tables 2 and 3 of the blank detail specification.

3.3.6.2 *Assessment levels*

The assessment level(s) for capability approval (see table 1) and for maintenance of capability approval (see relevant blank detail specification) shall be selected from tables 2 and 3 hereafter.

Table 2 - Assessment levels and acceptance criteria
for initial capability approval

In this table: n = sample size;

c = acceptance criterion (permitted number of defectives).

Inspection group or sub-group of table 1	Assessment level								
	K			L			M		
	<i>n</i>	<i>c</i>		<i>n</i>	<i>c</i>		<i>n</i>	<i>c</i>	
01	Required	–		–	–		–	–	
02a	75 (Note 1)	2		64 (note 1)	2		43	2	
02b	8	1		8	1		8	1	
03 (for information only)	2	–		2	–		2	–	
04	39	1	2	26	1	2	13	1	2
05	71 (Note 1)	1		60 (Note 1)	1		39	1	
06	26	1		13	1		8	1	
1	10	1	2	8	1	2	–	–	2
2 (Note 2)	13	1		10	1		8	1	
3	13	1		10	1		8	1	
4	13	1		10	1		8	1	
5 (1 000 h)	–	–		20	1		13	1	
(2 000 h)	20	1		–	–		–	–	

NOTES

1 This number may be reduced by the relevant number of circuits which are not needed when the tests in group 1 are not required.

2 A minimum of four circuits shall be used for each solvent specified.

Table 3 - Assessment levels and acceptance criteria
for quality conformance inspection

Table 3A - Lot-by-lot tests to be conducted on a sampling basis

In this table: *IL* = inspection level;

AQL = acceptable quality level.

Subclause numbers refer to section 4 of the generic specification.

Inspection group or sub-group	Assessment level					
	K		L		M	
<i>Screening (see table 4)</i>	Required		Not required		Not required	
	<i>IL</i>	<i>AQL</i>	<i>IL</i>	<i>AQL</i>	<i>IL</i>	<i>AQL</i>
<i>Sub-group A1</i> 4.3.2 External visual and marking examination	II	1	II	2,5	I	2,5
<i>Sub-group A2</i> 4.4.11 Major static and dynamic electrical characteristics at room temperature	II	0,25	II	0,4	II	1
<i>Sub-group A3</i> 4.4.11 Major static and dynamic electrical characteristics at extreme operating temperatures	S4	1	–	–	–	–
<i>Sub-group B1</i> 4.5.10 Solderability	S3	2,5	S3	2,5	S3	2,5
<i>Sub-group B2</i> 4.3.3 Dimensions	S4	1	S4	1	S4	1

Table 3B - Periodic tests to be conducted on a sampling basis

In this table: p = periodicity (in months);

n = sample size;

c = acceptance criterion (permitted number of defectives);

Subclause numbers refer to section 4 of the generic specification.

Inspection group or sub-group	Assessment level											
	K				L			M				
	<i>p</i>	<i>n</i>	<i>c</i>		<i>p</i>	<i>n</i>	<i>c</i>	<i>p</i>	<i>n</i>	<i>c</i>		
<i>Sub-group C1</i> 4.4.11 Major static and dynamic electrical characteristics at extreme temperatures (Note 8)	–	–	–		6	13	1		6	8	1	
<i>Sub-group C2</i> Sequence (Notes 1 and 2) 4.5.6 Vibration, swept frequency and 4.5.7 Acceleration, steady state or (Note 3) 4.5.5 Shock and 4.5.7 Acceleration, steady state	6	10	1	2	12	8	1	2	–	–	–	2
<i>Sub-group C3</i> Sequence 4.5.11 Resistance to soldering heat 4.4.15.2 Resistance to solvents (Note 7) 4.5.8 Change of temperature 4.5.3 Damp heat, steady state (Note 4)	6	13	1		12	10	1		12	8	1	
<i>Sub-group C4</i> Sequence 4.5.2 Cold 4.5.1 Storage at high temperature	6	13	1		12	10	1		12	8	1	
<i>Sub-group D1</i> 4.5.14 Endurance: 1 000 h Endurance: 2 000 h (Note 6)	– 3	– 20	– 1		6 –	20 –	1 –		6 –	13 –	1 –	
<i>Sub-group D2</i> Sequence (Note 5) 4.5.12.1 Tensile 4.5.12.3 Bending (wire or strip) or (Note 3) 4.5.12.1 Tensile 4.5.12.3 Bending (row) 4.5.12.2 Thrust	12	13	1		12	10	1		12	8	1	
4.5.16 Induced flammability (Note 7) (for information only)	12	2	–		12	2	–		12	2	–	

Notes on page 21, after table 1.

Table 4 – Screening

Sequences for screening shall be in accordance with table 4.

Steps	Examination or test	Generic specification reference	Details and conditions	Sequences				
				A	B	C	D	E
1*	Precap visual inspection	4.3.1	Under consideration	x				
2	Storage at high temperature	4.5.1	24 h at maximum storage temperature	x	x	x		x
3	Change of temperature	4.5.8	10 cycles $T_{\text{stg min.}} : T_{\text{stg max.}}$	x	x	x		x
4*	Acceleration, steady state	4.5.7	In the most critical direction. Acceleration level as specified in the detail specification	x	x	x		
5*	Sealing	4.5.9		x	x	x		
6	Electrical measurements (pre burn-in)		Selected parameters Remove defective devices (Note 1)	x	x		x	
7	Burn-in		As specified in the detail specification hours: 168 72 48	x	x		x	
8	Electrical measurements (post screening)		As specified in 6 Remove defective devices Reject lot if defects exceed 10 %	x	x	x	x	x
* Not normally applicable to non-cavity devices, unless specified in the detail specification.								

NOTES

1 Record the results of the measurements unless otherwise specified in the detail specification.

2 Screening is normally performed before group A, B and C inspection. When screening is performed after meeting the requirements of groups A and B on a lot-by-lot basis and group C on a periodic basis, the solderability, sealing and group A tests shall be repeated.

Additional post-screening tests may be required as specified in the blank detail specification.

3.4 Resubmission of rejected lots (lot-by-lot inspection)

Any lot rejected following electrical tests shall be returned to production for rework or rescreening for the identified defect. No new circuit shall be included in the lot.

The lot shall then be resubmitted and inspected under conditions of tightened inspection.

It will retain the same lot number and details of the new submission will be recorded. The same lot shall not be submitted more than three times.

3.5 *Manufacturing stages in a factory of an approved manufacturer in a non-IEC member country*

The application of the extension of the manufacturer's approval is permitted for the film integrated circuits and hybrid film integrated circuits covered by this sectional specification, provided that the conditions of subclause 3.2 of the generic specification are met.

4 Test and measurement procedures

This clause contains all the tests and measurement procedures which are of typical application for film integrated circuits and hybrid film integrated circuits and which are not described in section 4 of the generic specification.

Each detail specification shall state all the tests and measurement procedures required for lot-by-lot inspection and periodic testing. It shall, as a minimum, include the relevant tests given in this specification with stated methods and severities.

Environmental tests, measurements, severities and end-point limits for periodic tests of the CQCs shall be included in the detail specification. They shall be in accordance with the applicable numbers of the generic specification and this sectional specification.