

**Harmonized system of quality
assessment for electronic components**

**Semiconductor
devices —
Integrated circuits —
Sectional specification
for semiconductor
integrated circuits
excluding hybrid
circuits —**

**Section 1: Internal visual examination
for semiconductor integrated circuits
excluding hybrid circuits**

NOTE This British Standard should be used in conjunction with BS QC 790100:1991.

Committees responsible for this British Standard

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- Electronic Components Industry Federation
- GAMBICA (BEAMA Ltd.)
- Ministry of Defence
- National Supervising Inspectorate
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National foreword

This British Standard has been prepared under the direction of the Electronic Components Standards Policy Committee. It is identical with IEC 748-11-1:1992 (QC 790101) *Semiconductor devices. Integrated circuits — Part 11: Sectional specification for semiconductor integrated circuits excluding hybrid circuits — Section 1: Internal visual examination for semiconductor integrated circuits excluding hybrid circuits*, published by the International Electrotechnical Commission (IEC) and is a harmonized specification within the IECQ system of quality assessment for electronic components.

The standard is a supplement to IEC 748-11:1990 (BS QC 790100:1991).

Cross-reference

International Standard	Corresponding British Standard
IEC 748-11:1990 (QC 790100)	BS QC 790100:1991 <i>Semiconductor devices. Sectional specification for semiconductor integrated circuits excluding hybrid circuits</i> (Identical)

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Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, pages 1 to 26, an inside back cover and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

1 Scope and object

The purpose of these tests is to check the internal materials, construction and workmanship of integrated circuits for compliance with the requirements of the applicable specification.

These tests will normally be used prior to capping or encapsulation on a 100 % inspection basis to detect and eliminate devices with internal defects that could lead to device failure in normal application. They may also be employed on a sampling basis prior to capping to determine the effectiveness of the manufacturer's quality control and handling procedures for semiconductor devices.

2 Apparatus

The apparatus for this test shall include optical equipment capable of the specified magnification(s) and any visual standards (gauges, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate fixturing shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.

3 Procedure for integrated circuits

3.0 Introduction

3.0.1 General

The device shall be examined in a suitable sequence of observations within the specified magnification range to determine compliance with the requirements of the applicable specification and the criteria of the specified test condition. The inspections and criteria in this method shall be required as inspections for all devices and locations to which they are applicable. Where the criterion is intended for a specific device, process or technology, this is indicated.

Complex devices may require the substitution of alternative screening procedures for visual examination criteria pertaining to metal coverage, oxide and diffusion faults that are difficult or impractical to perform. These alternative screening methods and procedures are documented in the applicable detail specification and their use shall be on an optional basis.

The requirements are applicable to technologies with line widths down to 2 μm .

3.0.2 Sequence of inspection

The order in which criteria are presented is not a required order of examination and may be varied at the discretion of the manufacturer. Visual criteria specified in 3.1.1.2, 3.1.1.5, 3.1.1.7, 3.1.2, items 5) and 6) of 3.1.7, 3.1.8, items 1), 2) and 4) of 3.1.9 may be examined prior to die attachment without required reexamination after die attachment. The visual criteria specified in 3.1.6.2 and 3.1.6.3 may be examined prior to bonding without reexamination after bonding. The visual criteria specified in 3.1.1.1 and 3.1.3 may be examined prior to die attachment at high magnification provided they are reexamined after die attachment at low magnification. When inverted mounting techniques are employed, the inspection criteria contained herein that cannot be checked after mounting shall be checked prior to attachment of the die. Devices which fail any test criteria herein are defective devices. They shall be rejected and removed at the time of observation.

3.0.3 Air cleanliness classes

The two classes defined by this specification are shown below. Classifications are based on particle count with a maximum allowable number of particles 0,5 μm and larger, or 5,0 μm and larger per unit volume.

Particle size is expressed as the apparent maximum linear dimension or the diameter of the particle.

One of the following particle counting methods shall be employed on the site in use:

- 1) For particle sizes 0,5 μm and larger, equipment employing light scattering principles shall be used.
- 2) For particle sizes 5,0 μm and larger, microscopic counting of particles collected on a membrane filter, through which a sample of air has been drawn, may be used.
- 3) Other monitoring methods and equipment may be used only if demonstrated to be of an accuracy and repeatability equal to those methods listed above.

Manual microscopic methods are adequate for monitoring air in the 3 500 class. Particle counts are to be taken at specified intervals during work activity periods at a location which will yield the particle count of the air in the proximity of the work location. The preferred location for the particle count is at work level height with the sampling probe pointed into the air stream.

3.0.3.1 Class 3,5

Particle count not to exceed a total of 3,5 particles of 0,5 μm per litre and larger or 0,35 particle of 5 μm and larger per litre.

3.0.3.2 Class 3 500

Particle count not to exceed a total of 3 500 particles of 0,5 µm per litre and larger or 25 particles of 5 µm and larger per litre.

3.0.4 Inspection control

In all cases, examination prior to final preseal inspection shall be performed under the same quality program that is required at the final preseal inspection station. Care shall be exercised after inspections per 3.0.2 to ensure that defects created during subsequent handling will be detected and rejected at final preseal inspection. During the time interval between visual inspection and preparation for sealing, devices shall be stored in a controlled environment.

3.0.5 Magnification

High magnification inspection shall be performed perpendicular to the die surface with normal light incidence. Low magnification inspection shall be performed with either a monocular, binocular or stereo-microscope from any appropriate angle, with the device suitably illuminated. The inspection criteria of 3.1.4 and 3.1.6.1 may be examined at high magnification at the manufacturer's option.

3.0.6 Definitions (for inspection purposes only)

1) **Active circuit area** includes all kinds of functional circuit elements, operating metallization or any connected combinations thereof excluding beam leads.

NOTE In this context, "active" is the counterpart of "inactive" and has nothing to do with active and passive components.

2) **Controlled environment** shall be in accordance with the requirements of class 3,5 environment for air cleanliness. The use of an inert gas environment such as nitrogen shall satisfy the requirements for storing in controlled environment. The relative humidity shall not exceed 50 %.

3) **Diffusion tub** is an isolated volume of semiconductor material, of either "P" or "N" type, surrounded by isolation material.

4) **Foreign material** is any material not used in the manufacture of the microcircuit or any material that is displaced from its original or intended position within the micro-circuit package and shall be considered attached if it cannot be removed by a nominal gas blow of approximately 140 kPa.

Conductive foreign material is defined as any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspection.

NOTE A particle shall be considered embedded in the glassivation when there is evidence of colour fringing around the periphery of the particle.

5) **Functional circuit elements** are active or passive components such as diodes, transistors, capacitors, resistors, crossunders, etc.

6) **Gate oxide bridge** is the area lying between the drain and source diffusions of MOS structures. References to the metallization covering the gate oxide bridge shall include all materials that are used for the gate electrode.

7) **Glassivation** is the top layer of insulating material that covers the active circuit area including metallization, except bonding pads and beam leads. Cracking is the presence of minute cracks in the glassivation.

8) **Junction** is the outer edge of the passivation step that delimits the boundary between "P" and "N" type semiconductor material.

9) **Multilayered metallization** (conductors) is two or more layers of metal or any other material used for interconnections that are not isolated from each other by a grown or deposited insulating material. The term "underlying metal" shall refer to any layer below the top layer of metal.

10) **Multilevel metallization** (conductors) is two or more layers of metal or any other material used for interconnections that are isolated from each other by a grown or deposited insulating material.

11) **Operating metallization** (conductors) is any metal or any other material used for interconnection except metallized scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads and identification markings.

12) **Organic polymer (epoxy) vapour residue** is the material that is emitted from the polymer, that forms on an available surface.

13) **Original width** is the width dimension or distance that is intended by design (e.g. original metal width, original diffusion width, original beam width, etc.).

14) **Passivation step** is a change in thickness of the passivation for metal to metal or metal to silicon interconnection, by design, excluding lines on the surface where passivation layers have been removed as a result of normal device processing.

15) **Passivation** is the silicon oxide, nitride or other insulating material that is grown or deposited directly on the die prior to the deposition of metal.

16) **Peripheral metal** is all metal that lies immediately adjacent to or over the scribe grid.

17) **Thick film** is a film deposited, for example, by screen printing processes and fired at high temperature to fuse into its final form.

18) **Thin film** is a film (usually less than 10 μm thickness) which is deposited onto a substrate by an accretion process such as vacuum evaporation, sputtering or pyrolytic decomposition.

19) **Substrate** is the supporting structural material into and/or upon which the passivation, metallization and circuit elements are placed.

20) **Narrowest resistor width** is the narrowest portion of a given resistor, prior to trimming. The narrowest resistor width for a block resistor may be specified in the approved manufacturer's documentation.

21) **Kerf** is that portion of the resistor area from which resistor material has been removed or modified by trimming.

22) **Detritus** is a fragment of the original or laser-modified resistor material remaining in the kerf.

23) **Block resistor** is a sheet resistor which, for trimming purposes, is designed to be much wider than would be dictated by power density requirements and shall be identified in the approved manufacturer's precap visual implementation document.

24) **Rebond** is a second bonding made between two pads, or a pad and a bonding terminal, to replace the original bonded wire, which has either been removed, leaving the welded portion of the bond attached to the pad or bonding terminal, or failed to adhere at the first bonding attempt.

25) **Scratch** is any tearing defect. Probe marks in the surface of the metallization are considered as scratches.

26) **Void** is any region in the metallization where underlying material is visible and which is not caused by a scratch.

3.0.7 Interpretation

For inspections performed in the magnification range of 100 x to 200 x, the criteria of "2,5 μm of passivation or metal" can be satisfied by a "line of separation" or a "line of metal". Reference herein to "that exhibits" shall be considered satisfied when the visual image or visual appearance of the device under examination indicates that a specific condition is present and shall not require confirmation by any other method of testing.

3.1 Test conditions

Internal visual examination as required in 3.1.1 through 3.1.6 shall be conducted on each microcircuit and each integrated circuit chip. In addition, the applicable criteria in 3.1.7 through 3.1.9 shall be used for the appropriate microcircuit areas where glassivation, dielectric isolation or film resistors are used. The high magnification inspection shall be performed within the range of 100 x to 200 x and the low magnification inspection within the range of 30 x to 60 x.

3.1.1 Metallization defects, high magnification

No device shall be acceptable that exhibits the following in the operating metallization:

3.1.1.1 Metallization scratches

1) Scratch in the metallization that exposes underlying passivation anywhere along its length and leaves less than 50 % of the original metal width undisturbed (see Figure 3).

2) Scratch that completely crosses a metallization path and damages the surface of the surrounding passivation on either side (for MOS devices, the path shall be the (*L*) dimension [see Figure 4]).

3) Scratch in multilayered metallization that exposes the underlying metal anywhere along its length and leaves less than 25 % of the top layer original metal width undisturbed (see Figure 3).

NOTE The criteria of items 1), 2) and 3) can be excluded for peripheral power or ground metallization where parallel paths exist, so that an opening at the scratch would not cause an unintended isolation of the metallization path.

4) Scratch in the metallization over a passivation step that leaves less than 75 % of the original metal width at the step undisturbed.

NOTE The criteria of items 1) through 4) can be excluded for the last 25 % of linear length of the contact cut and all metal beyond on the termination end(s) of the metallization runs. In these cases, there shall be at least 50 % of the contact opening area covered by metallization and at least a continuous 40 % of the contact opening perimeter covered by undisturbed metallization (see Figure 5).

5) Any scratch in the metallization, over the gate oxide bridge, that exposes underlying passivation and leaves less than 50 % of the length or width of the metallization between source and drain diffusions undisturbed (see Figure 4) (applicable to MOS structures).

6) Scratch in the metallization that exposes the dielectric material of a thin film capacitor or cross-over.

7) Scratch in the bonding pad or fillet area that exposes underlying passivation and reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 % of the narrowest entering interconnect metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately.

8) Scratches (probe marks, etc.) in the bonding pad area that expose underlying passivation over more than 25 % of the original unglassivated metallization area.

3.1.1.2 Metallization voids

1) Voids in the metallization that leave less than 50 % of the original metal width undisturbed (see Figure 6).

NOTE This criterion can be excluded for peripheral power or ground metallization where parallel paths exist so that an opening at the voids would not cause an unintended isolation of the metallization path. When application of this exclusion causes or permits a device design to exceed the current density limitation imposed by the design document, this exclusion shall not apply. Current density shall be determined by design, not visual inspection.

2) Voids in the metallization over a passivation step that leave less than 75 % of the original metal width at the step undisturbed.

NOTE The criteria of items 1) and 2) can be excluded for the last 25 % of linear length of the contact cut and all metal beyond on the termination end(s) of the metallization runs. In these cases, there shall be at least 50 % of the contact opening area covered by metallization and at least a continuous 40 % of the contact opening perimeter covered by undisturbed metallization (see Figure 5).

3) Voids in the metallization over the gate oxide bridge that leave less than 75 % of the metallization length (L) between source and drain diffusions undisturbed (see Figure 4) (applicable to MOS structures).

4) Voids that leave less than 60 % of the metallization area over the gate oxide bridge undisturbed (applicable to MOS structures).

5) Voids that leave less than 75 % of the metallization width coincident with the source or drain diffusion junction line undisturbed (see Figure 4) (applicable to MOS structures).

6) Voids in the bonding pad area that leave less than 75 % of its original unglassivated metallization area undisturbed.

7) Voids in the bonding pad or fillet area that reduce the metallization path width connecting the bond to the interconnecting metallization to less than 50 % of the narrowest entering interconnect metallization stripe width (see Figure 7).

NOTE If two or more stripes enter a bonding pad, each shall be considered separately.

8) Voids in the metallization of a thin film capacitor that reduce the metallization area by more than 25 %.

3.1.1.3 Metallization corrosion

Any metallization corrosion.

3.1.1.4 Metallization adherence

Any metallization lifting, peeling or blistering.

3.1.1.5 Metallization probing

The criteria contained in 3.1.1.1 shall apply as limitations on probing damage.

3.1.1.6 Metallization bridging

Any metallization bridging where the separation between any two metallization paths is reduced to less than 2,5 μm unless by design.

3.1.1.7 Metallization alignment

1) Contact window that has less than 50 % of its area covered by metallization.

2) Contact window that has less than 40 % of its perimeter covered by metallization.

NOTE When, by design, metal is completely contained in a contact window, the criteria of item 1) area coverage and of item 2) perimeter coverage can be deleted as applicable provided the design criteria are satisfied.

3) A metallization path not intended to cover a contact window that is separated from the window by less than 2,5 μm .

4) Any exposure of the gate oxide bridge from source to drain diffusions (see Figure 8) (applicable to MOS structures).

5) Any exposure of the gate oxide bridge that leaves less than 75 % of the metallization coincident with the source and drain diffusion junction line undisturbed (applicable to MOS structures).

6) Gate metallization not coincident with or extending over the diffused guard ring.

NOTE This criterion applies to MOS structures containing a diffused guard ring. MOS devices that do not contain a diffused guard ring shall have gate metallization extending not less than 2,5 μm beyond the gate oxide bridge (see Figure 4 and Figure 8).

3.1.2 Diffusion and passivation layer faults, high magnification

No device shall be acceptable that exhibits the following:

1) Any diffusion defects that allow unintentional bridging between diffused areas (see Figure 9).

2) Any isolation diffusion that is discontinuous, except isolation walls around unused areas or bonding pads, or any other diffused area with less than 25 % of the original diffusion width remaining.

3) Either multiple lines or a complete absence of passivation visible at the edge and continuing under the metallization (see Figure 10).

NOTE Double or triple lines indicate that it can have sufficient depth to penetrate down to bare silicon; however, should the absence of glassivation in the defect area or the characteristics of the present glassivation allow verification of the presence or absence of passivation by colour or colour comparisons, respectively, then these techniques may be used. The criterion of item 3) can be excluded when a second passivation layer is applied in a separate operation and by a different process prior to metallization deposition.

4) An active junction not covered by passivation, unless by design.

3.1.3 *Scribing and die defects, high magnification*

No device shall be acceptable that exhibits:

1) Less than 25 μm of passivation visible between the operating metallization or bond periphery and the edge of the die.

NOTE This criterion can be excluded for peripheral metallization including bonding pads where the metallization is at the same potential as the die.

2) A chip out in the active circuit area (see Figure 11).

NOTE This criterion can be excluded for peripheral metallization that is at the same potential as the die. At least 50 % of the undisturbed metallization width shall remain at the chip out, except that there shall be no width criteria where parallel paths exist, so that an opening at the chip out would not cause an unintended isolation of the metallization path.

3) Any substrate or passivation crack in the active circuit area or a crack that exceeds 75 μm in length (see Figure 11).

4) Any crack that comes closer than 25 μm to any operating metallization or other active circuit area on the die (see Figure 11).

NOTE This criterion can be excluded for peripheral metallization that is at the same potential as the die.

5) A crack that exceeds 25 μm in length, inside the scribe grid or scribe line and points toward operating metallization or functional circuit elements (see Figure 11).

3.1.4 *Bond inspection, low magnification*

These inspection and criteria shall be required for the bond type(s) and location(s) to which they are applicable when viewed from above.

NOTE A wire tail is not considered part of the bond when determining physical bond dimensions.

3.1.4.1 *Gold ball bonds*

No device shall be acceptable that exhibits:

1) Gold ball bonds on the die or package post where the ball bond diameter is less than twice or greater than six times the wire diameter.

2) Gold ball bonds where the wire exit is not completely within the periphery of the ball and where the wire does not exit vertically for a distance of at least one wire diameter before arcing.

3) Gold ball bonds where the wire centre exit is not within the boundaries of the bonding pad.

4) Intermetallic formation extending radially more than 2,5 μm completely around the periphery of any gold ball bond for that portion of the gold ball bond located on metal.

3.1.4.2 *Wedge bonds*

No device shall be acceptable that exhibits:

1) Ultrasonic wedge bonds on the die or package post that are less than 1,2 times or greater than three times the wire diameter in width, or are less than 1,5 times or greater than five times the wire diameter in length (see Figure 12).

2) Thermocompression wedge bonds on the die or package post that are less than 1,5 times or greater than three times the wire diameter in width, or are less than 1,5 times or greater than five times the wire diameter in length (see Figure 12).

3) Wedge bonds at the point where metallization exits from the bonding pad that do not exhibit a line of undisturbed metal visible between the periphery of the bond and at least one side of the entering metallization stripe (see Figure 7 and Figure 13).

NOTE 1 This criterion can be excluded when the entering metallization stripe is greater than 50 μm in width and the bond pad dimension on the entering metal stripe side is greater than 90 μm .

NOTE 2 These requirements for a visual line of metal can be satisfied when an acceptable wire tail obscures the area of concern, providing the following condition exists: the bond is located more than 2,5 μm from the intersecting line of the entering metallization stripe and the bonding pad, and there is no visual evidence of disturbed pad metallization at the bond and wire tail interface.

3.1.4.3 *Tailless bonds (crescent)*

No device shall be acceptable that exhibits:

1) Tailless bonds on the die or package post that are less than 1,2 times or greater than five times the wire diameter in width, or are less than 0,5 times or greater than three times the wire diameter in length (see Figure 12).

2) Tailless bonds where the bond impression does not cover the entire width of the wire.

3) Tailless bonds at the point where metallization exits from the bonding pad that do not exhibit a line of undisturbed metal visible between the periphery of the bond and at least one side of the entering metallization stripe.

3.1.4.4 General (gold ball, wedge and tailless)

No device shall be acceptable that exhibits:

- 1) Bonds on the die where less than 50 % of the bond is within the unglassivated bonding pad area.
- 2) Bonds on the package post that are not completely within two package post widths (i.e. the narrowest post width) from the inner edge of the package post, or bonds that are not completely within the boundaries of the package post.
- 3) Bonds placed so that the wire exiting from the bond crosses over another bond.
- 4) Bonds placed so that the separation between the bonds or between the bond and operating metallization not connected to it is less than 2,5 μm .
- 5) Wire bond tails that extend over or make contact with any metallization not covered by glassivation and not connected to the wire.
- 6) Wire bond tails that exceed two wire diameters in length at the bonding pad or four wire diameters in length at the package post.
- 7) Bonds where less than 50 % of the bond is located within an area that is free of die preform mounting material.
- 8) A bond on top of another bond, bond wire tail or residual segment of lead wire. An ultrasonic wedge bond alongside a previous bond, where the observable width of the first bond is reduced by less than 6 μm , is considered acceptable.
- 9) Any evidence of repair of conductors by bridging with an addition of bonding wire or ribbon.

3.1.4.5 Rebonding

Rebonding is allowed for monolithic integrated circuits when:

- 1) At least 50 % of the attachment area of a rebond is placed on undisturbed metal (excluding probe marks which do not expose underlying passivation).
- 2) A maximum of one rebond attempt has been made at any one bonding pad or bonding terminal location.
- 3) The bond pad area is large enough to accommodate a rebond.
- 4) The second bond is at a point near to the metallization exit.

3.1.5 Internal leads, low magnification

This inspection and criteria shall be required for the lead type(s) and location(s) to which they are applicable.

3.1.5.1 Wires

No device shall be acceptable that exhibits:

- 1) Any wire that touches another wire (excluding common wires), package post, unglassivated operating metallization, die or any portion of the package.
- 2) Excessive loop or sag in any wire so that it comes closer than two wire diameters to another wire, package post, unglassivated operating metallization or die, or to a portion of the package. However, this requirement does not apply within a volume defined by a spherical radial distance from the bond perimeter on the die surface of 125 μm for ball bonds, or 250 μm for ultrasonic and thermocompression bonds.
- 3) Nicks, cuts, crimps, scoring or neckdown in any wire that reduces the wire diameter by more than 25 %.
- 4) Wire bond tails that exceed two wire diameters in length at the bonding pad or four wire diameters in length at the package post.
- 5) Tearing at the junction of the wire and bond.
- 6) Any wire making a straight line run from die bonding pad to package post that has no arc [see also item 2) of 3.1.4.1].
- 7) Wire(s) crossing wire(s) (except common conductors).
- 8) Wire(s) not in accordance with bonding diagram.

3.1.6 Package conditions, low magnification

No device shall be acceptable that exhibits:

3.1.6.1 Foreign material

Foreign material or particles may be blown off with a normal gas blow (approximately 140 kPa). The device shall then be inspected and be rejected when it exhibits the following:

- 1) Unattached foreign material on the surface of the die or within the package.
- 2) Unattached foreign material on the surface of the lid or cap.

NOTE This criterion can be satisfied by a normal gas blow (approximately 140 kPa) or a suitable cleaning process, providing that the lids or caps are subsequently held in a controlled environment until capping.

- 3) Attached conductive foreign material that bridges metallization paths, package leads, lead to package metallization, functional circuit elements or junctions, or any combination thereof.

- 4) Ink on the surface of the die that covers more than 25 % of a bonding pad area or that bridges any combination of unglassivated metallization or bare silicon area.