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CECC

Système Harmonisé d'Assurance de la Qualité
des Composants Electroniques

DOCUMENT GUIDE:

QUESTIONNAIRE D'AUDIT
DES LIGNES DE FABRICATION
DES CIRCUITS INTEGRES ET DES ASIC
(BASE SUR EN 190 000)

Harmonized System of Quality Assessment for
Electronic Components

GUIDANCE DOCUMENT:

QUESTIONNAIRE FOR AUDITING
IC & ASIC MANUFACTURING LINES
(BASED ON EN 190 000)

Harmonisiertes Gütebestätigungssystem für
Bauelemente der Elektronik

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FRAGENKATALOG: AUDITS
FÜR IC UND ASIC FERTIGUNGSLINIEN
(AUF DER BASIS VON EN 190 000)



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QUESTIONNAIRE FOR AUDITING IC and ASIC MANUFACTURING LINES (BASED ON EN190,000)

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QUALITY ORGANIZATION

1. QUALITY MANAGEMENT

- 1.1 Describe the Technology Review Board (TRB) or the equivalent organisation in the company, facility or task.
- 1.2 Describe the domains of activities and the levels of decisions and responsibilities of the TRB. Show how it concerns:
 - Total Quality Management programme
 - review and maintenance of all processes
 - change control
 - reliability data analysis
 - failure analysis, corrective actions
 - rework
 - European Qualified Manufacturing List components recall procedures
 - qualification status of technology.
- 1.3 Describe the TQM plan. Show how it concerns the following activities, as a minimum :
 - Quality plan
 - Manufacturing process failure analysis
 - Field failure return programme
 - Quality improvement plan
 - Statistical Process Control plan
 - Corrective action plan
 - Change control programme
 - Test vehicles assessment plan
 - EQML certification/qualification plan.

2. QUALITY IMPROVEMENT PLAN

- 2.1 Describe the analysis performed for continuous improvement of quality.
- 2.2 Which areas are affected by the quality improvement programme (QIP)?
- 2.3 Describe the QIP.
- 2.4 Are SPC data used in the QIP?
- 2.5 Are data resulting from failure analysis and field return used in the QIP?

3. SUBCONTRACTING

- 3.1 Describe reasons for subcontracting
- 3.2 Are subcontractors external or internal (belonging to the same organisation)?
- 3.3 Which activities are subcontracted?
- 3.4 Which procedures are used to select subcontractors?
- 3.5 Is there an updated list of subcontracted activities?

- 3.6 How many times is the list updated in a year?
- 3.7 Are deliveries from a subcontractor managed in a different way as compared to normal purchases?
- 3.8 Describe the programme for auditing subcontractors (frequency, relevant documents, etc.)
- 3.9 How are corrective actions performed on subcontractors?
- 3.10 Which controls are performed on subcontractors' suppliers?
- 3.11 How are audit results taken into account for the performance of corrective actions?

4. CONCURRENT ENGINEERING

- 4.1 Is there correlation between the system design and the component design?
- 4.2 Are there a strategy and tools to correlate system development, including possible engineering changes, and ASIC development, in order to maintain both coherency and parallel time scheduling between the two processes?
- 4.3 Is there interaction between the designers and production engineers?
- 4.4 Are training courses for the designers on "design for manufacturability" (DFM) organised, and do records exist to identify trained personnel?
- 4.5 Is there a group gathering knowledge on design and on fields of manufacture, appointed with the objectives of:
 - contributing to the design, checking (or imposing) manufacturability constraints
 - transferring to the production phase the knowledge acquired during the design phase?
- 4.6 Are design specifications defined in accordance with the available technologies and manufacturing processes?
- 4.7 Are the processes that need to be modified or newly developed clearly identified?

5. STATISTICAL PROCESS CONTROL

- 5.1 How long has an SPC programme been in use?
- 5.2 How many processes are SPC- monitored (define a list and the percentage of the totality of processes)?
- 5.3 How are control parameters determined?
- 5.4 How are control limits for each parameter defined?
- 5.5 How are SPC data analysed and processed?
- 5.6 Define frequency and size for each sampling activity
- 5.7 How are security and repeatability of sampling ensured?
- 5.8 Which kind of training on SPC is undertaken for:
 - managers
 - engineers
 - operators?
- 5.9 Which actions are taken if one out-of-control point is detected?
- 5.10 When is the production stopped? Which procedures are used to restart production?

6. ELECTROSTATIC DISCHARGE (ESD) PROTECTION ORGANISATION

- 6.1 Which kind of policy is in place to avoid electrostatic discharge?
- 6.2 Which procedures are applied?
- 6.3 Which areas are ESD-protected?
- 6.4 Are protection levels specified for protected areas?
- 6.5 Are there company developed specifications for ESD?
- 6.6 Are audits on ESD performed periodically? If so, specify references (checklist, norms, etc.)
- 6.7 Which subjects are analysed during ESD audits?
- 6.8 Which instruments are used by auditors?
- 6.9 Is personnel training on ESD matters performed regularly?
- 6.10 Is CECC 00015 (EN 100015) applied?
- 6.11 Does an updated list of material usable in ESD-protected areas exist?

7. SECURITY

- 7.1 How are safety and security guaranteed for all kinds of paper documents?
- 7.2 How are safety and security guaranteed for all kinds of computer-based documents?
- 7.3 Is a master list of all documentation available and regularly updated?
- 7.4 Are archives and backups positioned in different locations in order to avoid loss?
- 7.5 Is access to data restricted to authorised personnel only?
- 7.6 Are recovery plans from facility loss foreseen?
- 7.7 Are the same provisions on security applied to sub-contractors?
- 7.8 Are there second source suppliers for all strategic material?
- 7.9 Which strategies are adopted in order to prevent supplier loss risk?

PROCESS DESIGN (M1)

- a) Describe the Process Design flowchart.
- b) Does it include process characterisation (see M4)?
- c) If not describe the interfaces between process design and process characterisation.
- d) Are preliminary specifications defined (user needs analysis, exhaustive functional description, chip area estimates, dynamic performances estimates, working conditions, target tool, etc.) in order to establish a preliminary evaluation of the performance of new library element?
- e) Are these specifications reviewed to ensure coherence with characterisation and verification results?
- f) In which way are design rules defined and verified ?
- g) Which reliability rules are taken into account?
- h) Describe in which way the standard for libraries is developed.
- i) Is there process design involvement to create elementary elements of new library? If so, describe it
- j) Do these elements include complete geometric representation, data sheet, validation representation and test vectors for fixed cells?
- k) Do these elements include primitive geometric representation, equations for calculation of geometry, outline, timing, consumption, validation methodology and test vectors for parametric cells?
- l) Are timing parameters of the cells estimated using back annotation procedures or measurement by an electron beam test system?
- m) How are the delay parameters of library macro blocks derived (e.g. by interpolating single cell delay parameters or using a back annotation procedure applied to the full block or measuring with an electron beam test system)?
- n) In which way are the new library elements integrated into the Computer Aided Design tool?
- o) Are libraries documented at electrical and layout levels, in order to allow the designer to perform small modifications of critical cells?
- p) Does this integration include icons or icons generating programmes, logic and dynamic simulation models, specific tests for new elements?
- q) How is technology mapping performed on the basis of a given library?

[G.I.1] SCOPE AND FIELD OF COMPETENCE AND CAPABILITY

- a) How does the process design centre manage the quality according to quality manual?
- b) Who controls the following items:
 - process design management
 - senior project leaders
 - IC design group representatives
 - integration group management
 - representatives of other tasks as appropriate to the declared scope?
- c) Does the claimed competence and capability include the following :
 - basic technologies (processes) , layers , elements , geometries, etc.
 - target IC families covered
 - design rules identification
 - CAD data and tools
 - IC application fields supported
 - procedures to start process design activities?

[G.I.2] DESCRIPTION OF ACTIVITIES

- a) How are the organisation, procedures and activities of the Process Design Centre described?
- b) How are the following items identified:
 - structure and quality management system
 - design process including inputs and outputs
 - interfaces with other tasks and entities (suppliers, contractors, etc.)
 - design rules and CAD library interactions
 - CAD tools for design and validation
 - procedures for process characterisation and design validation?

[G.I.3] INTERFACES AND SUB-CONTRACTING PROCEDURES**[G.I.3.1]**

- a) Describe customer interfaces (types and controls of specifications, CAD requirements and deliverables, validation procedures and specifications, responsibilities and customer involvement).

[G.I.3.2]

- a) Which activities are sub-contracted?
- b) Do they include:
 - mask making (for test circuits)
 - wafer fab (for test circuits , process characterisation, etc.)
 - assembly and packaging (for test circuits , process characterisation , etc.)
 - test, measurement, and analysis (electrical and environmental)
 - CAD activities
- c) How are the sub-contracted activities described and specified?

[G.I.3.3]

- a) How are the approved mask makers identified?
- b) How are they qualified?
- c) If external mask makers are used, are they identified and qualified and are the scope and limits of capability clearly defined?

[G.I.3.4]

- a) If external test laboratories are used, are they identified and qualified and are the scope and limits of capability clearly defined?

[G.I.3.5]

- a) Does the process design centre list all wafer-fabrications for which they design processes?
- b) How are they qualified?

[G.I.3.6]

- a) How are all special requirements for assembly /packaging detailed in design rules?

- b) If external assembly/packaging operations are used, how are they qualified?

[G.I.4] PROCEDURES FOR DESIGN AND VERIFICATION TOOLS

- a) Are the procedures for creation, verification, validation and integration of CAD design rules and library elements stated for each CAD tool qualified?
- b) Where are the processes for the creation of new library elements described?
- c) Which procedures are specified for verification and validation of characteristics and application rules for library elements?

[G.I.5] PROCEDURES FOR INTEGRATION AND VALIDATION

- a) Which procedures define the methodology used to integrate a new library element in a qualified CAD tool?
- b) Which icon generation methods or icon calculation programs are used?
- c) Are the definition and validation of logic and dynamic simulation models defined in co-ordination with the final characteristics of the element?
- d) How are the simulation results of the schematic diagram (extracted from the layout) and the logic simulation results of library elements compared?
- e) Which elements are used to check the accuracy of the dynamic characteristics, and how is this done?
- f) How are the analogue simulation results on critical paths and the logical dynamic simulations after layout compared?
- g) How are analogue and dynamic simulations and results obtained from test circuits correlated?

IC DESIGN (M2)

- a) Describe the IC design centre organisation , activities and responsibilities.
- b) What is the relationship between the IC design centre and the customer?
- c) Which documents are used to define the product?
- d) Are mask making and test program/pattern generation under IC Design Centre responsibility?
- e) If yes, describe the activities; if no, describe the relationship and the inputs between the two organisations.

[G.II.1] SCOPE AND FIELD OF COMPETENCE AND CAPABILITY

- a) Describe the capability, technology and type of circuits for which the centre claims competence.
- b) Which tasks are essential to the design of a circuit?
- c) How are they listed and documented?
- d) Which activities are subcontracted?
- e) Are they identified and how are they managed?
- f) How are ICs, developed by the centre, identified?
- g) How are semiconductor materials (GaAs, Si, etc.), Processes (MOS, etc.), technologies (analogue, mixed, ECL , etc.) assembly methods and packaging defined and identified?

[G.II.2] DESCRIPTION OF ACTIVITIES

- a) How are the activities of the design centre documented?
- b) Is a flow chart of these activities available?
- c) Do the activities include: ... (see page G21)?
- d) How is the relationship between subcontractors identified in the design review?

[G.II.3] INTERFACES

[G.II.3.1.]

- a) Is the interface to CAD process design identified?
- b) Does it include:
 - management of software configuration and library updates,
 - upward compatibility
 - documentation
 - traceability
 - usage limits
 - usage of verification tools?

[G.II.3.2]

- a) How are the interface with, and the involvement of, the customer during the various design steps clearly identified?
- b) Are specifications defined while the system (equipment) is still under development, so that they can be changed during the device design?
- c) Are system partitioning and the selection of the functions to be integrated the result of the co-operation between system and device designers?
- d) How do system and device designers cooperate during the specification formalisation phase?
- e) Are functional requirements thoroughly discussed with possible users to clarify the object of the project?
- f) How are worst case conditions in which the device must operate examined to ensure high availability of the device?
- g) How are stabilised and safe (as opposed to marginal) technologies selected?
- h) How often are specifications checked with system designers to ensure correlation between what is currently expected and the device under development?
- i) Do specification include: writing the technical need specifications, design, functional simulation, test oriented simulation, place and route, characterisation and evaluation of prototypes?
- l) Is the design centre responsible for the application of the design and fabrication rules?
- m) Is the design centre responsible for the correct test methodology in order to fulfil the requirements of the specifications?
- n) Is the design centre responsible for verifying that selected subcontractors are qualified and operate only within their qualified capability?

[G.II.3.3]

- a) Is a list of qualified mask makers available?
- b) Is the following information available in respect of mask makers:
 - name , address
 - proof of approval by specified foundries for the specified process
 - name of the supervisor of the mask maker
 - identification of the capability manual of the mask maker
 - a brief summary of the interface between the design centre and the mask maker?

[G.II.3.4]

- a) Describe the interface between the design centre and the wafer-fabrication plants.
- b) Does this interface include details regarding design review, process change notification and test results?
- c) Does the design centre specify rules for delivering the prototypes?
- d) Does the design centre specify rules for full production?
- e) Is a list of qualified wafer-fabrication plants available?
- f) Is the following information available for qualified wafer-fabrication plants:
 - name and address
 - name of the supervisor of wafer fab
 - identification of the capability manual
 - the technologies and procedures used?
- g) Is a list of documents, tools, etc., to be transferred to wafer-fabrication plants available?

[G.II.3.5]

- a) Is a list of qualified assembly and packaging fabrication plants available ?
- b) Are the following information available for qualified assembly and packaging-fabs:
 - name and address
 - name of the supervisor of assembly and packaging fabrication plants
 - identification of the capability manual
 - the technologies and procedures used
 - list of documents and tools delivered?

[G.II.3.6]

- a) Is a list of qualified test laboratories available ?
- b) Is the following information available in respect of qualified test laboratories:
 - name and address
 - name of the supervisor of qualified test laboratories
 - identification of the capability manual
 - the test equipments used
 - list of interfaces, documents and tools used?

[G.II.4] PROCEDURES FOR DESIGN AND VERIFICATION

[G.II.4.1.]

- a) Which recommendations or guide-lines are given to the customer designing part of an IC (e.g. at block level)?