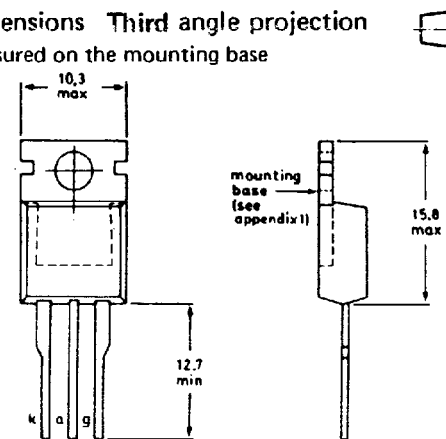


BRITISH STANDARDS INSTITUTION 2, PARK STREET, LONDON, W1A 2BS	BS CECC 50 011-003 CECC 50 011-003 ISSUE 1, OCTOBER 1979
Specification available from:- As shown in PD9002 MULLARD LIMITED Mullard House, Torrington Place, London, WC1E 7HD	 Page 1 of 14 pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH BS CECC 50 000: 1977	MANUFACTURER'S TYPE NUMBER BT151 See PD9002 and CECC 00 200
Outline and dimensions Third angle projection Note: T_{case} is measured on the mounting base  For detail dimensions see IEC 191-2 SO178 Marking information see Page 3	For ordering information see Page 3 GLASS PASSIVATED CASE RATED EUTECTIC BONDED SILICON THYRISTOR PRIMARILY INTENDED FOR USE IN HIGH FATIGUE STRESS APPLICATIONS INVOLVED IN THERMAL CYCLING AND REPEATED SWITCHING. 7.5 A 500 and 650 V PLASTIC ENCAPSULATED ASSESSMENT LEVEL F AND L PLUS ADDITIONAL TESTS

4. LIMITING VALUES

Absolute maximum values which apply over the operating temperature range (see 4.4.) unless otherwise stated.

4.1. Voltage ratings

TABLE 1

BT151 500R BT151 650 R

4.1.1. Crest working reverse voltage	V_{RWM}	400	400	V
4.1.2. Crest working off-state voltage	V_{DWM}	400	400	V
4.1.3. Repetitive peak reverse voltage	V_{RRM}	500	650	V
4.1.4. Repetitive peak off-state voltage	V_{DRM}	500	650	V
4.1.5. Non-repetitive peak reverse voltage	V_{RSM}	500	650	V
4.1.6. Non-repetitive peak off-state voltage	V_{DSM}	500	650	V

4.2. Current ratings

4.2.1. Mean on-state current at $T_{case} 85^{\circ}\text{C}$ (see Fig.1)

In single-phase circuits, sinusoidal 180° conduction angle with resistive load

4.2.2. Repetitive peak on-state current	I_{TRM}	65	A
4.2.3. Continuous (d.c.) on-state current	I_T	12	A

Refer to Qualified Products List PD 9002 and/or CECC 00200 for details of manufacturers approved to this specification.

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4. LIMITING VALUES (contd.)

4.2.4.1. Non-repetitive on-state surge current $t = 10$ ms;
half sinewave $T_{case} = 110^{\circ}\text{C}$, without reapplication of reverse voltage

$I_{TSM(1)}$ 105 A

4.2.4.2. Non-repetitive on-state surge current $t = 10$ ms;
half sinewave $T_{case} = 110^{\circ}\text{C}$, with reapplication of reverse voltage

$I_{TSM(2)}$ 100 A

Note: In both 4.2.4.1. and 4.2.4.2. loss of state control may occur.

4.2.5. Critical rate of rise of on-state current

di/dt 50 A/ μs

4.3. Gate ratings

4.3.3. Peak reverse gate voltage

V_{RGM} 5 V

4.3.5. Peak gate power dissipation

P_{GM} 5 W

4.3.6. Average gate power dissipation

$P_{G(AV)}$ 0.5 W

4.4. Temperature ratings

4.4.1. Maximum case temperature at which the above voltage ratings apply

T_{case} 125 $^{\circ}\text{C}$

4.4.2. Maximum and minimum virtual junction temperature at which
the above voltage and current ratings apply

$T_{(vj)}$ -40 to 110 $^{\circ}\text{C}$

4.4.3. Maximum and minimum storage temperature

$T_{(stg)}$ -40 to 125 $^{\circ}\text{C}$

4.5. Mechanical ratings – See Appendix 1

5. ELECTRICAL CHARACTERISTICS (All at $T_{case} = 25^{\circ}\text{C}$ unless otherwise stated)

5.1. Maximum peak on-state voltage at $I_{TM} = 25$ A
corresponding to $I_{T(AV)} = 7.5$ A

V_{TM} 1.8 V

5.3.1. Maximum peak reverse current at V_{RRM}

$I_{RM(1)}$ 100 μA

5.3.2. Minimum peak reverse current at V_{RRM} $T_{(vj)} = 110^{\circ}\text{C}$

$I_{RM(2)}$ 1 mA

5.5.1. Maximum peak off-state current at V_{DRM}

$I_{DM(1)}$ 100 μA

5.5.2. Maximum peak off-state current at V_{DRM} $T_{(vj)} = 110^{\circ}\text{C}$

$I_{DM(2)}$ 1 mA

5.6. Maximum and minimum holding current

I_H 2 mA min
20 mA max.

5.7. Maximum latching current $V_D = 100$ V
 R_G open circuit

I_L 40 mA

5.8. Minimum gate trigger current

I_{GT} 15 mA

5.9. Minimum gate trigger voltage

V_{GT} 1.5 V

5.10. Minimum gate non-trigger voltage

V_{GD} 250 mV

5.11. Critical rate of rise of off-state voltage

$V_D = V_{DWM}$ $T_{(vj)} = 100^{\circ}\text{C}$

R_{GK} open circuit

R_{GK} 100 Ω

dv/dt 50 V/ μs

dv/dt 200 V/ μs

5.13. Total power dissipation

P_{tot} See Fig.1

5.14. Maximum thermal resistance junction to case

R_{th} 1.3 $^{\circ}\text{C/W}$

6. MARKING

- (1) Each thyristor shall bear the following markings:
 - (a) The type number, e.g., BT151 500R.
 - (b) The factory identification code.
 - (c) The date code.
- (2) Each package containing one or more of these thyristors shall bear all the above marking and in addition
 - (e) The BS CECC specification number.

7. RELATED DOCUMENTS

BS 6001	Sampling procedures and tables for inspection by attributes.
BS E9000	General requirements of electronic components of assessed quality harmonised with the CENELEC Electronic Components Committee system.
PD 9002	Component selection guide.
CECC 00 200	Qualified product list.
BS CECC 50 000	Generic specification for discrete semiconductor devices.

8. ORDERING INFORMATION

Orders for these thyristors shall state

- (1) Quantity
- (2) Manufacturer's type number (see Page 1)
- (3) The CECC specification number
- (4) The assessment level (F or L) required

9. TEST CONDITIONS AND INSPECTION REQUIREMENTS

Samples submitted to tests marked 'D' shall not be accepted for release (see Clause 3.5.6. of BS CECC 50 000).

All tests shall be made at $T_{case} = 25 \pm 5^{\circ}C$ unless otherwise stated.

Marking must withstand all tests of this specification which might change or damage it and must remain legible.

TABLE 2 – INSPECTION REQUIREMENTS

GROUP A – Lot by lot

Examination or test	Ref.	Conditions at $T_{\text{case}} = 25^{\circ}\text{C}$ unless otherwise stated	Inspection requirements					
			Limits		Units	Levels	IL	AQL %
			Min.	Max.				
Subgroup A1						F	1	0.65
Visual inspection	4.2.1.					L	1	0.65
Subgroup A2a						F	11	0.25
Non-operatives						L	11	0.25
Open circuit	4.3.4. T-101	) V_{TM} at (		7	V			
Short circuit		) $I_{\text{TM}} = 25\text{ A}$ (	0.7					
		) R_{GK} open circuit (						
Subgroup A2b						F	11	1.0
Peak on-state voltage V_{TM}	4.3.4. T-101	$I_{\text{TM}} = 25\text{ A}$ $R_{\text{gk}} = \text{open circuit}$		1.8	V	L	11	1.0
Peak reverse current I_{RM1}	4.3.4. T-102	$V_{\text{R}} = V_{\text{RRM}}$ Table 1 $R_{\text{gk}} = \text{open circuit}$ $f = 50\text{ Hz}$		100	μA			
Gate trigger current I_{GT}	4.3.4. T-109	$V_{\text{D}} = 6\text{ V}$ $R_{\text{gk}} = \text{open circuit}$		15	mA			
Gate trigger voltage V_{GT}	4.3.4. T-109	$f = 50\text{ Hz}$		1.5	V			
		oscilloscope method						
Subgroup A3						F	1	2.5
Peak reverse current I_{RM2}	4.3.4. T-102	$V_{\text{R}} = V_{\text{RRM}}$ Table 1 $R_{\text{gk}} = \text{open circuit}$ $f = 50\text{ Hz}$ $T_{\text{case}} = 110^{\circ}\text{C}$		1	mA	L	1	2.5
Peak off-state current I_{DM2}	4.3.4. T-103	$V_{\text{D}} = V_{\text{DRM}}$ Table 1 $R_{\text{gk}} = \text{open circuit}$ $f = 50\text{ Hz}$ $T_{\text{case}} = 110^{\circ}\text{C}$		1	mA			
Subgroup A4						F	S3	2.5
Critical rate of rise of off-state voltage dv/dt	4.3.4. T-112	$V_{\text{D}} = 0.7 \times V_{\text{DRM}}$ Table 1 (exponential rate of rise) $R_{\text{gk}} = \text{open circuit}$ $T_{\text{case}} = 110^{\circ}\text{C}$	50		V/ μs	L	S3	2.5
Gate non-trigger voltage V_{GD}	4.3.4. T-110	$V_{\text{D}} = V_{\text{DRM}}$ Table 1 $R_{\text{gk}} = \text{open circuit}$ $T_{\text{case}} = 110^{\circ}\text{C}$	250		mV			

GROUP B – Lot by lot

Examination or test	Ref.	Conditions at $T_{\text{case}} = 25^{\circ}\text{C}$ unless otherwise stated	Inspection requirements					
			Limits		Units	Levels	IL	AQL %
			Min.	Max.				
Subgroup B1						F	S2	2.5
Major dimensions	4.2.2.	IEC 191-2 SO-178 D E		15.8 10.3	mm mm	L	S2	2.5
Subgroup B4						F	S4	2.5
Solderability	4.4.7	Soldering iron method				L	S4	2.5
Subgroup B5						F	S4	4.0
Rapid change of temperature followed by	4.4.4.	Test Nc $T_A = 0^{\circ}\text{C}$, $T_B = 100^{\circ}\text{C}$				L	na	na
Accelerated damp heat (D)	4.4.2.	Method 1						
Subgroup B8						F	S3	4.0
Electrical endurance	4.5.2.8.	168 (–10, +72 h) $f = 50\text{ Hz}$, stud mounted V_{RWM} Table 1 V_{DWM} Table 1				L	na	na
Post-test end-points for Subgroup B5								
Peak on-state voltage V_{TM}	4.3.4. T-101	$I_{\text{TM}} = 25\text{ A}$ $R_{\text{gk}} = \text{open circuit}$		1.8	V			
Peak reverse current I_{RM2}	4.3.4. T-102	$V_{\text{R}} = V_{\text{RRM}}$ Table 1 $R_{\text{gk}} = \text{open circuit}$ $f = 50\text{ Hz}$ $T_{\text{case}} = 110^{\circ}\text{C}$		1	mA			
Peak off-state current I_{DM2}	4.3.4. T-103	$V_{\text{D}} = V_{\text{DRM}}$ Table 1 $R_{\text{gk}} = \text{open circuit}$ $f = 50\text{ Hz}$ $T_{\text{case}} = 110^{\circ}\text{C}$		1	mA			
Gate trigger current I_{GT}	4.3.4. T-109	$V_{\text{D}} = 6\text{ V}$ $R_{\text{gk}} = \text{open circuit}$ $f = 50\text{ Hz}$		15	mA			