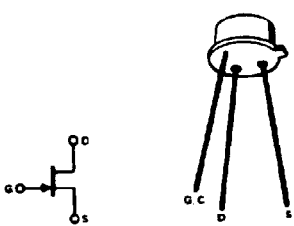


BRITISH STANDARDS INSTITUTION 2, PARK STREET, LONDON W1A 2BS	BS CECC 50 012-017 ISSUE 1 July 1988 Page 1 of 14 pages
Specification available from: As shown in PD9002, CECC 00200 and SILICONIX LTD. MORRISTON SWANSEA SA6 6NE. Telephone (0792) 310100. Telex 48197	 DETAIL SPECIFICATION FOR U308 U309 U310
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH BS CECC 50 000: 1982	SINGLE GATE JUNCTION F.E.T. ORDERING INFORMATION: See clause 7 of this document
1. MECHANICAL DESCRIPTION Drawing not to scale 	2. Semiconductor Material: Silicon Polarity: N-Channel Device type: Junction-gate FET Encapsulation: Hermetically sealed metal can Application: HF amplification Power: Ambient rated 3. LEVEL OF QUALITY ASSESSMENT E
For Detail Dimensions see IEC 191-2 B11 and C22 Marking: See Clause 6 of this document	

4. LIMITING VALUES (Absolute maximum rating system)

These apply over the operating temperature range unless otherwise stated

CECC 50012 Section 2 Reference		SYMBOL	VALUE		
			MIN.	MAX.	UNIT
4.1	Operating temperature range All types	T_{amb}	-55	150	$^{\circ}\text{C}$
4.2	Storage temperature range All types	T_{stg}	-65	200	$^{\circ}\text{C}$
4.3	Drain - source voltage All types	V_{DSX}	-	25	V
4.4	Gate - source reverse voltage All types	V_{GSR}	-	25	V
4.5	Gate - drain reverse voltage All types	$-V_{GDO}$	-	25	V
4.6	Gate current All types	I_{GF}	-	20	mA
4.7	Drain current (pulsed, 2 ms)	I_D	-	60	mA
			-	30	
			-	60	
4.8.1	Power dissipation ($T_{amb} = 25^{\circ}\text{C}$) (derate linearly at the rate of $4.0 \text{ mW}/^{\circ}\text{C}$)	P_{tot}	-	500	mW

Refer to current Qualified Products List CECC 00 200 or PD 9002 for details of manufacturers approved to this specification.

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5. CHARACTERISTICS

 $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated.

* indicates verified in inspection testing clause 9.

CECC 50012 Section 2 Reference	PARAMETER AND TEST CONDITIONS	VALUE			
		SYMBOL	MIN	MAX	UNITS
5.1*	Gate reverse current All types $V_{GS} = -15.0 \text{ V}$ $V_{DS} = 0 \text{ V}$	$-I_{GSS(1)}$	-	150	pA
5.2*	Gate reverse current All types $V_{GS} = -15.0 \text{ V}$ $V_{DS} = 0 \text{ V}$ $T_{amb} = 150^{\circ}\text{C}$	$-I_{GSS(2)}$	-	150	nA
5.3*	Gate source cut-off voltage $V_{DS} = 10.0 \text{ V}$ U308 $I_D = 1.0 \text{ nA}$ U309 U310	$-V_{GS(OFF)}$	1.0	6.0	V
			1.0	4.0	V
			2.5	6.0	V
5.4*	Drain current (pulsed) (Note 1) $V_{DS} = 10.0 \text{ V}$ U308 $V_{GS} = 0 \text{ V}$ U309 U310	I_{DSS}	12	60	mA
			12	30	mA
			12	60	mA
5.7*	Y-parameters $V_{DG} = 10 \text{ V}$ $I_D = 10 \text{ mA}$				
5.7.1	$f = 105.0 \text{ MHz}$ All types	$\text{Re}(Y_{11s})$	-	25	mS
		$\text{Im}(Y_{11s})$	-	5	mS
	$f = 450.0 \text{ MHz}$	$\text{Re}(Y_{11s})$	-	30	mS
		$\text{Im}(Y_{11s})$	-	15	mS
5.7.2	$f = 105.0 \text{ MHz}$ All types	$\text{Re}(Y_{22s})$	-	0.3	mS
		$\text{Im}(Y_{22s})$	-	3.0	mS
	$f = 450.0 \text{ MHz}$	$\text{Re}(Y_{22s})$	-	1.0	mS
		$\text{Im}(Y_{22s})$	-	15.0	mS

Note 1: Pulse duration 2 ms duty cycle $\leq 1.5\%$

5. **CHARACTERISTICS** $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated.

* indicates verified in inspection testing clause 9.

CECC 50012 Section 2 Reference	PARAMETER AND TEST CONDITIONS	VALUE			
		SYMBOL	MIN	MAX	UNITS
5.7.3	$f = 105.0 \text{ MHz}$ All types	$\text{Re}(Y_{21s})$	-10	-25	mS
		$\text{Im}(Y_{21s})$	0	3.0	mS
	$f = 450.0 \text{ MHz}$	$\text{Re}(Y_{21s})$	-10	-25	mS
		$\text{Im}(Y_{21s})$	0	10	mS
5.7.4	$f = 105.0 \text{ MHz}$ All types	$\text{Re}(Y_{12s})$	-	-0.5	mS
		$\text{Im}(Y_{12s})$	-	-0.2	mS
	$f = 450.0 \text{ MHz}$	$\text{Re}(Y_{12s})$	-	2.0	mS
		$\text{Im}(Y_{12s})$	-	-0.8	mS
5.8*	Noise factor All types	F			
	$V_{DG} = 10.0 \text{ V}$ $f = 105.0 \text{ MHz}$		-	2.0	dB
	$I_D = 10.0 \text{ mA}$ $f = 450.0 \text{ MHz}$		-	3.5	dB
5.9 *	Power gain All types	G_p			
	$V_{DG} = 10.0 \text{ V}$ $f = 105.0 \text{ MHz}$		14	-	dB
	$I_D = 10.0 \text{ mA}$ $f = 450.0 \text{ MHz}$		10	-	dB

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6. MARKING

- (1) Each transistor shall bear the following marking:
 - (a) The manufacturer's type number (see Table 1)
 - (b) The factory identification code
 - (c) The date code
- (2) Each package containing one or more of these transistors shall bear all of the above markings except (b) and in addition:
 - (d) this detail specification number (see Table 1).

- (3) Interpretation of marking information: XXXXXX E Y

Device type number	_____	_____	_____
Quality Assessment Level	_____	_____	_____
Screening sequence	_____	_____	_____

KEY:

Quality Assessment Level
(CECC 50 000)

E

Screening Sequence: Y
(CECC 50 000)

BLANK	No screening
A	Sequence A
B	Sequence B
C	Sequence C
D	Sequence D

7. ORDERING INFORMATION

The following minimum information is necessary to order a specific device, unless otherwise specified:

- Precise type number.
- CECC reference of detail specification with issue number and/or date when relevant.
- Level of quality assessment as defined in Appendix IIA of CECC 50 000, and, if required, screening sequence as defined in Appendix VI of CECC 50 000.
- Any other particulars.

TABLE 1

ORDER TYPE	SPECIFICATION NUMBER				MARKING
BS U308X - E to	BS CECC 50 012-017	Issue 1	dated July 1988		U308E - Y
BS U309X - E to	BS CECC 50 012-017	Issue 1	dated July 1988		U309E - Y
BS U310X - E to	BS CECC 50 012-017	Issue 1	dated July 1988		U310E - Y

8. RELATED DOCUMENTS

- CECC 00 007 Basic specifications: Sampling plans and procedures for inspection by attributes.
- CECC 00 100 CECC Basic Rules
- CECC 50 000 Harmonised system of Quality Assessment for electronic components:
Generic specification: Discrete semiconductor devices.
- IEC 68-2 Basic environmental testing procedures.
- IEC 191-2 Mechanical standardisation of semiconductor devices.

9. TEST CONDITIONS AND INSPECTION REQUIREMENTS

These are given in the following tables, where the values and exact test conditions are specified as required by the relevant text in CECC 50 000.

