

BRITISH STANDARDS INSTITUTION 2, PARK STREET, LONDON W1A 2BS	BS CECC 50 012-023 ISSUE 1 July 1988
Specification available from: As shown in PD9002, CECC 00200 and SILICONIX LTD. MORRISTON SWANSEA SA6 6NE. Telephone (0792) 310100. Telex 48197	Page 1 of 14 pages DETAIL SPECIFICATION FOR 2N4416 2N4416A
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH BS CECC 50 000: 1982	SINGLE GATE JUNCTION F.E.T. ORDERING INFORMATION: See clause 7 of this document
1. MECHANICAL DESCRIPTION Drawing not to scale  For Detail Dimensions see IEC 191-2 B12 and C7. Marking: See Clause 6 of this document	2. Semiconductor Material: Silicon Polarity: N-Channel Device type: Junction-gate FET Encapsulation: Hermetically sealed metal can Application: HF amplification Power: Ambient rated 3. LEVEL OF QUALITY ASSESSMENT E

4. LIMITING VALUES (Absolute maximum rating system)

These apply over the operating temperature range unless otherwise stated

CECC 50012 Section 2 Reference		SYMBOL	VALUE		
			MIN.	MAX.	UNIT
4.1	Operating temperature range	T_{amb}	-55	150	$^{\circ}\text{C}$
4.2	Storage temperature range	T_{stg}	-65	200	$^{\circ}\text{C}$
4.3	Drain - source voltage	V_{DSX}	-	30	V
	2N4416			35	
4.4	Gate - source reverse voltage	V_{GSR}	-	30	V
	2N4416A			35	V
4.5	Gate - drain reverse voltage	$-V_{GDR}$	-	30	V
	2N4416			35	V
4.6	Gate current	I_G	-	10	mA
4.7	Drain current (pulsed, 300 μs)	I_D	-	15	mA
4.8	Total power dissipation ($T_{amb} = 25^{\circ}\text{C}$) (derate linearly at the rate of 1.7 mW/ $^{\circ}\text{C}$)	P_{tot}	-	300	mW

Refer to current Qualified Products List CECC 00 200 or PD 9002 for details of manufacturers approved to this specification



Documents

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5. **CHARACTERISTICS** $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated.

* indicates verified in inspection testing clause 9.

CECC 50012 Section 2 Reference	PARAMETER AND TEST CONDITIONS	VALUE			
		SYMBOL	MIN	MAX	UNITS
5.1*	Gate reverse current All types $-V_{GS} = 20.0\text{ V}$ $V_{DS} = 0\text{ V}$	$-I_{GSS(1)}$	-	0.1	nA
5.2*	Gate reverse current All types $-V_{GS} = 20.0\text{ V}$ $V_{DS} = 0\text{ V}$ $T_{amb} = 150^{\circ}\text{C}$	$-I_{GSS(2)}$	-	0.1	μA
5.3*	Gate source cut-off voltage $V_{DS} = 15.0\text{ V}$ $I_D = 1\text{ nA}$ 2N4416 2N4416A	$-V_{GS(OFF)}$	-	6.0	V
			2.5	6.0	V
5.4*	Drain current (Note 1) All types $V_{DS} = 15.0\text{ V}$ $V_{GS} = 0\text{ V}$	I_{DSS}	5.0	15.0	mA
5.7*	Y-parameters $V_{DS} = 15\text{ V}$ $V_{GS} = 0\text{ V}$				
5.7.1	$f = 100.0\text{ MHz}$ All types $f = 400.0\text{ MHz}$	$\text{Re}(Y_{11s})$	-	0.1	mS
		$\text{Im}(Y_{11s})$	-	2.5	mS
		$\text{Re}(Y_{11s})$	-	1.0	mS
		$\text{Im}(Y_{11s})$	-	10.0	mS
5.7.2	$f = 100.0\text{ MHz}$ All types $f = 400.0\text{ MHz}$	$\text{Re}(Y_{22s})$	-	0.075	mS
		$\text{Im}(Y_{22s})$	-	1.0	mS
		$\text{Re}(Y_{22s})$	-	0.3	mS
		$\text{Im}(Y_{22s})$	-	4.0	mS
5.7.3	$f = 100.0\text{ MHz}$ All types $f = 400.0\text{ MHz}$	$\text{Re}(Y_{21s})$	4.0	15.0	mS
		$\text{Im}(Y_{21s})$	0	-2.0	mS
		$\text{Re}(Y_{21s})$	4.0	15.0	mS
		$\text{Im}(Y_{21s})$	-1.0	-4.0	mS

Note 1: Pulse test duration 300 μs , Duty Cycle $\leq 5\%$

5. CHARACTERISTICS

 $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated.

* indicates verified in inspection testing clause 9.

CECC 50012 Section 2 Reference	PARAMETER AND TEST CONDITIONS	VALUE			
		SYMBOL	MIN	MAX	UNITS
5.7.4	$f = 100.0 \text{ MHz}$ All types	$\text{Re } (Y_{12s})$	-	-0.02	mS
		$\text{Im } (Y_{12s})$	-	-0.6	mS
	$f = 400.0 \text{ MHz}$	$\text{Re } (Y_{12s})$	-	-0.3	mS
		$\text{Im } (Y_{12s})$	-	-4.0	mS
5.8*	Noise factor $V_{DS} = 15.0 \text{ V}$ $I_D = 5.0 \text{ mA}$ $R_G = 1.0 \text{ k}\Omega$ $f = 100 \text{ MHz}$ Bandwidth = 5 MHz All types	F	-	2.0	dB
	Noise factor $V_{DS} = 15.0 \text{ V}$ $I_D = 5.0 \text{ mA}$ $R_G = 1.0 \text{ k}\Omega$ $f = 400 \text{ MHz}$ Bandwidth = 5 MHz All types	F	-	4.0	dB
5.9*	Common-source power gain $V_{DS} = 15.0 \text{ V}$ $I_D = 5.0 \text{ mA}$ $f = 100 \text{ MHz}$ All types	G_p	18	-	dB
	Common-source power gain $V_{DS} = 15.0 \text{ V}$ $I_D = 5.0 \text{ mA}$ $f = 400 \text{ MHz}$ All types	G_p	10	-	dB

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6. **MARKING**

- (1) Each transistor shall bear the following marking:
 - (a) The manufacturer's type number (see Table 1)
 - (b) The factory identification code
 - (c) The date code
- (2) Each package containing one or more of these transistors shall bear all of the above markings except (b) and in addition:
 - (d) this detail specification number (see Table 1).

- (3) Interpretation of marking information: XXXXXX E Y

Device type number _____

Quality Assessment Level _____

Screening sequence _____

KEY:

Quality Assessment Level
(CECC 50 000)

E

Screening Sequence
(CECC 50 000:1982 APPENDIX VI)

BLANK

No screening

A

Sequence A

B

Sequence B

C

Sequence C

D

Sequence D

7. **ORDERING INFORMATION**

The following minimum information is necessary to order a specific device, unless otherwise specified:

- Precise type number.
- CECC reference of detail specification with issue number and/or date when relevant.
- Level of quality assessment as defined in Appendix IIA of CECC 50 000, and, if required, screening sequence as defined in Appendix VI of CECC 50 000.
- Any other particulars.

TABLE 1

ORDER TYPE	SPECIFICATION NUMBER			MARKING
BS 2N4416E-Y to	BS CECC 50 012-023	Issue 1	dated July 1988	2N4416E - Y
BS 2N4416AE-Y to	BS CECC 50 012-023	Issue 1	dated July 1988	2N4416AE - Y

8. RELATED DOCUMENTS

CECC 00 007	Basic specifications: Sampling plans and procedures for inspection by attributes.
CECC 00 100	CECC Basic Rules
CECC 50 000	Harmonised system of Quality Assessment for electronic components: Generic specification: Discrete semiconductor devices.
IEC 68-2	Basic environmental testing procedures.
IEC 191-2	Mechanical standardisation of semiconductor devices.

9. TEST CONDITIONS AND INSPECTION REQUIREMENTS

These are given in the following tables, where the values and exact test conditions are specified by the relevant text in CECC 50 000.