

BRITISH STANDARDS INSTITUTION
2, PARK STREET, LONDON, W1A 2BS

BS CECC 50012-026
ISSUE 1 APRIL 1984



ELECTRONIC COMPONENT OF ASSESSED QUALITY
IN ACCORDANCE WITH:
CECC 50000, Issue.

Page 1 of 14 pages

SILICONIX LIMITED
MORRISTON (UK), SA6 6NE
Tel: (0792) 74681 Telex 48197

DETAIL SPECIFICATION FOR:

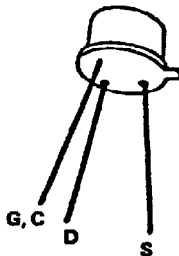
2N5432
2N5433
2N5434

SINGLE GATE JUNCTION F.E.T.

ORDERING INFORMATION:

See clause 7 of this document

1. MECHANICAL DESCRIPTION



2.

Semiconductor Material	: Silicon
Polarity	: N-Channel
Device type	: Junction-gate
Encapsulation	: Hermetically sealed metal can
Application	: Switching
Power	: Ambient rated

3. LEVELS OF QUALITY ASSESSMENT

E, F and L

For Detail Dimensions See IEC 191-2 B4C and C4
Marking: See Clause 6 of this document

4. LIMITING VALUES (Absolute maximum rating system)

These apply over the operating temperature range unless otherwise stated.

CECC 50012 Section 3 Reference		SYMBOL	VALUE		
			MIN.	MAX.	UNIT
4.1	Operation temperature range All types	T_{amb}	-65	150	$^{\circ}\text{C}$
4.2	Storage temperature range All types	T_{stg}	-65	150	$^{\circ}\text{C}$
4.3	Drain - source voltage All types	V_{DSS}	-	25	V
4.4	Gate - source voltage All types	V_{GSR}	-	-25	V
4.5	Gate - drain reverse voltage with source O/C All types	V_{GDO}	-	-25	V
4.6	Gate current All types	I_{GF}	-	100	mA
4.7	Drain current - continuous $T_{amb} = 25^{\circ}\text{C}$ All types	I_D	-	400	mA
4.8	Power dissipation ($T_{amb} = 25^{\circ}\text{C}$) (derate linearly at the rate of $2.3 \text{ mW}/^{\circ}\text{C}$)	P_{tot}	-	300	mW

See the relevant Qualified Products List PD9002 and/or CECC 00200 for availability of components made to this specification.

5. CHARACTERISTICS

$T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated.

† Indicates verified in inspection testing clause 9.

CECC 500 12 Section 3 Reference	PARAMETER AND TEST CONDITIONS	Symbol	Min.	Max.	Units
5.1 [†]	Gate reverse current $V_{GSR} = 15\text{ V}$ $V_{DS} = 0\text{ V}$ All types	$I_{GSS(1)}$	—	200	pA
5.2 [†]	Gate reverse current $V_{GSR} = 15\text{ V}$ $V_{DS} = 0\text{ V}$ $T_{amb} = 150^{\circ}\text{C}$ All types	$I_{GSS(2)}$	—	200	nA
5.3 [†]	Gate-source cut-off voltage $V_{DS} = 5\text{ V}$ 2N5432 $I_D = 3\text{ nA}$ 2N5433 2N5434	$V_{GS(OFF)}$	4 3 1	10 9 4	V V V
5.4 [†]	Drain current (pulsed) $V_{DS} = 15\text{ V}$ 2N5432 $V_{GS} = 0\text{ V}$ 2N5433 2N5434	I_{DSS}	150 100 30	— — —	mA mA mA
5.7 [†]	Drain cut-off current $V_{DS} = 5\text{ V}$ All types	I_{DSX}	—	200	pA
5.8 [†]	Static on-state voltage $V_{GS} = 0\text{ V}$ $I_D = 10\text{ mA}$ 2N5432 $V_{GS} = 0\text{ V}$ $I_D = 10\text{ mA}$ 2N5433 $V_{GS} = 0\text{ V}$ $I_D = 10\text{ mA}$ 2N5434	$V_{DS(ON)}$	— — —	50 70 100	mV mV mV

5. CHARACTERISTICS (Contd.) $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated.

† Indicates verified in inspection testing clause 9.

CECC 50012 Section 3 Reference	PARAMETER AND TEST CONDITIONS	Symbol	Min.	Max.	Units
5.9.1 [†]	Input capacitance $V_{GSR} = 10\text{ V}$ $f = 1\text{ MHz}$ All types	C_{11ss}	—	30	pF
5.9.2 [†]	Output capacitance $V_{GS} = 10\text{ V}$ $f = 1\text{ MHz}$ All types	C_{22ss}	—	20	pF
5.9.3 [†]	Reverse transfer capacitance $V_{GSR} = 10\text{ V}$ $f = 1\text{ MHz}$ All types	C_{12ss}	—	15	pF
SEE SWITCHING TIME TEST CIRCUIT, APPENDIX II					
5.10 [†]	Turn-ON delay time All types	$t_{d(ON)}$	—	4	ns
5.10 [†]	Rise time All types	t_r	—	1	ns
5.10 [†]	Turn-OFF delay time All types	$t_{d(OFF)}$	—	6	ns
5.10 [†]	Fall time All types	t_f	—	30	ns

6. MARKING

- 1) Each transistor shall bear the following marking:
 - a) The manufacturer's type number (See Table 1).
 - b) The factory identification code.
 - c) The date code.
- 2) Each package containing one or more of these transistors shall bear all the above markings except (b) and in addition
 - d) This detail specification number (See Table 1).

- 3) Interpretation of marking information

	XXXXXX	X	Y
Device Type No.			
Quality Assessment Level			
Screening Sequence			

KEY:

Quality Assessment Level
(CECC 50000 ISSUE III APPENDIX IIA)

E
F
L

Screening Sequence
(CECC 50000 ISSUE III APPENDIX VI)

BLANK
A
B
C
D

No Screening
Sequence A
Sequence B
Sequence C
Sequence D

7. ORDERING INFORMATION

The following minimum information is necessary to order a specific device, unless otherwise specified:

- precise type number
- CECC reference of detail specification with issue number and/or date when relevant
- level of quality assessment as defined in Appendix II A of CECC 50000, and, if required, screening sequence as defined in Appendix VI of CECC 50000
- any other particulars.

TABLE 1

ORDER TYPE	SPECIFICATION NUMBER			MARKING
BS 2N5432X – Y to	BS CECC 50012-026	Issue 1	dated April 1984	2N5432X – Y
BS 2N5433X – Y to	BS CECC 50012-026	Issue 1	dated April 1984	2N5433X – Y
BS 2N5434X – Y to	BS CECC 50012-026	Issue 1	dated April 1984	2N5434X – Y

8. RELATED DOCUMENTS

BS 6001	Sampling procedures and tables for inspection by attributes.
BSE 9000	General requirements for electronic components of assessed quality.
BS CECC 50000	Generic specification for discrete semiconductor devices.
CECC 00200	Qualified products list.
IEC 147	Essential ratings and characteristics of semiconductor devices and general principles of measuring methods.
IEC 191-2	Mechanical standardisation of semiconductor devices – Dimensions.
PD 9002	BS 9000 Component selection guide.

9. TEST CONDITIONS AND INSPECTION REQUIREMENTS

These are given in the following tables, where the values and exact test conditions to be used should be specified as required for a given type, and as required by the relevant text in CECC 50000.

GROUP A

Lot by lot

All tests are non-destructive (3.5.6 of CECC 50000)

Clause numbers are made with respect to CECC 50000 unless otherwise stated.

EXAMINATION OR TEST AND REFERENCE	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated	INSPECTION REQUIREMENTS							
		LIMITS			LEVELS				
		Min.	Max.	Unit	E		F + L		
					IL	AQL	IL	AQL	
<u>Subgroup A1</u> Visual inspection (4.2.1)	4.2.1					I	0.65%	I	0.65%
<u>Subgroup A2a</u> Non-operatives (4.3.4 T.071) $I_{GSS}(1)$ $V_{GS}(\text{OFF})$ (4.3.4 T.075)	$V_{GSR} = 15\text{ V}$ $V_{DS} = 0\text{ V}$ All types $V_{DS} = 6\text{ V}$ 2N5432 $I_D = 3\text{ nA}$ 2N5433 2N5434					II	0.15%	II	0.15%

* Pulse width 300 μs , duty cycle $\leq 3\%$.