

UTE

Spécification française harmonisée
Système CENELEC d'assurance de la qualité
12, Place des Etats-Unis
75783 PARIS CEDEX 16

Téléphone : (1) 47 23 72 57

Télex : 620434F

CECC 90 101-023

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Page 0

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COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :
*ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :*

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 101 (NF C 86-213)

UTE C 86-213/B 43

Adoptée le 16 novembre 1987

BS9420 F010-012

BS9420 F028-030

BS9420 F938-944

Issue 3

May, 1978

DESSIN ET DIMENSIONS :
OUTLINE AND DIMENSIONS :

CEI 191-2 - Types 050 G 04 - 050 G 03
IEC 191-2 - Types 050 G 04 - 050 G 03

Référence française : F 105 - F 105A
French reference :

IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS

Voir Tableau II
See Table II

SPECIFICATION PARTICULIERE POUR
MICROSTRUCTURES LOGIQUES SELON FS 90 101
DETAIL SPECIFICATION FOR DIGITAL INTEGRATED CIRCUITS IN ACCORDANCE WITH FS 90 101

54/64/74 72**BASCULE BISTABLE J-K**

**MASTER-SLAVE BISTABLE
WITH SEPARATE PRESET AND CLEAR**

TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :

Circuit monolithique bipolaire au silicium, boîtiers
avec ou sans cavité.

*Silicon monolithic bipolar integrated circuit,
cavity/non-cavity packages.*

NIVEAUX D'ASSURANCE DE QUALITE : P, Y, L
ASSESSMENT LEVELS :

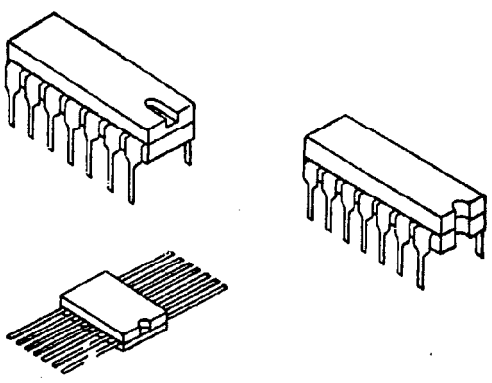
AMENDMENTS TO THE FOLLOWING CLAUSES

- § 2 - Add :
Most negative low level input voltage at an input current : $I_{IKB} = -12 \text{ mA}$, $V_{IKB} = -1,5 \text{ V}$
- § 3 To be replaced by CECC 90 000/3 § 2.5
- § 4 To be deleted
- § 5 To be replaced by CECC 90 000/3 § 2.6
- § 6 To be replaced by CECC 90 000/3 § 4.10.1
- § 7 All inspection level and AQL are those specified in 90 100/3.
Replace A3b by A4a, A3c by A4b, A4 by A5.
Add A8 of 90 100/3 (Assessment level P only).
Apply to A2 extreme temperature testing with A7a/A7b 90 000 inspection requirements.
For groups B, C, D, apply 90 100/3.
Sub-groups A6, A7 : not applicable.

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.
Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.

**Documents**

Document Sharing Hub

BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON W1A 2BS	BS 9420 F010-012 BS 9420 F028-030 BS 9420 F938-944 ISSUE 3, MAY 1978
ELECTRONIC COMPONENTS OF ASSESSED QUALITY: DETAIL SPECIFICATION	
Outlines not to scale  For detail dimensions: 14 Lead Flat-Pack – see Appendix I 14 Lead Dual in-line – see BS 3934 SO-87B	SILICON MONOLITHIC TTL J – K MASTER-SLAVE BISTABLE WITH SEPARATE PRESET AND CLEAR FULL ASSESSMENT LEVEL AND APPLICATION CATEGORIES S1, S2, S3 and S4 TYPES: 5472 6472 7472 See clause 5 CERAMIC/GLASS HERMETICALLY SEALED ENCAPSULATION OR DUAL IN-LINE PLASTIC ENCAPSULATION

1. Limiting conditions of use (not for inspection purposes).

Absolute values (non-simultaneous)				Units
V_{CC}	Maximum continuous positive supply voltage		7.0	V
	Maximum continuous negative supply voltage		0.5	V
	Maximum continuous positive input voltage		5.5	V
	Maximum continuous negative input voltage		0.5	V
$-I_{IL}$	Maximum input current	(J or K inputs)	1.6	mA
		(Preset, Clock or Clear inputs)	3.2	mA
	Maximum reverse input current		1.0	mA
T_{amb}	Ambient operating temperature range	5472	–55 to +125	°C
		6472	–40 to +85	°C
		7472	0 to +70	°C
	Storage temperature range		–65 to +150	°C
T_{stg}	Shock (0.5 ms duration)		14 700	m/s ²
	Vibration		196	m/s ²

Copies of this specification are available from manufacturers listed in the Qualified Products List, Part 1 of PD 9002.

BS 9420 F010 to 012
BS 9420 F028 to 030
BS 9420 F938 to 944
Issue 3, May 1978

2. Recommended conditions of use and associated characteristics (not for inspection purposes)
Over the full ambient operating temperature range unless otherwise stated.

			Min.	Max.	Units
V_{CC}	Positive supply voltage	5472	4.5	5.5	V
		6472 & 7472	4.75	5.25	V
I_{CC}	Total supply current per package			20.0	mA
V_{IH}	HIGH state input voltage	5472	2.0	5.5	V
		6472 & 7472	2.0	5.25	V
V_{IL}	LOW state input voltage		0	0.8	V
V_{OH}	HIGH state output voltage		2.4		V
V_{OL}	LOW state output voltage			0.4	V
$I_{IH(1)}$	HIGH state input current, $V_{IN} = V_{IH}$ maximum value			1.0	mA
$I_{IH(2)}$	HIGH state input current, $V_{IN} = 2.4V$ (J or K inputs)			40.0	μA
	(Preset, Clock or Clear inputs)			80.0	μA
$-I_{IL}$	LOW state input current, $V_{IN} = 0.4V$ (J or K inputs)			1.6	mA
	(Preset, Clock or Clear inputs)			3.2	mA
$-I_{OH}$	HIGH state output current			400.0	μA
I_{OL}	LOW state output current			16.0	mA
$-I_{OS}$	Output short-circuit current	5472	20.0	57.0	mA
		6472 & 7472	18.0	57.0	mA
t_{PHL}	HIGH state to LOW state propagation time at 25°C*			40.0	ns
t_{PLH}	LOW state to HIGH state propagation time at 25°C*			25.0	ns
$t_{p(clock)}$	Duration of clock pulse (Clock HIGH)		20.0		ns
	(Clock LOW)		47.0		ns
$t_{p(preset)}$	Duration of preset pulse		25.0		ns
$t_{p(clear)}$	Duration of clear pulse		25.0		ns
t_{set-up}	Minimum set-up time w.r.t. positive edge of clock		0		ns
$f_{(clock)}$	Clock frequency			> 15.0	MHz
$t_{(hold)}$	Minimum hold time w.r.t. negative edge of clock		0		ns

*See subgroup A4 for details.

Table 1
Function table

Inputs (Before clock pulse)		Outputs (After clock pulse)	
J	K	Q output	$\bar{Q}$ output
L	L	Q_n	$\bar{Q}_n$
L	H	L	H
H	L	H	L
H	H	$\bar{Q}_n$	Q_n

Q_n = Output state at Q before clock pulse

When a LOW input is applied directly to the Clear input, output Q is set to LOW. This input is independent of the clock.

When a LOW input is applied to the Preset input, output Q is set to HIGH. This input is independent of the clock.

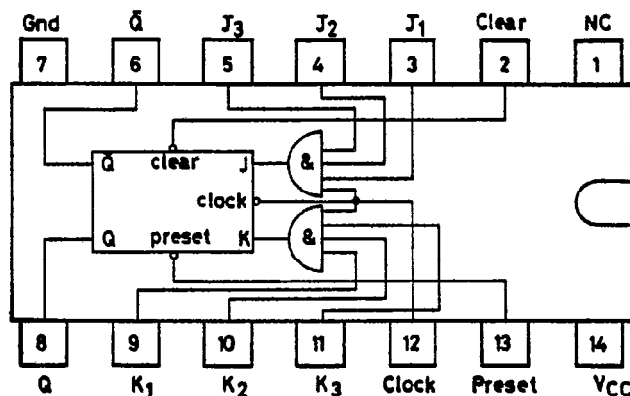
The device is triggered by the negative edge of the clock.

BS 9420 F010 to 012
BS 9420 F028 to 030
BS 9420 F938 to 944
Issue 3, May 1978

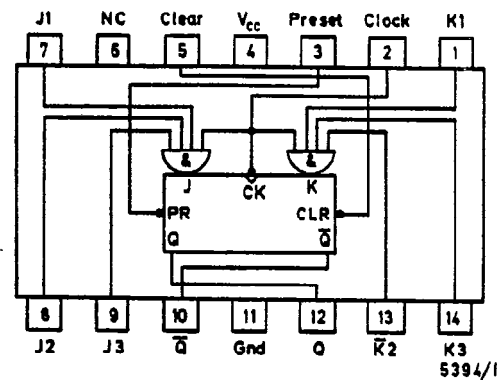
Table II

Logic diagrams and connections

DUAL IN-LINE



FLAT-PACK



3. Marking

(1) Each integrated circuit shall bear the following markings:

- Terminal identification.
- The manufacturer's type number.
- The factory identification code.
- The date code.

(2) Each package containing one or more of these circuits shall bear the markings 'b', 'c' and 'd' above and in addition:

- The BS detail specification number e.g., BS9420 F010.

4. Related documents

BS 3934 'Dimensions of semiconductor devices',
BS 6001 'Sampling procedures and tables for inspection by attributes',
BS 9000 'General requirements for electronic components of assessed quality',
PD 9002 'Qualified products list for electronic components of assessed quality',
BS 9400 'Integrated electronic circuits of assessed quality: Generic data and methods of test'.

5. Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturer's integrated circuit type and package identification as detailed in PD 9002 to BS 9420 F... as defined below.

TYPE		APPLICATION CATEGORY				FULL ASSESSMENT LEVEL
		S1	S2	S3	S4	
CERAMIC Dual in-line and Flat-Pack	5472	F028	F029	F030	F938	F010
	6472	★	F939	F940	F941	F011
	7472	★	F942	F943	F944	F012
PLASTIC Dual in-line	5472	★	★	★	★	F010
	6472	★	★	★	★	F011
	7472	★	★	★	★	F012

★ = Not available at the present time.

BS 9420 F010 to 012
BS 9420 F028 to 030
BS 9420 F938 to 944
Issue 3, May 1978

6. Screening procedures

Production batches submitted for 100% screening shall be rejected if more than a total of 10% of the devices in the batch fail the electrical test requirements subsequent to the burn-in screen 1.2.9.2 in categories S1, S2 and S4.

