

UTE

Spécification française harmonisée
Système CENELEC d'assurance de la qualité
12, Place des Etats-Unis
75783 PARIS CEDEX 16

Téléphone : (1) 47 23 72 57 Téléc : 620434F

CECC 90 101-025

EDITION 1 - Novembre 1987
ISSUE 1 - November 1987



Page 0

Nombre total de pages : 16
Total number of pages :

**COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :**

**ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :**

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 101 (NF C 86-213)

UTE C 86-213/B 45

Adoptée le 16 novembre 1987

BS9420 F016 to F018

BS9420 F034 to F036

BS9420 F097 to F103

Issue 2

July, 1977

**DESSIN ET DIMENSIONS ;
OUTLINE AND DIMENSIONS :**

CEI 191-2 - Types 050 G 04 - 050 G 03
IEC 191-2 - Types 050 G 04 - 050 G 03

Référence française : F 105 - F 105A
French reference :

**IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS**

Voir Tableau II
See Table II

**SPECIFICATION PARTICULIERE POUR
MICROSTRUCTURES LOGIQUES SELON FS 90 101
DETAIL SPECIFICATION FOR DIGITAL INTEGRATED
CIRCUITS IN ACCORDANCE WITH FS 90 101**

54/64/74 74

BASCULE BISTABLE TYPE D $\overline{R}$ $\overline{S}$

**DUAL D-TYPE BISTABLE
WITH PRESET AND CLEAR**

**TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :**

Circuit monolithique bipolaire au silicium, boîtiers
avec ou sans cavité.

Silicon monolithic bipolar integrated circuit,
cavity/non-cavity packages.

**NIVEAUX D'ASSURANCE DE QUALITE : P, Y, L
ASSESSMENT LEVELS :**

AMENDMENTS TO THE FOLLOWING CLAUSES

§ 2 - Add :

Most negative low level input voltage at an input current : $I_{IKB} = -12 \text{ mA}$, $V_{IKB} = -1,5 \text{ V}$

§ 3 To be replaced by CECC 90 000/3 § 2.5

§ 4 To be deleted

§ 5 To be replaced by CECC 90 000/3 § 2.6

§ 6 To be replaced by CECC 90 000/3 § 4.10.1

§ 7 All inspection level and AQL are those specified in 90 100/3.

Replace A3b by A4a, A3c by A4b, A4 by A5.

Add A8 of 90 100/3 (Assessment level P only).

Apply to A2 extreme temperature testing with A7a/A7b 90 000 inspection requirements.

For groups B, C, D, apply 90 100/3.

Sub-groups A6, A7 : not applicable.

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.

Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.



Documents

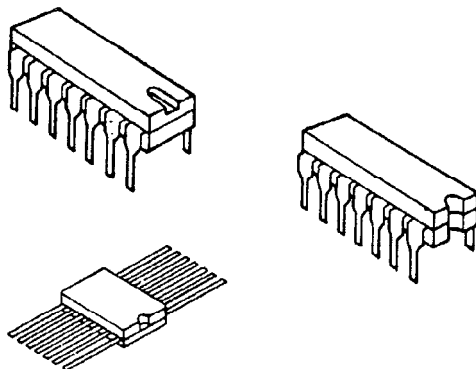
Document Sharing Hub

BRITISH STANDARDS INSTITUTION

2, PARK STREET,
LONDON, W1A 2BSBS9420 F016 to F018
BS9420 F034 to F036
BS9420 F097 to F103
ISSUE 2, JULY, 1977

ELECTRONIC COMPONENTS OF ASSESSED QUALITY: DETAIL SPECIFICATION

Outlines not to scale.

For details dimensions:
14 Lead Flat-Pack — see Appendix I
14 Lead Dual in-line — BS 3934 SO-87BSILICON MONOLITHIC TTL
DUAL D-TYPE BISTABLE CIRCUITS
WITH PRESET AND CLEARFULL ASSESSMENT LEVEL AND
APPLICATION CATEGORIES
S1, S2, S3 AND S4

TYPES

5474
6474
7474

See Clause 5

CERAMIC/GLASS HERMETICALLY
SEALED ENCAPSULATION OR
DUAL IN-LINE PLASTIC
ENCAPSULATION

1. Limiting conditions of use (not for inspection purposes)

Absolute values (non-simultaneous)

			Units
V_{CC}	Maximum continuous positive supply voltage	7.0	V
	Maximum continuous negative supply voltage	0.5	V
	Maximum continuous positive input voltage	5.5	V
	Maximum continuous negative input voltage	0.5	V
$-I_{IL}$	Maximum input current (D or preset inputs)	1.6	mA
	(Clock or Clear inputs)	3.2	mA
	Maximum reverse input current	1.0	mA
T_{amb}	Ambient operating temperature range	5474	-55 to +125 °C
		6474	-40 to + 85 °C
		7474	0 to + 70 °C
T_{stg}	Storage temperature range		-65 to +150 °C
	Shock (0.5 ms duration)	14 700	m/s ²
	Vibration	196	m/s ²

Copies of this specification are available from manufacturers
listed in the Qualified Products List Part 1, of PD 9002.

BS 9420 F016 to F018
BS 9420 F034 to F036
BS 9420 F097 to F103
Issue 2, July, 1977

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

Over the full ambient operating temperature range unless otherwise stated.

			Min.	Max.	Units
V_{CC}	Positive supply voltage	5474	4.5	5.5	V
		6474 & 7474	4.75	5.25	V
V_{IH}	HIGH state input voltage	5474	2.0	5.5	V
		6474 & 7474	2.0	5.25	V
I_{CC}	Total supply current per package at V_{CC} maximum value			30.0	mA
V_{OH}	HIGH state output voltage		2.4		V
V_{IL}	LOW state input voltage		0	0.8	V
V_{OL}	LOW state output voltage			0.4	V
$I_{IH} (1)$	HIGH state input current at, $V_{IN} = V_{IH}$ maximum value			1.0	mA
$I_{IH} (2)$	HIGH state input current at, $V_{IN} = 2.4V$	D input		40.0	μA
		Clear input		120.0	μA
		Preset or clock inputs		80.0	μA
$-I_{IL}$	LOW state input current at, $V_{IN} = 0.4V$			1.6	mA
I_{OL}	LOW state output current			16.0	mA
$-I_{OH}$	HIGH state output current			400.0	μA
I_{OS}	Output short-circuit current	5474	20.0	57.0	mA
		6474 & 7474	18.0	57.0	mA
t_{PHL}	HIGH to LOW state propagation time at 25°C*			40.0	ns
t_{PLH}	LOW to HIGH state propagation time at 25°C*			25.0	ns
$f(\text{clock})$	Clock frequency			15.0	MHz
$t_{p(\text{clock})}$	Duration of clock pulse	(clock HIGH)	30.0		ns
		(clock LOW)	37.0		ns
$t_{p(\text{preset})}$	Duration of preset pulse		30.0		ns
$t_{p(\text{clear})}$	Duration of clear pulse		30.0		ns
$t(\text{setup})$	Minimum set-up time w.r.t. positive edge of clock		20.0		ns
$t(\text{hold})$	Minimum hold time w.r.t. positive edge of clock		5.0		ns

*See Subgroup A4 for details

BS 9420 F016 to F018
BS 9420 F034 to F036
BS 9420 F097 to F103
Issue 2, July, 1977

Table 1

Function Table (each Bistable)

INPUTS				OUTPUTS	
Preset	Clear	Clock	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	$\uparrow$	H	H	L
H	H	$\uparrow$	L	L	H
H	H	L	X	Q ₀	$\bar{Q}$ ₀

H = HIGH state

L = LOW state

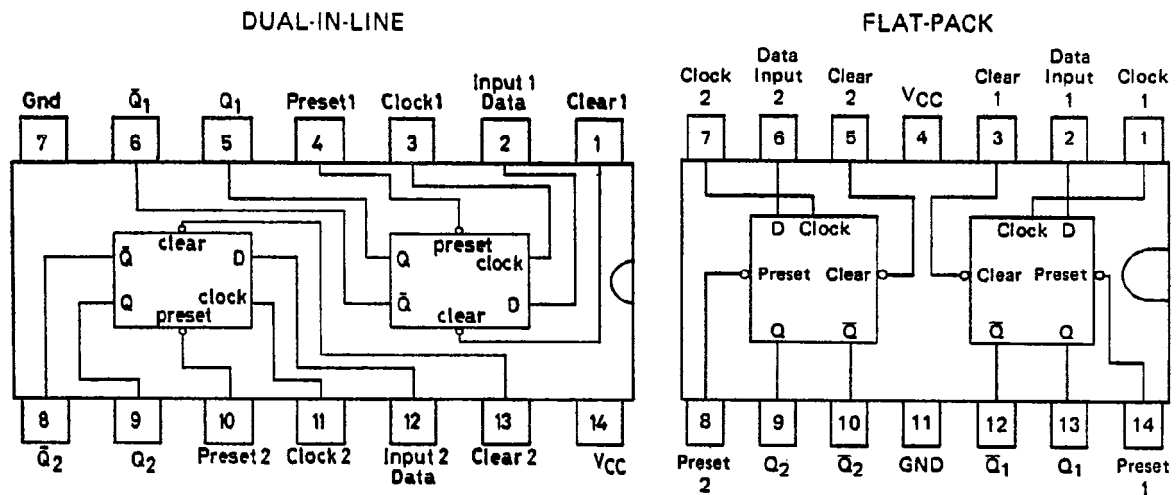
X = Irrelevant

 $\uparrow$ = Transition from LOW to HIGH levelQ₀, $\bar{Q}$ ₀ = The level of Q, $\bar{Q}$ before the indicated steady-state input conditions were established.

* = This configuration is nonstable, ie it will not persist when preset and clear inputs return to their inactive (HIGH) level.

Table II

Logic diagram and connections



BS 9420 F016 to F018
 BS 9420 F034 to F036
 BS 9420 F097 to F103
 Issue 2, July, 1977

3. Marking

(1) Each integrated circuit shall bear the following markings

- Terminal identification.
- The manufacturer's type number.
- The factory identification code, or manufacturer's trade mark.
- The date code.

(2) Each package containing one or more of these circuits shall bear the markings b, c and d above and in addition.

- The BS detail specification number. Example BS 9420 F035.

4. Related documents

BS 3934 'Dimensions of semiconductor devices'

BS 6001 'Sampling procedures and tables for inspection by attributes'

BS 9000 'General requirements for electronic components of assessed quality'

PD 9002 'Qualified products list for electronic components of assessed quality'

BS 9400 'Integrated electronic circuits of assessed quality: Generic data and methods of test'

5. Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturer's integrated circuit type and package identification as detailed in PD 9002 to BS 9420 F . . .
 as defined below.

TYPE		APPLICATION CATEGORY				FULL ASSESSMENT LEVEL
		S1	S2	S3	S4	
CERAMIC Dual-in-line and Flat-Pack	5474	F034	F035	F036	F097	F016
	6474	*	F098	F099	F100	F017
	7474	*	F101	F102	F103	F018
PLASTIC Dual-in-line	5474	*	*	*	*	F016
	6474	*	*	*	*	F017
	7474	*	*	*	*	F018

* = Not available at present.