

UTE

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CECC 90 101-029

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Page 0

Nombre total de pages : 16
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COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :
ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 101 (NF C 86-213)

UTE C 86-213/B 49

Adoptée le 16 novembre 1987

BS9442 F016 to F018

BS9442 F055 to F057

BS9442 F086 to F092

Issue 2

July, 1977

DESSIN ET DIMENSIONS :
OUTLINE AND DIMENSIONS :

CEI 191-2 - Types 050 G 04 - 050 G 03
IEC 191-2 -

Référence française : F 105 - F 105A
French reference :

IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS

Voir Tableau II
See Table II

SPECIFICATION PARTICULIERE POUR
MICROSTRUCTURES LOGIQUES SELON FS 90 101
DETAIL SPECIFICATION FOR DIGITAL INTEGRATED CIRCUITS IN ACCORDANCE WITH FS 90 101

54/64/74 90A

COMPTEUR DECIMAL ET BINAIRE
BCD DECADE COUNTERS

TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :

Circuit monolithique bipolaire au silicium, boîtiers
avec ou sans cavité.

Silicon monolithic bipolar integrated circuit,
cavity/non-cavity packages.

NIVEAUX D'ASSURANCE DE QUALITE : P, Y, L
ASSESSMENT LEVELS :

AMENDMENTS TO THE FOLLOWING CLAUSES

§ 2 - Add :

Most negative low level input voltage at an input current : $I_{IKB} = -12 \text{ mA}$, $V_{IKB} = -1,5 \text{ V}$

§ 3 To be replaced by CECC 90 000/3 § 2.5

§ 4 To be deleted

§ 5 To be replaced by CECC 90 000/3 § 2.6

§ 6 To be replaced by CECC 90 000/3 § 4.10.1

§ 7 All inspection level and AQL are those specified in 90 100/3.

Replace A3b by A4a, A3c by A4b, A4 by A5.

Page 9, t_{PHL} parameter :

- change limit for t_{PHL} parameter from input $R_{(9)}$ to outputs B and C from 24 ns to 40 ns (same limit as for $R_{(0)}$)
Add A8 of 90 100/3 (Assessment level P only).

Apply to A2 extreme temperature testing with A7a/A7b 90 000 inspection requirements.

For groups B, C, D, apply 90 100/3.

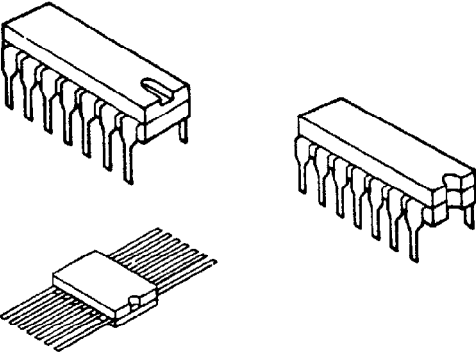
Sub-groups A6, A7 : not applicable.

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.

Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.

**Documents**

Document Sharing Hub

BRITISH STANDARDS INSTITUTION 2, PARK STREET, LONDON, W1A 2BS	BS9442 F016, 017, 018 BS9442 F055, 056, 057 BS9442 F086 to 092 Issue 2, July, 1977
ELECTRONIC COMPONENTS OF ASSESSED QUALITY: DETAIL SPECIFICATION	
Outlines not to scale  For details dimensions: 14 Lead Flat-Pack – see Appendix I 14 Lead Dual in-line – BS 3934 SO-87B	SILICON MONOLITHIC TTL BCD DECADE COUNTERS
	FULL ASSESSMENT LEVEL AND APPLICATION CATEGORIES S1, S2, S3 AND S4
	TYPES 5490A 6490A 7490A See Clause 5
	CERAMIC/GLASS HERMETICALLY SEALED ENCAPSULATION OR DUAL-IN-LINE PLASTIC ENCAPSULATION

1. Limiting conditions of use (not for inspection purposes)

Absolute values (non-simultaneous)			Units
V _{CC}	Maximum continuous positive supply voltage	7.0	V
	Maximum continuous negative supply voltage	0.5	V
	Maximum continuous positive input voltage	5.5	V
	Maximum continuous negative input voltage	0.5	V
-I _{IL}	Maximum input current for each input	A input *	3.2 mA
		B input *	4.8 mA
		(Reset inputs)	1.6 mA
			1.0 mA
	Maximum reverse input current for each input		
T _{amb}	Ambient operating temperature range	5490A	-55 to +125 °C
		6490A	-40 to + 85 °C
		7490A	0 to + 70 °C
T _{stg}	Storage temperature range		-65 to +150 °C
	Shock (0.5 ms duration)	14 700	m/s ²
	Vibration	196	m/s ²

Copies of this specification are available from manufacturers listed in the Qualified Products List Part 1, of PD 9002.

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2. Recommended conditions of use and associated characteristics (not for inspection purposes)

Over the full ambient operating temperature range unless otherwise stated.

			Min.	Max.	Units
V_{CC}	Positive supply voltage	5490A	4.5	5.5	V
		6490A & 7490A	4.75	5.25	V
V_{IH}	HIGH state input voltage	5490A	2.0	5.5	V
		6490A & 7490A	2.0	5.25	V
I_{CC}	Total supply current per package at V_{CC} Maximum value			42.0	mA
V_{OH}	HIGH state output voltage		2.4		V
V_{IL}	LOW state input voltage		0	0.8	V
V_{OL}	LOW state output voltage			0.4	V
$I_{IH} (1)$	HIGH state input current at, $V_{IN} = V_{IH}$ maximum value			1.0	mA
$I_{IH} (2)$	HIGH state input current at, $V_{IN} = 2.4V$	(A input) *		80.0	μA
		(B input) *		120.0	μA
		(Reset inputs) *		40.0	μA
$-I_{IL}$	LOW state input current at, $V_{IN} = 0.4V$	(A input) *		3.2	mA
		(B input) *		4.8	mA
		(Reset inputs) *		1.6	mA
$-I_{OH}$	HIGH state output current			800.0	μA
I_{OL}	LOW state output current			16.0	mA
$-I_{OS}$	Output short circuit current	5490A	20.0	57.0	mA
		6490A & 7490A	18.0	57.0	mA
t_{PHL}	HIGH to LOW state propagation time at 25°C (From input A to output D) *			50.0	ns
t_{PLH}	LOW to HIGH state propagation time at 25°C (From input A to output D) *			48.0	ns
f_{max}	Maximum frequency of operation (From input A to output A)		32.0		MHz
	(From input B to output B)		16.0		MHz
$t_p (count)$	Duration of input count pulse	(A input)	15.0		ns
		(B input)	30.0		ns
$t_p (reset)$	Duration of input reset pulse		15.0		ns
$t_{(set-up)}$	Reset inactive state set-up time		25.0		ns

*See Table II and Subgroup A4 for details

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Table I
Function tables
RESET sequence

RESET inputs				OUTPUTS			
R ₀ (1)	R ₀ (2)	R ₉ (1)	R ₉ (2)	A	B	C	D
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X		COUNT		
L	X	X	L				
X	L	L	X				
X	L	X	L				

X=Logic state irrelevant

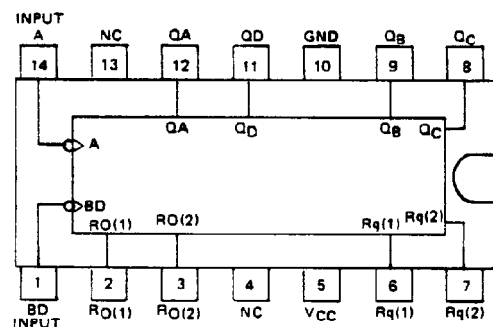
BCD COUNT sequence (output Q_A
connected to input B)

Count	Outputs			
	Q _A	Q _B	Q _C	Q _D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

B1-QUINARY COUNT (output Q_D
connected to input A)

Count	Output			
	Q _A	Q _B	Q _C	Q _D
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

Table II
Logic diagram and connections



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3. Marking

(1) Each integrated circuit shall bear the following markings

- a. Terminal identification.
- b. The manufacturer's type number.
- c. The factory identification code, or manufacturer's trade mark.
- d. The date code.

(2) Each package containing one or more of these circuits shall bear the markings b, c and d above and in addition.

- e. The BS detail specification number. Example BS 9442 F055

4. Related documents

BS 3934 'Dimensions of semiconductor devices'

BS 6001 'Sampling procedures and tables for inspection by attributes'

BS 9000 'General requirements for electronic components of assessed quality'

PD 9002 'Qualified products list for electronic components of assessed quality'

BS 9400 'Integrated electronic circuits of assessed quality: Generic data and methods of test'

5. Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturer's integrated circuit type and package identification as detailed in PD 9002 to BS 9442 F . . . as defined below.

TYPE		APPLICATION CATEGORY				FULL ASSESSMENT LEVEL
		S1	S2	S3	S4	
CERAMIC Dual-in-line and Flat-Pack	5490A	F055	F056	F057	F086	F016
	6490A	*	F087	F088	F089	F017
	7490A	*	F090	F091	F092	F018
PLASTIC Dual-in-line	5490A	*	*	*	*	F016
	6490A	*	*	*	*	F017
	7490A	*	*	*	*	F018

* = Not available at present.