

UTE

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CECC 90 101-032

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Page 0

Nombre total de pages : 14
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COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :
*ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :*

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 101 (NF C 86-213)

UTE C 86-213/B 52

Adoptée le 16 novembre 1987

BS9440 F028 to F030

BS9440 F055 to F057

BS9440 F125 to F131

Issue 1

November, 1977

DESSIN ET DIMENSIONS :
OUTLINE AND DIMENSIONS :

CEI 191-2 - Types 050 G 09 - 050 G 08
IEC 191-2 - Types 050 G 09 - 050 G 08

Référence française : F 117 - F 117A
French reference :

IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS

Voir Tableau II
See Table II

SPECIFICATION PARTICULIERE POUR
MICROSTRUCTURES LOGIQUES SELON FS 90 101
DETAIL SPECIFICATION FOR DIGITAL INTEGRATED CIRCUITS IN ACCORDANCE WITH FS 90 101

54/64/74 94

REGISTRE A DECALAGE
A 4 ELEMENTS BINAIRES

**4-BIT PARALLEL-IN SERIAL-OUT
SHIFT REGISTER**

TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :

Circuit monolithique bipolaire au silicium, boîtiers
avec ou sans cavité.

*Silicon monolithic bipolar integrated circuit,
cavity/non-cavity packages.*

NIVEAUX D'ASSURANCE DE QUALITE : P, Y, L
ASSESSMENT LEVELS :

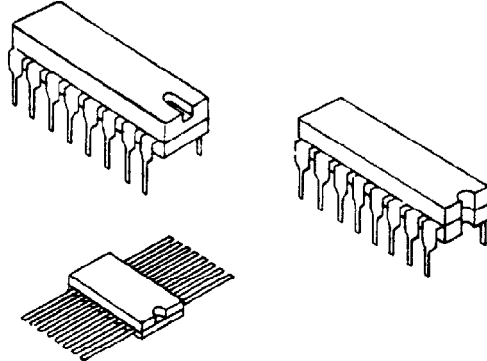
AMENDMENTS TO THE FOLLOWING CLAUSES

- § 2 - Add :
Most negative low level input voltage at an input current : $I_{IKB} = -12 \text{ mA}$, $V_{IKB} = -1,5 \text{ V}$
- § 3 To be replaced by CECC 90 000/3 § 2.5
- § 4 To be deleted
- § 5 To be replaced by CECC 90 000/3 § 2.6
- § 6 To be replaced by CECC 90 000/3 § 4.10.1
- § 7 All inspection level and AQL are those specified in 90 100/3.
Replace A3b by A4a, A3c by A4b, A4 by A5.
Add A8 of 90 100/3 (Assessment level P only).
Apply to A2 extreme temperature testing with A7a/A7b 90 000 inspection requirements.
For groups B, C, D, apply 90 100/3.
Sub-groups A6, A7 : not applicable.

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.
Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.

**Documents**

Document Sharing Hub

BRITISH STANDARDS INSTITUTION 2, PARK STREET, LONDON, W1A 2BS	BS 9440 F028 to F030 BS 9440 F055 to F057 BS 9440 F125 to F131 Issue 1, November, 1977
ELECTRONIC COMPONENTS OF ASSESSED QUALITY: DETAIL SPECIFICATION	
Outlines not to scale  For details dimensions: 16 Lead Flat-Pack — see Appendix I 16 Lead Dual in-Line — BS 3934 SO-87C	SILICON MONOLITHIC TTL DIGITAL 4-BIT PARALLEL — IN SERIAL — OUT SHIFT REGISTER
	FULL ASSESSMENT LEVEL AND APPLICATION CATEGORIES S1, S2, S3 AND S4
	TYPES 5494 6494 7494 See Clause 5
	CERAMIC/GLASS HERMETICALLY SEALED ENCAPSULATION OR DUAL-IN-LINE PLASTIC ENCAPSULATION

1. Limiting conditions of use (not for inspection purposes)

Absolute values			Units
V_{CC}	Maximum continuous positive supply voltage	7.0	V
	Maximum continuous negative supply voltage	0.5	V
	Maximum continuous positive input voltage	5.5	V
	Maximum continuous negative input voltage	0.5	V
	Maximum input current PE1 and PE2 inputs	6.4	mA
$-I_{IL}$	Other inputs	1.6	mA
	Maximum reverse input current	1.0	mA
T_{amb}	Ambient operating temperature range	5494 -55 to +125	°C
		6494 -40 to +85	°C
		7494 0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150	°C
	Shock (0.5 ms duration)	14 700	m/s ²
	Vibration	196	m/s ²

Copies of this specification are available from manufacturers listed in the Qualified Products List Part 1, of PD 9002.

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2. Recommended conditions of use and associated characteristics (not for inspection purposes)
 Over the full ambient operating temperature range unless otherwise stated.

			Min.	Max.	Units
V_{CC}	Positive supply voltage	5494	4.5	5.5	V
		6494 & 7494	4.75	5.25	V
V_{IH}	HIGH state input voltage	5494	2.0	5.5	V
		6494 & 7494	2.0	5.25	V
I_{CC}	Total supply current per package at V_{CC} maximum value	5494		50.0	mA
		6494 & 7494		58.0	mA
V_{OH}	HIGH state output voltage		2.4		V
V_{IL}	LOW state input voltage		0	0.8	V
V_{OL}	LOW state output voltage			0.4	V
$I_{IH(1)}$	HIGH state input current at $V_{IN} = V_{IH}$ maximum value			1.0	mA
$I_{IH(2)}$	HIGH state input current at $V_{IN} = 2.4V$	PE1 and PE2 inputs		160.0	μA
		Other inputs		40.0	μA
$-I_{IL}$	LOW state input current at $V_{IN} = 0.4V$	PE1 and PE2 inputs		6.4	mA
		Other inputs		1.6	mA
I_{OL}	LOW state output current			16.0	mA
$-I_{OH}$	HIGH state output current			400.0	μA
$-I_{OS}$	Output short circuit current	5494	20.0	57.0	mA
		6494 & 7494	18.0	57.0	mA
t_{PHL}	HIGH to LOW state propagation time at 25°C*			40.0	ns
t_{PLH}	LOW to HIGH state propagation time at 25°C*			40.0	ns
$f_{max.}$	Frequency of operation			> 10.0	MHz
$t_{(set-up)}$	Set-up time HIGH level data		35.0		ns
	LOW level data		25.0		ns
$t_{(hold)}$	Hold time		0		ns
$t_{p(clock)}$	Width of Clock pulse		35.0		ns
$t_{p(clear)}$	Width of Clear pulse		30.0		ns
$t_{p(preset)}$	Width of Preset pulse		30.0		ns

*See subgroup A4 for details.

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The register comprises four R-S master-slave bistables and associated gates and performs right-shift operations as a serial-in/serial-out register, or as a dual source, parallel-to-serial converter.

The outputs of the R-S bistables are simultaneously set to LOW by the application of a HIGH level signal to the Clear input while the internal presets are HIGH. Clearing is independent of the level of the Clock input.

Parallel loading is accomplished, after clearing, by presenting the data to be loaded to either the P1 inputs (P1A, P1B, P1C, P1D) or the P2 inputs (P2A, P2B, P2C, P2D) while the associated Preset Enable input (PE1 or PE2) is HIGH. Presetting, like clearing, is independent of the level of the Clock input.

Transfer of information to the outputs occurs on the LOW to HIGH transition of the Clock input. Proper information must be present at the R-S inputs of each bistable prior to the clock transition. The Serial input provides this information to the first bistable while the outputs of the subsequent bistables provide the information for the remaining R-S inputs. For the transfer to be effective, the Clear input must be LOW and the internal presets must be HIGH when clocking occurs.

Table I
Function tables

PRESET

PRESET INPUTS				INTERNAL PRESET A
PE1	PA1	PE2	PA2	
L	X	L	X	H*
L	X	X	L	H*
X	L	L	X	H*
X	L	X	L	H*
H	H	X	X	L†
X	X	H	H	L†

X = Logic state irrelevant. *Inactive. †Active.

REGISTER

INTERNAL PRESETS				INPUTS			INTERNAL OUTPUTS			OUTPUT
A	B	C	D	CLEAR	CLOCK	SERIAL	Q _A	Q _B	Q _C	Q _D
H	H	H	H	H	X	X	L	L	L	L
L	L	L	L	L	X	X	H	H	H	H
H	H	H	H	L	L	X	Q _{AO}	Q _{BO}	Q _{CO}	Q _{DO}
L	H	L	H	L	L	X	H	Q _{BO}	H	Q _{DO}
H	H	H	H	L	†	H	H	Q _{AN}	Q _{BN}	Q _{CN}
H	H	H	H	L	†	L	L	Q _{AN}	Q _{BN}	Q _{CN}

X = Logic state irrelevant. † = Transition from LOW to HIGH level.

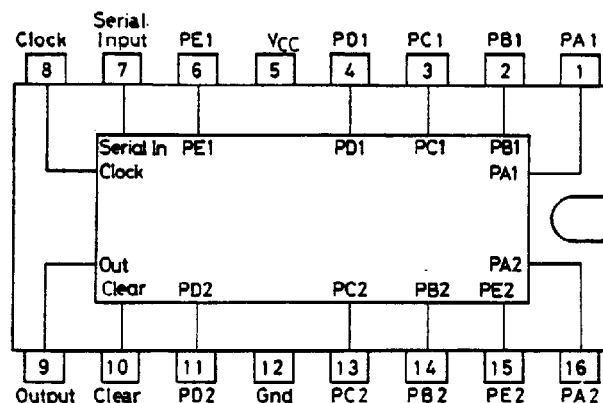
Q_{AO}, Q_{BO}, Q_{CO}, Q_{DO} is the level of Q_A, Q_B, Q_C, Q_D respectively before the indicated steady state input conditions were established.

Q_{AN}, Q_{BN}, Q_{CN} is the level of Q_A, Q_B, Q_C respectively before the most recent LOW to HIGH level transition of the Clock.

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Table II

Logic diagram and connections



3. Marking

(1) Each integrated circuit shall bear the following markings

- Terminal identification.
- The manufacturer's type number.
- The factory identification code, or manufacturer's trade mark.
- The date code.

(2) Each package containing one or more of these circuits shall bear the markings b, c and d above and in addition.

- The BS detail specification number. Example BS 9440 F056

4. Related documents

BS 3934 'Dimensions of semiconductor devices'

BS 6001 'Sampling procedures and tables for inspection by attributes'

BS 9000 'General requirements for electronic components of assessed quality'

PD 9002 'Qualified products list for electronic components of assessed quality'

BS 9400 'Integrated electronic circuits of assessed quality: Generic data and methods of test'

5. Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturer's integrated circuit type and package identification as detailed in PD 9002 to BS 9440 F ... as defined below.

TYPE		APPLICATION CATEGORY				FULL ASSESSMENT LEVEL
		S1	S2	S3	S4	
CERAMIC Dual-in-line and Flat-Pack	5494	F055	F056	F057	F125	F028
	6494	*	F126	F127	F128	F029
	7494	*	F129	F130	F131	F030
PLASTIC Dual-in-line	5494	*	*	*	*	F028
	6494	*	*	*	*	F029
	7494	*	*	*	*	F030

* Not available at present.