

UTE

Spécification française harmonisée
Système CENELEC d'assurance de la qualité
12, Place des Etats-Unis
75783 PARIS CEDEX 16

Téléphone : (1) 47 23 72 57

Télex : 620434F

CECC 90 101-033

EDITION 1 - Novembre 1987

ISSUE 1 - November 1987



Page 0

Nombre total de pages : 15
Total number of pages :

COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :
*ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :*

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 101 (NF C 86-213)

UTE C 86-213/B 53

Adoptée le 16 novembre 1987

BS9440 F031 to F033

BS9440 F058 to F060

BS9440 F132 to F138

Issue 2

April, 1977

DESSIN ET DIMENSIONS :
OUTLINE AND DIMENSIONS :

CEI 191-2 - Types 050 G 04 - 050 G 03
IEC 191-2 - Types 050 G 04 - 050 G 03

Référence française : F 105 - F 105A
French reference :

IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS

Voir Tableau II
See Table II

SPECIFICATION PARTICULIERE POUR
MICROSTRUCTURES LOGIQUES SELON FS 90 101
DETAIL SPECIFICATION FOR DIGITAL INTEGRATED CIRCUITS IN ACCORDANCE WITH FS 90 101

54/64/74 95A

REGISTRE A DECALAGE A 4 ELEMENTS
BINAIRES AVEC CHARGEMENT PARALLELE

**4-BIT PARALLEL ACCESS
SHIFT REGISTER**

TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :

Circuit monolithique bipolaire au silicium, boîtiers
avec ou sans cavité.

*Silicon monolithic bipolar integrated circuit,
cavity/non-cavity packages.*

NIVEAUX D'ASSURANCE DE QUALITE : P, Y, L
ASSESSMENT LEVELS :

AMENDMENTS TO THE FOLLOWING CLAUSES

§ 2 - Add :

Most negative low level input voltage at an input current : $I_{IKB} = -12 \text{ mA}$, $V_{IKB} = -1,5 \text{ V}$

§ 3 To be replaced by CECC 90 000/3 § 2.5

§ 4 To be deleted

§ 5 To be replaced by CECC 90 000/3 § 2.6

§ 6 To be replaced by CECC 90 000/3 § 4.10.1

§ 7 All inspection level and AQL are those specified in 90 100/3.

Replace A3b by A4a, A3c by A4b, A4 by A5.

Add A8 of 90 100/3 (Assessment level P only).

Apply to A2 extreme temperature testing with A7a/A7b 90 000 inspection requirements.

For groups B, C, D, apply 90 100/3.

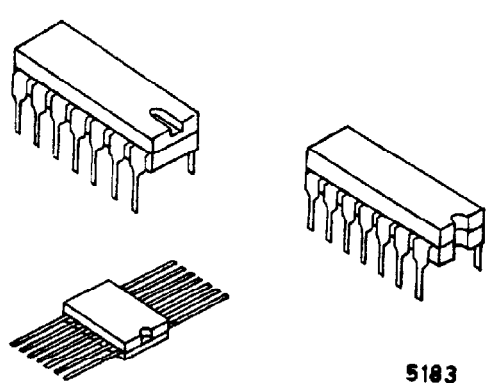
Sub-groups A6, A7 : not applicable.

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.

Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.

**Documents**

Document Sharing Hub

BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON W1A 2BS	BS 9440 F031 to 033 BS 9440 F058 to 060 BS 9440 F132 to 138 ISSUE 2, APRIL 1977
ELECTRONIC COMPONENTS OF ASSESSED QUALITY: DETAIL SPECIFICATION	
Outlines not to scale  5183 For detail dimensions: 14 Lead Flat-Pack – see Appendix I 14 Lead Dual in-line – see BS 3934 SO-87B	SILICON MONOLITHIC TTL FOUR-BIT PARALLEL ACCESS SHIFT REGISTER FULL ASSESSMENT LEVEL AND APPLICATION CATEGORIES S1, S2, S3 and S4 TYPES: 5495A 6495A 7495A See clause 5 CERAMIC/GLASS HERMETICALLY SEALED ENCAPSULATION OR DUAL IN-LINE PLASTIC ENCAPSULATION

1. Limiting conditions of use (not for inspection purposes)

Absolute values (non-simultaneous)			Units
V_{CC}	Maximum continuous positive supply voltage	7.0	V
	Maximum continuous negative supply voltage	0.5	V
	Maximum continuous negative input voltage	0.5	V
	Maximum continuous positive input voltage	5.5	V
$-I_{IL}$	Maximum input current for Serial, Clock and A, B, C, D inputs*	1.6	mA
$-I_{IL}$	Maximum input current for Mode Control input*	3.2	mA
	Maximum reverse input current for Serial, Clock and A, B, C, D inputs*	1.0	mA
	Maximum reverse input current for Mode Control input*	1.0	mA
T_{sto}	Storage temperature range	-65 to +150	°C
T_{amb}	Ambient operating temperature range	5495A -55 to +125	°C
		6495A -40 to +85	°C
		7495A 0 to +70	°C
	Shock (0.5 ms duration)	14 700	m/s ²
	Vibration	196	m/s ²

*See Table II

Copies of this specification are available from manufacturers
 Listed in the Qualified Products List Part 1, of PD 9002

BS 9440 F031 to 033
BS 9440 F058 to 060
BS 9440 F132 to 138
Issue 2, April 1977

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

Over the full ambient operating temperature range unless otherwise stated.

			Min.	Max.	Units
V_{CC}	Positive supply voltage	5495A	4.5	5.5	V
		6495A & 7495A	4.75	5.25	V
V_{IH}	HIGH state input voltage	5495A	2.0	5.5	V
		6495A & 7495A	2.0	5.25	V
I_{CC}	Total supply current per package at V_{CC} = maximum value			63.0	mA
V_{OH}	HIGH state output voltage		2.4		V
V_{IL}	LOW state input voltage		0	0.8	V
V_{OL}	LOW state output voltage			0.4	V
$I_{IH(1)}$	HIGH state input current at $V_{IN} = V_{IH}$ maximum value			1.0	mA
$I_{IH(2)}$	HIGH state input current at $V_{IN} = 2.4V$ (Serial, Clock and A, B, C, D inputs) (Mode Control input)			40.0	μA
				80.0	μA
$-I_{IL}$	LOW state input current at $V_{IN} = 0.4V$ (Serial, Clock and A, B, C, D inputs) (Mode Control input)			1.6	mA
				3.2	mA
$-I_{OH}$	HIGH state output current			800.0	μA
$-I_{OL}$	LOW state output current			16.0	mA
$-I_{OS}$	Output short circuit current		18.0	57.0	mA
t_{PHL}	HIGH to LOW state propagation time at 25°C* (From Clock 1 or Clock 2 to outputs)			36.0	ns
t_{PLH}	LOW to HIGH state propagation time at 25°C* (From Clock 1 or Clock 2 to outputs)			27.0	ns
f_{max}	Frequency of operation			≥ 25.0	MHz
$t_{p(clock)}$	Width of clock pulse		20.0		ns
$t_{(set-up)}$	Set-up time required at Serial, A, B, C, D inputs		15.0		ns
$t_{(hold)}$	Hold time required at Serial, A, B, C, D inputs (see fig 2)		0		ns
$t_{(enable)(1)}$	Time to enable Clock 1 (t_1 in Fig. 3)		15.0		ns
$t_{(enable)(2)}$	Time to enable Clock 2 (t_2 in Fig. 3)		15.0		ns
$t_{(inhibit)(1)}$	Time to inhibit Clock 1 (t_3 in Fig. 3)		5.0		ns
$t_{(inhibit)(2)}$	Time to inhibit Clock 2 (t_4 in Fig. 3)		5.0		ns

*See subgroup A4 for details.

BS 9440 F031 to 033
BS 9440 F058 to 080
BS 9440 F132 to 138
Issue 2, April 1977

Table 1

Function table

When a logical 0 level is applied to the Mode Control input, the number 1 AND gates are enabled and the number 2 AND gates are inhibited. In this mode the output of each bistable is coupled to the R-S inputs of the succeeding bistable. Right-shift operation is performed by clocking at the Clock 1 input, and serial data is entered at the Serial input. Clock 2 and parallel inputs A through D are inhibited by the number 2 AND gates.

When a logical 1 level is applied to the Mode Control input, the number 1 AND gates are inhibited (decoupling the outputs from the succeeding R-S inputs to prevent right-shift) and the number 2 AND gates are enabled to allow entry of data through parallel inputs A through D and Clock 2. This mode permits parallel loading of the register or, with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each bistable to the parallel input of the previous bistable (D output to input C, and etc.), and serial data is entered at input D.

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to Clock 1 and Clock 2. Information must be present at the R-S inputs of the master-slave bistables prior to clocking.

INPUTS					OUTPUTS			
PARALLEL				MODE CONTROL	CLOCK (2)	CLOCK (1)	SERIAL	Q _A Q _B Q _C Q _D
A	B	C	D					
X	X	X	X	H	H	X	X	Q _{AO} Q _{BO} Q _{CO} Q _{DO}
a	b	c	d	H	↓	X	X	a b c d
Q _B Q _C Q _D d				H	↓	X	X	Q _{BN} Q _{CN} Q _{DN} d
X	X	X	X	L	L	H	X	Q _{AO} Q _{BO} Q _{CO} Q _{DO}
X	X	X	X	L	X	↓	H	H Q _{AN} Q _{BN} Q _{CN}
X	X	X	X	L	X	↓	L	L Q _{AN} Q _{BN} Q _{CN}
X	X	X	X	↑	L	L	X	Q _{AO} Q _{BO} Q _{CO} Q _{DO}
X	X	X	X	↓	L	L	X	Q _{AO} Q _{BO} Q _{CO} Q _{DO}
X	X	X	X	↓	L	H	X	Q _{AO} Q _{BO} Q _{CO} Q _{DO}
X	X	X	X	↑	H	L	X	Q _{AO} Q _{BO} Q _{CO} Q _{DO}
X	X	X	X	↑	H	H	X	Q _{AO} Q _{BO} Q _{CO} Q _{DO}

X = Logic state irrelevant.

↑ = Transition from LOW to HIGH level.

↓ = Transition from HIGH to LOW level.

a, b, c, d = The level of the steady-state input at inputs A, B, C, D respectively.

Q_{AO}, Q_{BO}, Q_{CO}, Q_{DO} = The level of Q_A, Q_B, Q_C, Q_D respectively before the indicated steady-state input conditions were established.

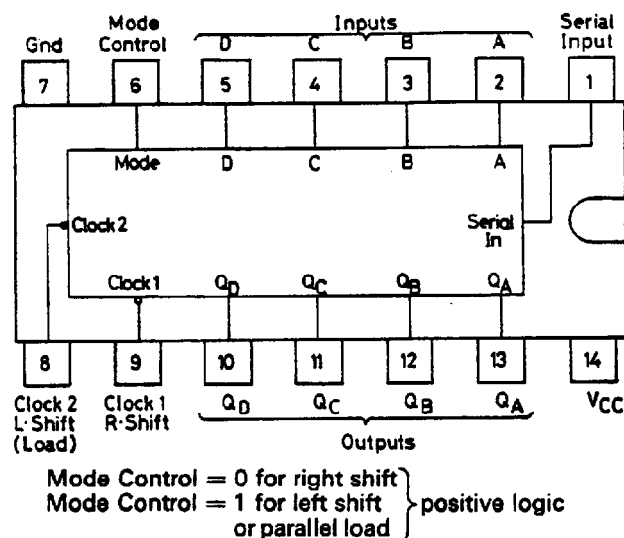
Q_{AN}, Q_{BN}, Q_{CN}, Q_{DN} = The level of Q_A, Q_B, Q_C, Q_D respectively before the most-recent HIGH to LOW transition of the clock.

BS 9440 F031 to 033
BS 9440 F058 to 060
BS 9440 F132 to 138

Issue 2, April 1977

Table II

Logic diagram and connections



3. Marking

- (1) Each integrated circuit shall bear the following markings:
 - a. Terminal identification.
 - b. The manufacturer's type number.
 - c. The factory identification code.
 - d. The date code.
- (2) Each package containing one or more of these circuits shall bear the markings 'b', 'c' and 'd' above and in addition:
 - e. The BS detail specification number e.g., BS 9440 F031.

4. Related documents

BS 3934 'Dimensions of semiconductor devices',
BS 6001 'Sampling procedures and tables for inspection by attributes',
BS 9000 'General requirements for electronic components of assessed quality',
PD 9002 'Qualified products list for electronic components of assessed quality',
BS 9400 'Integrated electronic circuits of assessed quality: Generic data and methods of test'.

5. Ordering information

Orders for these integrated circuits shall contain the following minimum information:
Manufacturer's integrated circuit type and package identification as detailed in PD 9002 to BS 9440 F... as defined below.

TYPE		APPLICATION CATEGORY				FULL ASSESSMENT LEVEL
		S1	S2	S3	S4	
CERAMIC Dual in-line and Flat-Pack	5495A	F058	F059	F060	F132	F031
	6495A	★	F133	F134	F135	F032
	7495A	★	F136	F137	F138	F033
PLASTIC Dual in-line	5495A	★	★	★	★	F031
	6495A	★	★	★	★	F032
	7495A	★	★	★	★	F033

★ = Not available at the present time.