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UTE

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CECC 90 101-034

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COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :
*ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :*

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 101 (NF C 86-213)

UTE C 86-213/B 54

Adoptée le 16 novembre 1987

BS9405 F0685 to F0697

Issue 1

August, 1980

DESSIN ET DIMENSIONS :
OUTLINE AND DIMENSIONS :

CEI 191-2 - Types 050 G 09 - 050 G 08
IEC 191-2 - Types 050 G 09 - 050 G 08

Référence française : F 117 - F 117A
French reference :

IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS

Voir Tableau II
See Table II

SPECIFICATION PARTICULIERE POUR
MICROSTRUCTURES LOGIQUES SELON FS 90 101
DETAIL SPECIFICATION FOR DIGITAL INTEGRATED CIRCUITS IN ACCORDANCE WITH FS 90 101

54/64/74 120**GENERATEUR SYNCHRONISE DE SIGNAUX****DUAL PULSE SYNCHRONISERS/DRIVERS**

TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :

Circuit monolithique bipolaire au silicium, boîtiers
avec ou sans cavité.

*Silicon monolithic bipolar integrated circuit,
cavity/non-cavity packages.*

NIVEAUX D'ASSURANCE DE QUALITE : P, Y, L
ASSESSMENT LEVELS :

AMENDMENTS TO THE FOLLOWING CLAUSES

§ 2 - Add :

Most negative low level input voltage at an input current : $I_{IKB} = -12 \text{ mA}$, $V_{IKB} = -1,5 \text{ V}$

- Page 2, I_{CC} parameter : change limit from 5 mA to 90 mA

- Page 2, $I_{IH(2)}$ parameter : change limits from 80 A to 80 μA and from 360 A to 360 μA

§ 3 To be replaced by CECC 90 000/3 § 2.5

§ 4 To be deleted

§ 5 To be replaced by CECC 90 000/3 § 2.6

§ 6 To be replaced by CECC 90 000/3 § 4.10.1

§ 7 All inspection level and AQL are those specified in 90 100/3.

Replace A3b by A4a, A3c by A4b, A4 by A5.

Add A8 of 90 100/3 (Assessment level P only).

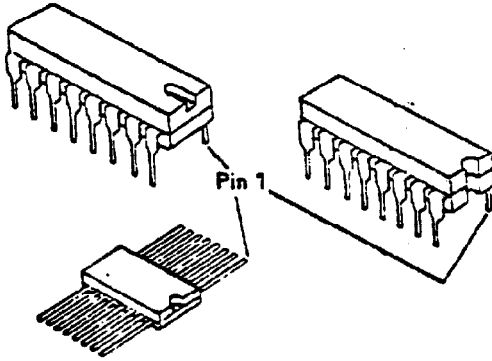
Apply to A2 extreme temperature testing with A7a/A7b 90 000 inspection requirements.

For groups B, C, D, apply 90 100/3.

Sub-groups A6, A7 : not applicable.

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.

Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.

BRITISH STANDARDS INSTITUTION 2, PARK STREET, LONDON, W1A 2BS Specification available from: As shown in PD 9002	BS 9405 P0685 to P0697 ISSUE 1 AUGUST 1980 Page 1 of 20 Pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH BS 9400: 1970	MANUFACTURER'S TYPE NUMBER 54120 64120 74120 SEE PD 9002
Outline not to scale. Isometric projection.  For detail dimensions: Lead Flatpack - See Appendix 1 Lead Dual-in-line - BS 3934 SO-675 Marking information - See Clause 3	For ordering information see clause 5. SILICON MONOLITHIC TTL DUAL PULSE SYNCHRONISERS/DRIVERS (See clause 8) CERAMIC/GLASS HERMETICALLY SEALED ENCAPSULATION OR DUAL-IN-LINE PLASTIC ENCAPSULATION FULL ASSESSMENT LEVEL AND APPLICATION CATEGORIES S1, S2, S3 and S4

1. LIMITING CONDITIONS OF USE (not for inspection purposes)

Absolute values (non-simultaneous)

V_{CC}	Maximum continuous positive supply voltage		7.0 V
	Maximum continuous negative supply voltage		0.5 V
V_{IN}	Maximum continuous positive input voltage		5.5 V
$-V_{IN}$	Maximum continuous negative input voltage		0.5 V
$-I_{IN}$	Maximum input current (clamping mode)		12.0 mA
T_{amb}	Ambient operating temperature range	SW20	-55°C to -125°C
		6W20	-40°C to + 95°C
		7W20	0°C to + 70°C
T_{stg}	Storage temperature range		-55°C to +150°C
	Shock (10.5 ms duration)		14 700 m/s ²
	Vibration		196 m/s ²

Refer to Qualified Products List PD 9002 for details of manufacturers approved to this specification

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2. RECOMMENDED CONDITIONS OF USE AND ASSOCIATED CHARACTERISTICS
(Not for inspection purposes)

These characteristics apply over the ambient operating temperature range unless otherwise stated.

			Min.	Max.	Unit
V_{CC}	Positive supply voltage	54120	4.5	5.5	V
		64120, 74120	4.75	5.25	V
I_{CC}	Total supply current per package at V_{CC} maximum		-	5.0	mA
V_{IH}	HIGH state input voltage		2.0	5.5	V
V_{IL}	LOW state input voltage		-	0.8	V
V_{OH}	HIGH state output voltage at $-I_{OH} = I_{OH}$ max.		2.4	-	V
V_{OL}	LOW state output voltage $I_{OL} = 48$ mA		-	0.4	V
$I_{IH(1)}$	HIGH state input current $V_{IN} = V_{IH}$ max.		-	1.0	mA
$I_{IH(2)}$	HIGH state input current $V_{IN} = V_{OH}$ min.	Clock Input	-	80.0	A
		Other Inputs	120.0	360.0	A
$-I_{IL}$	LOW state input current $V_{IN} = V_{OL}$ max.	Clock Input	-	3.2	mA
		Other Inputs	-	2.1	mA
$-I_{OH}$	HIGH state output current		-	2.4	mA
I_{OL}	LOW state output current		-	28.0	mA
$-I_{OS}$	Output short circuit current		35.0	90.0	mA
$-V_{IK}$	Input Clamping Voltage $V_{CC} = \text{Min.}$ $I_L = -12$ mA		-	1.5	V

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2. RECOMMENDED CONDITIONS OF USE AND ASSOCIATED CHARACTERISTICS (Contd.)

SWITCHING CHARACTERISTICS

$V_{CC} = 5V$, $T_{amb} = 25^{\circ}C$, $C_L = 45 pF$, $R_L = 133 \Omega$

			Min.	Max.	Unit
t_{PHL}	HIGH to LOW state propagation time	From C to Y		25.0	ns
		From C to $\bar{Y}$		13.0	ns
t_{PLH}	LOW to HIGH state propagation time	From C to Y		22.0	ns
		From C to $\bar{Y}$		16.0	ns
t_{set-up}	Input set-up time	Any input except mode control	12.0	-	ns
		Mode Control - $t_{set-up}(H)$	0.0	-	ns
		$t_{set-up}(L)$	12.0	-	ns
t_{hold}	Hold Time	Any input except mode control	3.0	-	ns
		Mode Control	20.0	-	ns

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FUNCTION TABLE

TABLE I

INPUTS			FUNCTION
R	S1	S2	
X	L	X	Pass Output Pulses
X	X	L	Pass Output Pulses
L	M	M	Inhibit Output Pulses
M	.	M	Start Output Pulses
M	M	.	Start Output Pulses
.	M	M	Stop Output Pulses
M	M	M	Continue

M = high-level steady state

L = low-level steady state

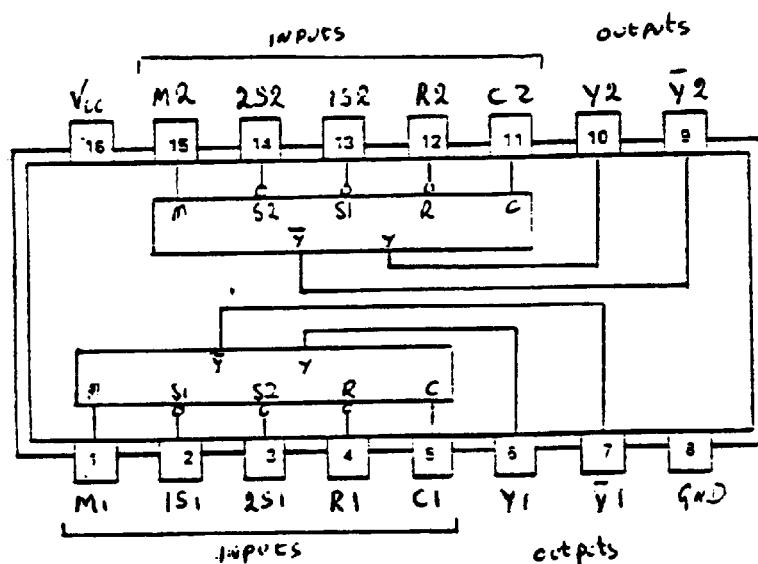
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X = irrelevant

*Operation initiated by test - transition from high

PIN CONNECTION DIAGRAM

TABLE II



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3. MARKING.

- 3.1 Each integrated circuit shall bear the following markings:
- (a) Terminal identification.
 - (b) The manufacturer's type number.
 - (c) The factory identification code, or manufacturer's trade mark.
 - (d) The date code.
- 3.2 Each package containing one or more of these circuits shall bear the markings (b), (c) and (d) above and in addition:
- (e) The B.S. detail specification number.

4. RELATED DOCUMENTS.

- BS 2011 Basic environmental testing procedures.
- BS 3934 Dimensions of semiconductor devices.
- BS 6001 Sampling procedures and tables for inspection by attributes.
- BS 9000 General requirements for electronic components of assessed quality.
- BS 9400 Integrated electronic circuits of assessed quality: Generic data and methods of test.
- PD 9002 Qualified Products List for electronic components of assessed quality.

5. ORDERING INFORMATION.

Orders for these integrated circuits shall contain the following minimum information:

Manufacturer's integrated circuit type and package identification
 as detailed in PD 9002 to BS9405 F..... as defined below -

TYPE		APPLICATION CATEGORY				FULL ASSESSMENT LEVEL
		S1	S2	S3	S4	
CERAMIC Dual-in-line and Flatpack	54120	F0685	F0686	F0687	F0688	F0689
	64120	.	F0690	F0691	F0692	F0693
	74120	.	F0694	F0695	F0696	F0697
PLASTIC Dual-in-line	54120	.	.	.	.	F0689
	64120	.	.	.	.	F0693
	74120	.	.	.	.	F0697

Note: . Not available at present.