

UTE

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CECC 90 101-048

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Nombre total de pages : 16
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COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :
*ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :*

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 101 (NF C 86-213)

UTE C 86-213/B 68

Adoptée le 16 novembre 1987

BS9442 F022 to F024

BS9442 F040 to F042

BS9442 F128 to F134

Issue 1

May, 1981

DESSIN ET DIMENSIONS :
OUTLINE AND DIMENSIONS :

CEI 191-2 - Types 050 G 09 - 050 G 08
IEC 191-2 - Types 050 G 09 - 050 G 08

Référence française : F 117 - F 117A
French reference :

IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS

Voir Tableau II
See Table II

SPECIFICATION PARTICULIERE POUR
MICROSTRUCTURES LOGIQUES SELON FS 90 101
DETAIL SPECIFICATION FOR DIGITAL INTEGRATED CIRCUITS IN ACCORDANCE WITH FS 90 101

54/64/74 163

**COMPTEUR BINAIRE
A 4 ELEMENTS BINAIRES
4-BIT BINARY COUNTER**

TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :

Circuit monolithique bipolaire au silicium, boîtiers
avec ou sans cavité.

*Silicon monolithic bipolar integrated circuit,
cavity/non-cavity packages.*

NIVEAUX D'ASSURANCE DE QUALITE : P, Y, L
ASSESSMENT LEVELS :

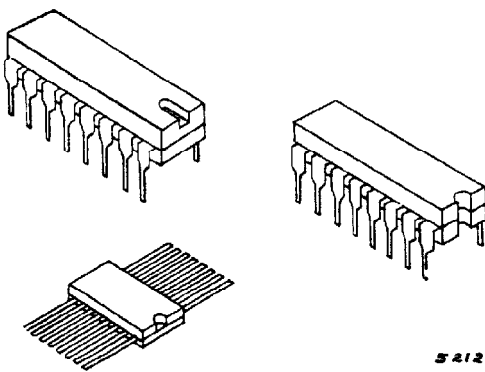
AMENDMENTS TO THE FOLLOWING CLAUSES

- § 2 - Add :
Most negative low level input voltage at an input current : $I_{IKB} = -12 \text{ mA}$, $V_{IKB} = -1,5 \text{ V}$
- § 3 To be replaced by CECC 90 000/3 § 2.5
- § 4 To be deleted
- § 5 To be replaced by CECC 90 000/3 § 2.6
- § 6 To be replaced by CECC 90 000/3 § 4.10.1
- § 7 All inspection level and AQL are those specified in 90 100/3.
- Page 6, I_{IL} clock parameter : replace limit 1,6 mA by 3,2 mA
 - Page 7, $I_{IH(2)}$ parameter : replace "for enable T input" by "for enable T and clock inputs"
 - Page 8, for t_{PHL} and t_{PLH} parameters, swap limits given for :
 - "clock (load input high) to each output" and
 - "clock (load input low) to each output"
- Replace A3b by A4a, A3c by A4b, A4 by A5.
Add A8 of 90 100/3 (Assessment level P only).
Apply to A2 extreme temperature testing with A7a/A7b 90 000 inspection requirements.
For groups B, C, D, apply 90 100/3.
Sub-groups A6, A7 : not applicable.

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.
Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.

**Documents**

Document Sharing Hub

BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON W1A 2BS	BS 9442 F022 to 024 BS 9442 F040 to 042 BS 9442 F128 to 134 ISSUE 1, MAY 1981
ELECTRONIC COMPONENTS OF ASSESSED QUALITY: DETAIL SPECIFICATION	
Outlines not to scale  For detail dimensions: 16 Lead Flat-Pack – see Appendix I 16 Lead Dual in-line – see BS 3934 SO-87C	SILICON MONOLITHIC TTL FOUR-BIT BINARY COUNTER FULL ASSESSMENT LEVEL AND APPLICATION CATEGORIES S1, S2, S3 and S4 TYPES: 54163 64163 74163 See clause 5 CERAMIC/GLASS HERMETICALLY SEALED ENCAPSULATION OR DUAL IN-LINE PLASTIC ENCAPSULATION

1. Limiting conditions of use (not for inspection purposes)

Absolute values (non-simultaneous)			Units
V_{CC}	Maximum continuous positive supply voltage	7.0	V
	Maximum continuous negative supply voltage	0.5	V
	Maximum continuous positive input voltage	5.5	V
	Maximum continuous negative input voltage	0.5	V
$-I_{IL}$	Maximum input current (Enable T input)	3.2	mA
	Maximum input current for other inputs	1.6	mA
	Maximum reverse input current	1.0	mA
T_{stg}	Storage temperature range	-65 to +150	°C
T_{amb}	Ambient operating temperature range	54163 -55 to +125	°C
		64163 -40 to +85	°C
		74163 0 to +70	°C
	Shock (0.5 ms duration)	14 700	m/s ²
	Vibration	196	m/s ²

Copies of this specification are available from manufacturers listed in the Qualified Products List, Part 1 of PD 9002.

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2. Recommended conditions of use and associated characteristics (not for inspection purposes)
Over the full ambient operating temperature range unless otherwise stated.

			Min.	Max.	Units
V_{CC}	Positive supply voltage	54163	4.5	5.5	V
		64163 & 74163	4.75	5.25	V
V_{IH}	HIGH state input voltage	54163	2.0	5.5	V
		64163 & 74163	2.0	5.25	V
I_{CC}	Total supply current per package at V_{CC} = maximum value	54163		91.0	mA
		64163 & 74163		101.0	mA
V_{OH}	HIGH state output voltage		2.4		V
V_{IL}	LOW state input voltage		0	0.8	V
V_{OL}	LOW state output voltage			0.4	V
$I_{IH(1)}$	HIGH state input current at V_{IH} = maximum value			1.0	mA
$I_{IH(2)}$	HIGH state input current at $V_{OH} = 2.4V$ (Enable T input) *			80.0	μA
	(Other inputs) *			40.0	μA
$-I_{IL}$	LOW state input current at $V_{OL} = 0.4V$ (Enable T input) *			3.2	mA
	(Other inputs) *			1.6	mA
$-I_{OH}$	HIGH state output current			800.0	μA
I_{OL}	LOW state output current			16.0	mA
$-I_{OS}$	Output short circuit current	54163	20.0	57.0	mA
		64163 & 74163	18.0	57.0	mA
t_{PHL}	HIGH to LOW state propagation time at $25^{\circ}C$ †			38.0	ns
t_{PLH}	LOW to HIGH state propagation time at $25^{\circ}C$ †			35.0	ns
f_{max}	Frequency of operation			> 25.0	MHz
$t_{p(clock)}$	Duration of clock pulse		25.0		ns
$t_{p(clear)}$	Duration of clear pulse		20.0		ns
$t_{(set-up)}$	Set-up time (Load input) ‡		25.0		ns
	(Enable P and Data A, B, C, D inputs) ‡		20.0		ns
	(Clear input) ‡		20.0		ns
$t_{(hold)}$	Hold time		0		ns

*See table II †See subgroup A4 for details ‡See fig. 2 and 3

INPUTS									OUTPUTS				
CLEAR	LOAD	DATA				ENABLE		CLOCK	CARRY	Q _A	Q _B	Q _C	Q _D
		A	B	C	D	T	P						
L	H	L	L	L	L	L	L	H	L	L	L	L	
H	H	L	L	L	L	H	H	H	L	L	L	L	
H	H	L	L	L	L	H	H	L	L	L	L	L	
H	H	L	L	L	L	H	H	L	L	L	L	L	
H	H	L	L	L	L	H	H	L	L	L	L	L	
These conditions are applied for a further 13 clock pulses									L	Outputs follow binary count sequence to count of 15			
H	H	L	L	L	L	H	H	H	H	H	H	H	
H	L	L	L	L	L	L	L	H	L	H	H	H	
H	L	L	L	L	L	L	L	L	L	H	H	H	
H	L	L	L	L	L	L	L	L	L	L	H	H	
H	L	L	L	L	L	L	L	L	L	L	L	H	
H	L	L	L	L	L	L	L	L	L	L	L	L	
H	L	Data inputs follow binary count sequence to count of 15				L	L	L	L	Outputs follow binary count sequence after each clock pulse			
H	L	H	H	H	H	L	L	L	L	H	H	H	
H	H	H	H	H	H	L	H	L	H	H	H	H	
H	H	L	L	L	L	L	H	L	H	H	H	H	
H	H	L	L	L	L	L	H	L	H	H	H	H	
H	H	L	L	L	L	L	H	L	H	H	H	H	
H	H	L	L	L	L	L	H	L	L	H	H	H	

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The counter is a 4-bit binary counter incorporating a "Carry" circuit. Synchronous operation is provided by simultaneous clocking of the four J-K bistables, this arrangement causing the outputs to change coincident with each other when so ordered by the Count Enable inputs and internal gating. A buffered Clock input triggers the four bistables on its transition from LOW to HIGH.

Outputs may be preset by setting the Data inputs to the desired output levels, while the Load input is LOW, and taking the Clock from LOW to HIGH. During presetting, the levels of the Enable inputs are disregarded, and the LOW at the Load input disables the counter. LOW to HIGH transitions at the Load input should be avoided when the Clock input is LOW if the Enable inputs are HIGH at, or before, the Load input transition.

The "Carry" circuit allows counters to be cascaded without additional gating. The signals associated with this circuit are the two Count Enable inputs (P and T) and a Ripple Carry output. When the counter reaches its maximum count with both Count Enable inputs HIGH (both must be high for the counter to count), input T enables the Ripple Carry output which produces a HIGH output pulse. This pulse can be used to enable succeeding cascaded stages.

A LOW at the Clear input sets all four bistable outputs LOW after the succeeding Clock pulse, regardless of the levels of the Enable inputs.

3. Marking

- (1) Each integrated circuit shall bear the following markings:
 - a. Terminal identification.
 - b. The manufacturer's type number.
 - c. The factory identification code.
 - d. The date code.
- (2) Each package containing one or more of these circuits shall bear the markings 'b', 'c' and 'd' above and in addition:
 - e. The BS detail specification number e.g., BS 9442 F022.

4. Related documents

BS 3934 'Dimensions of semiconductor devices',
BS 6001 'Sampling procedures and tables for inspection by attributes',
BS 9000 'General requirements for electronic components of assessed quality',
PD 9002 'Qualified products list for electronic components of assessed quality',
BS 9400 'Integrated electronic circuits of assessed quality: Generic data and methods of test'.

5. Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturer's integrated circuit type and package identification as detailed in PD 9002 to BS 9442 F... as defined below.

TYPE		APPLICATION CATEGORY				FULL ASSESSMENT LEVEL
		S1	S2	S3	S4	
CERAMIC Dual in-line and Flat-Pack	54163	F040	F041	F042	F128	F022
	64163	★	F129	F130	F131	F023
	74163	★	F132	F133	F134	F024
PLASTIC Dual in-line	54163	★	★	★	★	F022
	64163	★	★	★	★	F023
	74163	★	★	★	★	F024

★ = Not available at the present time.