

UTE

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CECC 90 101-049

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Page 0

Nombre total de pages : 15
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COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :

ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 101 (NF C 86-213)

UTE C 86-213/B 69

Adoptée le 16 novembre 1987

BS9440 F037 to F039

BS9440 F064 to F066

BS9440 F167 to F173

Issue 2

July, 1977

DESSIN ET DIMENSIONS :
OUTLINE AND DIMENSIONS :

CEI 191-2 - Types 050 G 04 - 050 G 03
IEC 191-2 - Types 050 G 04 - 050 G 03

Référence française : F 105 - F 105A
French reference :

IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS

Voir Tableau II
See Table II

SPECIFICATION PARTICULIERE POUR
MICROSTRUCTURES LOGIQUES SELON FS 90 101
DETAIL SPECIFICATION FOR DIGITAL INTEGRATED
CIRCUITS IN ACCORDANCE WITH FS 90 101

54/64/74 164

REGISTRE A DECALAGE A 8 ELEMENTS BINAIRES
ENTREES SERIE, SORTIES PARALLELES

**8-BIT SERIAL-IN PARALLEL-OUT
SHIFT REGISTER**

TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :

Circuit monolithique bipolaire au silicium, boîtiers
avec ou sans cavité.

Silicon monolithic bipolar integrated circuit,
cavity/non-cavity packages.

NIVEAUX D'ASSURANCE DE QUALITE :
ASSESSMENT LEVELS :

P, Y, L

AMENDMENTS TO THE FOLLOWING CLAUSES

§ 2 - Add :

Most negative low level input voltage at an input current : $I_{IKB} = -12 \text{ mA}$, $V_{IKB} = -1,5 \text{ V}$

§ 3 To be replaced by CECC 90 000/3 § 2.5

§ 4 To be deleted

§ 5 To be replaced by CECC 90 000/3 § 2.6

§ 6 To be replaced by CECC 90 000/3 § 4.10.1

§ 7 All inspection level and AQL are those specified in 90 100/3.

Replace A3b by A4a, A3c by A4b, A4 by A5.

Add A8 of 90 100/3 (Assessment level P only).

Apply to A2 extreme temperature testing with A7a/A7b 90 000 inspection requirements.

For groups B, C, D, apply 90 100/3.

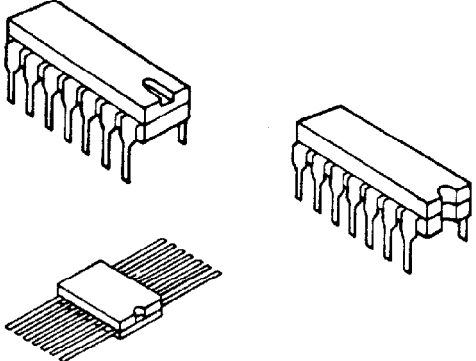
Sub-groups A6, A7 : not applicable.

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.

Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.

**Documents**

Document Sharing Hub

BRITISH STANDARDS INSTITUTION 2, PARK STREET, LONDON, W1A 2BS	BS9440 F037,038,039 BS9440 F064,065,066 BS9440 F167 to 173 ISSUE 2, JULY, 1977
ELECTRONIC COMPONENTS OF ASSESSED QUALITY: DETAIL SPECIFICATION	
Outlines not to scale.  For details dimensions: 14 Lead Flat-Pack – see Appendix I 14 Lead Dual in-line – BS 3934 SO-87B	SILICON MONOLITHIC TTL 8-BIT SERIAL-IN PARALLEL – OUT SHIFT REGISTER
	FULL ASSESSMENT LEVEL AND APPLICATION CATEGORIES S1, S2, S3 AND S4
	TYPES 54164 64164 74164 See Clause 5
	CERAMIC/GLASS HERMETICALLY SEALED ENCAPSULATION OR DUAL-IN-LINE PLASTIC ENCAPSULATION

1. Limiting conditions of use (not for inspection purposes)

Absolute values (non-simultaneous)			Units
V_{CC}	Maximum continuous positive supply voltage	7.0	V
	Maximum continuous negative supply voltage	0.5	V
	Maximum continuous positive input voltage	5.5	V
	Maximum continuous negative input voltage	0.5	V
$-I_{IL}$	Maximum input current	1.6	mA
	Maximum reverse input current	1.0	mA
T_{amb}	Ambient operating temperature range	54164	-55 to +125 °C
		64164	-40 to + 85 °C
		74164	0 to + 70 °C
T_{stg}	Storage temperature range		-65 to +150 °C
	Shock (0.5 ms duration)	14 700	m/s ²
	Vibration	196	m/s ²

Copies of this specification are available from manufacturers listed in the Qualified Products List Part 1, of PD 9002.

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2. Recommended conditions of use and associated characteristics (not for inspection purposes)

Over the full ambient operating temperature range unless otherwise stated.

			Min.	Max.	Units
V_{CC}	Positive supply voltage	54164	4.5	5.5	V
		64164 & 74164	4.75	5.25	V
V_{IH}	HIGH state input voltage	54164	2.0	5.5	V
		64164 & 74164	2.0	5.25	V
I_{CC}	Total supply current per package at V_{CC} maximum value			54.0	mA
V_{OH}	HIGH state output voltage		2.4		V
V_{IL}	LOW state input voltage		0	0.8	V
V_{OL}	LOW state output voltage			0.4	V
$I_{IH} (1)$	HIGH state input current at, $V_{IN} = V_{IH}$ maximum value			1.0	mA
$I_{IH} (2)$	HIGH state input current at, $V_{IN} = 2.4V$			40.0	μA
$-I_{IL}$	LOW state input current at, $V_{IN} = 0.4V$			1.6	mA
I_{OL}	LOW state output current			8.0	mA
$-I_{OH}$	HIGH state output current			400.0	μA
$-I_{OS}$	Output short-circuit current	54164	10.0	27.5	mA
		64164 & 74164	9.0	27.5	mA
t_{PHL}	HIGH to LOW state propagation time at 25°C*				
	from Clear input to outputs at $(C_L = 15 \text{ pF})$		—	36.0	ns
	from Clear input to outputs at $(C_L = 50 \text{ pF})$		—	42.0	ns
	from Clock input to outputs at $(C_L = 15 \text{ pF})$		—	32.0	ns
	from Clock input to outputs at $(C_L = 50 \text{ pF})$		—	37.0	ns
t_{PLH}	LOW to HIGH state propagation time at 25°C*				
	(from Clock inputs to outputs)				
	$C_L = 15 \text{ pF}$		—	27.0	ns
	$C_L = 50 \text{ pF}$		—	30.0	ns
$f_{max.}$	Maximum Frequency of operation		25.0	—	MHz
$t_{p(clock)}$	Duration of Clock pulse		20.0	—	ns
$t_{p(clear)}$	Duration of Clear pulse		20.0	—	ns
$t_{(setup)}$	Data set-up time (see Fig. 2)		15.0	—	ns
$t_{(hold)}$	Data hold time		5.0	—	ns

* See Subgroup A4 for details

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Table I

Function table

Serial data is entered on the positive transition of the clock pulse. A LOW level at either or both serial inputs inhibits the entry of data and sets the A output LOW on the next positive clock transition. A HIGH level on one of the serial inputs enables the other serial input

INPUTS				OUTPUTS			
Clear	Clock	A	B	Q _A	Q _B Q _H		
L	X	X	X	L	L	L	
H	L	X	X	Q _{AO}	Q _{BO}	Q _{HO}	
H	↑	H	H	H	Q _{AN}	Q _{GN}	
H	↑	L	X	L	Q _{AN}	Q _{GN}	
H	↑	X	L	L	Q _{AN}	Q _{GN}	

↑ = Positive clock transition.

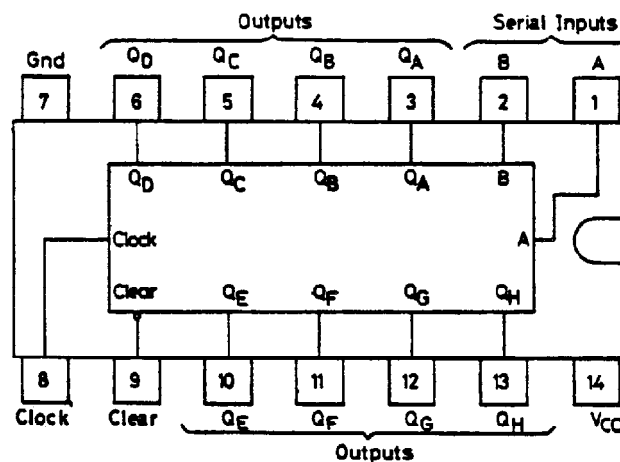
X = Logic state irrelevant.

Q_{AO}, Q_{BO}, etc. = The output logic level before the indicated steady state input conditions were applied.

Q_{AN}, . . . , Q_{GN} = The output logic level before the most recent positive clock transition.

Table II

Logic diagram and connections



The register is an 8-bit parallel-out serial shift register incorporating gated Serial Inputs (A and B) and an asynchronous Clear. The gated Serial inputs permit complete control over incoming data as a LOW at either input, or at both inputs, inhibits entry of new data and resets the first of the eight bistables to LOW at the succeeding Clock pulse. Either of the Serial inputs at HIGH enables the other input which then determines the state of the first bistable.

Change of data at the Serial inputs may be effected only when the Clock is HIGH or LOW. Clocking of the bistables occurs on the LOW to HIGH transition of the Clock input. All inputs are diode clamped to minimise transmission-line effects.

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3. Marking

(1) Each integrated circuit shall bear the following markings

- a. Terminal identification.
- b. The manufacturer's type number.
- c. The factory identification code, or manufacturer's trade mark.
- d. The date code.

(2) Each package containing one or more of these circuits shall bear the markings b, c and d above and in addition.

- e. The BS detail specification number. Example BS 9440 F065

4. Related documents

BS 3934 'Dimensions of semiconductor devices'

BS 6001 'Sampling procedures and tables for inspection by attributes'

BS 9000 'General requirements for electronic components of assessed quality'

PD 9002 'Qualified products list for electronic components of assessed quality'

BS 9400 'Integrated electronic circuits of assessed quality: Generic data and methods of test'

5. Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturer's integrated circuit type and package identification as detailed in PD 9002 to BS 9440 F ... as defined below.

TYPE		APPLICATION CATEGORY				FULL ASSESSMENT LEVEL
		S1	S2	S3	S4	
CERAMIC Dual-in-line and Flat-Pack	54164	F064	F065	F066	F167	F037
	64164	*	F168	F169	F170	F038
	74164	*	F171	F172	F173	F039
PLASTIC Dual-in-line	54164	*	*	*	*	F037
	64164	*	*	*	*	F038
	74164	*	*	*	*	F039

* = Not available at present.