

UTE

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CECC 90 101-050

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Page 0

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**COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :
ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :**

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 101 (NF C 86-213)

UTE C 86-213/B 70

Adoptée le 16 novembre 1987

BS9440 F040 to F042

BS9440 F067 to F069

BS9440 F174 to F180

Issue 1

March, 1978

**DESSIN ET DIMENSIONS :
OUTLINE AND DIMENSIONS :**

CEI 191-2 - Types 050 G 09 - 050 G 08
IEC 191-2 - Types 050 G 09 - 050 G 08

Référence française : F 117 - F 117A
French reference :

**IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS**

Voir Tableau II
See Table II

**SPECIFICATION PARTICULIERE POUR
MICROSTRUCTURES LOGIQUES SELON FS 90 101
DETAIL SPECIFICATION FOR DIGITAL INTEGRATED CIRCUITS IN ACCORDANCE WITH FS 90 101**

54/64/74 165

**REGISTRE A DECALAGE A 8 ELEMENTS BINAIRES
ENTREES PARALLELES, SORTIES SERIE**

**8-BIT PARALLEL-IN SERIAL-OUT
SHIFT REGISTER**

**TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :**

Circuit monolithique bipolaire au silicium, boîtiers avec ou sans cavité.

Silicon monolithic bipolar integrated circuit, cavity/non-cavity packages.

**NIVEAUX D'ASSURANCE DE QUALITE : P, Y, L
ASSESSMENT LEVELS :**

AMENDMENTS TO THE FOLLOWING CLAUSES

- § 2 - Add :
Most negative low level input voltage at an input current : $I_{IKB} = -12 \text{ mA}$, $V_{IKB} = -1,5 \text{ V}$
- § 3 To be replaced by CECC 90 000/3 § 2.5
- § 4 To be deleted
- § 5 To be replaced by CECC 90 000/3 § 2.6
- § 6 To be replaced by CECC 90 000/3 § 4.10.1
- § 7 All inspection level and AQL are those specified in 90 100/3.
Replace A3b by A4a, A3c by A4b, A4 by A5.
Add A8 of 90 100/3 (Assessment level P only).
Apply to A2 extreme temperature testing with A7a/A7b 90 000 inspection requirements.
For groups B, C, D, apply 90 100/3.
Sub-groups A6, A7 : not applicable.

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.
Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.

**Documents**

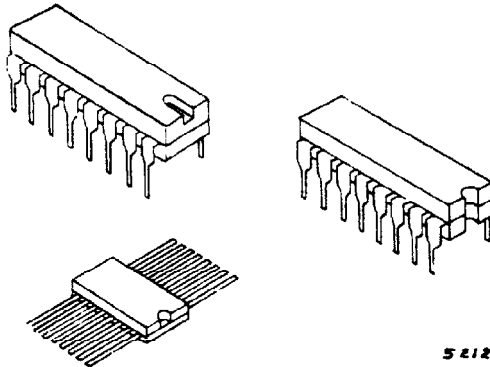
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BS 9440 F040 to 042
BS 9440 F067 to 069
BS 9440 F174 to 180
ISSUE 1, MARCH 1978

ELECTRONIC COMPONENTS OF ASSESSED QUALITY: DETAIL SPECIFICATION

Outlines not to scale



For detail dimensions:
16 Lead Flat-Pack – see Appendix I
16 Lead Dual in-line – see BS 3934 SO-87C

SILICON MONOLITHIC TTL
8-BIT PARALLEL-IN
SERIAL-OUT SHIFT REGISTER

FULL ASSESSMENT LEVEL
AND APPLICATION CATEGORIES
S1, S2, S3 and S4

TYPES:
54165
64165
74165

CERAMIC/GLASS HERMETICALLY
SEALED ENCAPSULATION OR
DUAL IN-LINE PLASTIC
ENCAPSULATION

1. Limiting conditions of use (not for inspection purposes)

Absolute values (non-simultaneous)

			Units
V_{CC}	Maximum continuous positive supply voltage	7.0	V
	Maximum continuous negative supply voltage	0.5	V
	Maximum continuous positive input voltage	5.5	V
	Maximum continuous negative input voltage	0.5	V
$-I_{IL}$	Maximum input current	(Shift/Load input)	3.2 mA
		(Other inputs)	1.6 mA
	Maximum reverse input current	1.0	mA
T_{amb}	Ambient operating temperature range	54165	-55 to +125 °C
		64165	-40 to +85 °C
		74165	0 to +70 °C
T_{sto}	Storage temperature range	-85 to +150	°C
	Shock (0.5 ms duration)	14 700	m/s ²
	Vibration	196	m/s ²

Copies of this specification are available from manufacturers listed in the Qualified Products List, Part 1 of PD 9002.

BS 9440 F040 to 042
BS 9440 F067 to 069
BS 9440 F174 to 180

Issue 1, March 1978

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

Over the full ambient operating temperature range unless otherwise stated.

			Min.	Max.	Units
V_{CC}	Positive supply voltage	54165	4.5	5.5	V
		64165 & 74165	4.75	5.25	V
V_{IH}	HIGH state input voltage	54165	2.0	5.5	V
		64165 & 74165	2.0	5.25	V
I_{CC}	Total supply current per package at V_{CC} maximum value			63.0	mA
V_{OH}	HIGH state output voltage		2.4		V
V_{IL}	LOW state input voltage		0	0.8	V
V_{OL}	LOW state output voltage			0.4	V
$I_{IH(1)}$	HIGH state input current at $V_{IN} = V_{IH}$ maximum value			1.0	mA
$I_{IH(2)}$	HIGH state input current at $V_{IN} = 2.4V$ (Shift/Load input)			80.0	μA
	(Other inputs)			40.0	μA
$-I_{IL}$	LOW state input current at $V_{IN} = 0.4V$ (Shift/Load input)			3.2	mA
	(Other inputs)			1.6	mA
I_{OL}	LOW state output current			16.0	mA
$-I_{OH}$	HIGH state output current			800.0	μA
$-I_{OS}$	Output short circuit current	54165	20.0	55.0	mA
		64165 & 74165	18.0	55.0	mA
t_{PHL}	HIGH to LOW state propagation time at 25°C*			40.0	ns
t_{PLH}	LOW to HIGH state propagation time at 25°C*			31.0	ns
	Frequency of operation			≥ 20.0	MHz
$t_{(set-up)}$	Set-up time	(Clock Enable)	30.0		ns
		(Parallel input)	10.0		ns
		(Serial input)	20.0		ns
		(Shift)	45.0		ns
$t_{(hold)}$	Hold time for any input		0		ns
$t_{p(clock)}$	Width of clock pulse		25.0		ns
$t_{p(load)}$	Width of load pulse		15.0		ns

*See subgroup A4 for details.

Table I
Function table

INPUTS					INTERNAL OUTPUTS		OUTPUT Q _H
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel			
				A H	Q _A	Q _B	
L	X	X	X	a h	a	b	h
H	L	L	X	X	Q _{AO}	Q _{BO}	Q _{HO}
H	L	↑	H	X	H	Q _{AN}	Q _{GN}
H	L	↑	L	X	L	Q _{AN}	Q _{GN}
H	H	↑	X	X	Q _{AO}	Q _{BO}	Q _{HO}

X = Irrelevant (any input, including transitions).

↑ = Transition from LOW to HIGH level.

a h = The level of steady-state input at inputs A to H respectively.

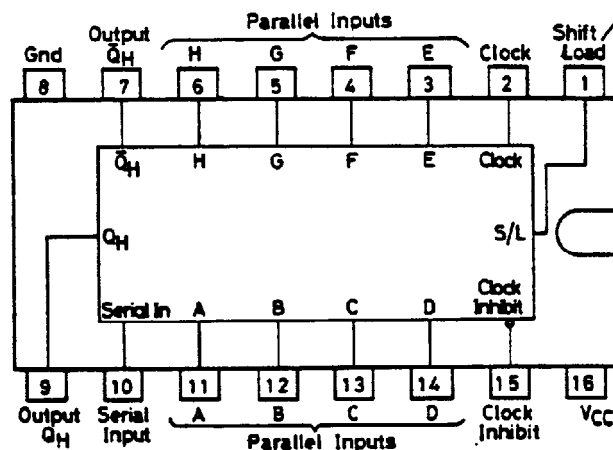
Q_{AO} , Q_{BO} , Q_{HO} = The level of Q_A , Q_B , Q_H respectively before the indicated steady-state input conditions were established.

Q_{AN} , Q_{GN} = The level of Q_A , Q_G respectively before the most-recent ↑ transition of the clock.

The 8-bit, parallel-load, serial shift register, when clocked, shifts data in the direction Q_A towards Q_H .

Parallel loading is accomplished by presenting the data to be loaded at the parallel inputs (A to H) and applying a HIGH to LOW-level signal at the Shift/Load input. Parallel loading is inhibited while the Shift/Load input is HIGH.

Two clock inputs (Clock and Clock Inhibit) are provided. With either of the clock inputs HIGH, clocking is inhibited. With either clock input LOW and the Shift/Load input HIGH, the other clock (i.e. the clock not held LOW) is enabled. The Clock Inhibit input should be changed to HIGH only while the Clock input is HIGH.

Table II
Logic diagram and connections

BS 9440 F040 to 042
BS 9440 F067 to 069
BS 9440 F174 to 180

Issue 1, March 1978

3. Marking

- (1) Each integrated circuit shall bear the following markings:
 - a. Terminal identification.
 - b. The manufacturer's type number.
 - c. The factory identification code.
 - d. The date code.
- (2) Each package containing one or more of these circuits shall bear the markings 'b', 'c' and 'd' above and in addition:
 - e. The BS detail specification number e.g., BS 9440 F040.

4. Related documents

BS 3934 'Dimensions of semiconductor devices',
BS 6001 'Sampling procedures and tables for inspection by attributes',
BS 9000 'General requirements for electronic components of assessed quality',
PD 9002 'Qualified products list for electronic components of assessed quality',
BS 9400 'Integrated electronic circuits of assessed quality: Generic data and methods of test'.

5. Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturer's integrated circuit type and package identification as detailed in PD 9002 to BS 9440 F... as defined below.

TYPE		APPLICATION CATEGORY				FULL ASSESSMENT LEVEL
		S1	S2	S3	S4	
CERAMIC Dual in-line and Flat-Pack	54165	F067	F068	F069	F174	F040
	64165	★	F175	F176	F177	F041
	74165	★	F178	F179	F180	F042
PLASTIC Dual in-line	54165	★	★	★	★	F040
	64165	★	★	★	★	F041
	74165	★	★	★	★	F042

★ = Not available at the present time.